Chapter 18 TSP(Transport Stream Processing Module)

18.1 Overview

The Transport Stream Processing Module(TSP) is designed for processing Transport Stream Packets, including receiving TS packets, PID filtering, TS descrambling, De-multiplexing and TS outputting. Processed data are transferred to memory buffer which are continued to be processing by software.
TPS supports the following features:
    Supports two TS input channels and one TS output channel
    Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input
    Supports serial and parallel output mode with PCR adjustment, and lsb-msb or msb-lsb bit ordering can be chosen in the serial output mode
    Supports 2 TS sources: demodulators and local memory
    Supports 2 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously
    Supports 1 PVR(Personal Video Recording) output channel
    1 built-in multi-channel DMA Controller
    DMAC supports:
    Word alignment transfer
    Fixed and incrementing addressing
    Word size transfer
    burst modes: Incr4, Incr8, Inc16; burst transfer will be done with INCR mode if the remaining data or address space is not capable to perform a complete burst transfer
    Hardware/software trigger mode
    LLP(List Link Programming) Mode
    DMA done and error interrupt for each PTI channel
    Each PTI supports
    64 PID filters
    TS descrambling with 16 sets of Control Word under CSA v2.0 standard,   up to 104Mbps
    16 PES/ES filters with PTS/DTS extraction and ES start code detection
    4/8 PCR extraction channels
    64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
    PID done and error interrupts for each channel
    PCR/DTS/PTS extraction interrupt for each channel

18.2 Block Diagram

The TSP comprises of following components:
    AMBA AHB slave interface
    Register block
   PTI
    DMAC
    TS Out Interface
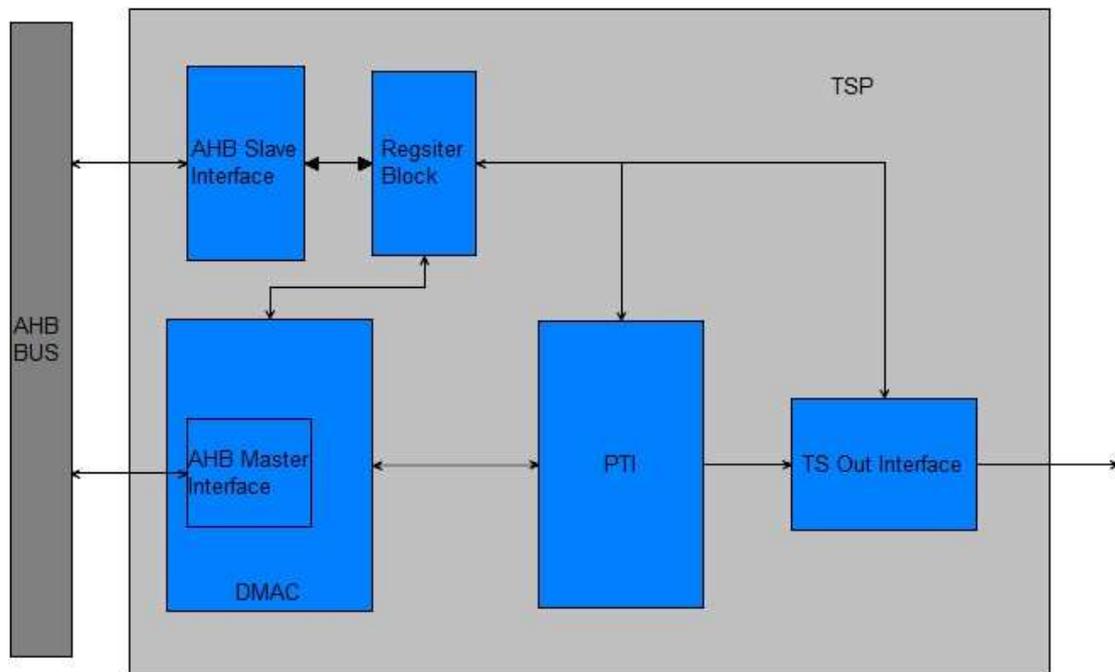
Fig. 18-1 TSP architecture

AHB Slave INTERFACE
The host processor can get access to the register block through AHB slave interface. The slave interface supports 32bit access.
Register block
All registers in the TSP are addressed at 32-bit boundaries to remain consistent with the AHB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.
PTI
Most of the TS processing are dealt with PTI. TS packets are re-synchronized, filtered, descrambled and demultiplexing, and the processed packets are transferred to memory buffer to be processed further by software. The embedded TS in interface can receive TS packets by connecting to a compliant TS demodulator. TS stream stored in the local memory is another source to fed into PTI through by using LLP DMA mode.
TS Out Interface
TS out interface can output either PID-filtered or non-PID-filtered TS packets from one PTI channel in a certain stream mode as configured. The TS receiver conforms to the stream mode to receive the TS packets.
DMAC
The DMAC performs all DMA transfers which get access to memory.

18.3 Function Description

18.3.1 TS Stream of TS_IN Interface

TS_IN interface supports 4 input TS stream mode: sync/valid serial mode, sync/valid parallel mode, sync/burst parallel mode, nosync/valid parallel mode.
A. Sync/Valid Serial Mode
In this mode, TS_IN interface takes use of TSI_SYNC and TSI_VALID clocked with TSI_CLK signal to sample input serial TS packet data.
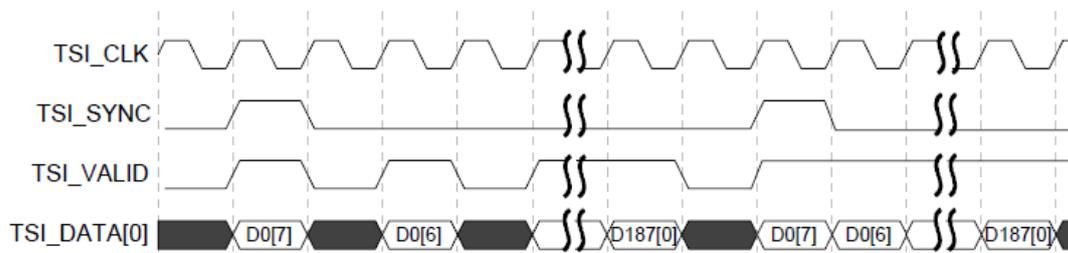
Fig. 18-2 Sync/Valid Serial Mode with Msb-Lsb Bit Ordering

TSI_SYNC must be active high together with TSI_VALID when indicating the first valid bit of a TS packet, and TSI_VALID indicates the 188*8 valid bits of a TS packet. TSI supports both msb-lsb and lsb-msb bit ordering.

B. Sync/Valid Parallel Mode

In this mode, TS_IN interface takes use of TSI_SYNC and TSI_VALID clocked with TSI_CLK signal to sample input parallel TS packet data.
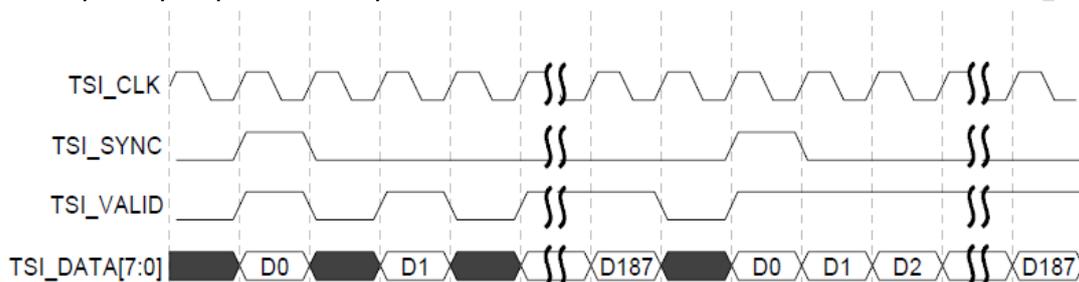

Fig. 18-3 Sync/valid Parallel Mode

TSI_SYNC must be active high together with TSI_VALID when indicating the first valid byte of a TS packet, and TSI_VALID indicates the 188 valid byte of a TS packet.

C. Sync/Burst Parallel Mode

In this mode, TSI only takes use of TSI_SYNC to sample input parallel TS packet data.
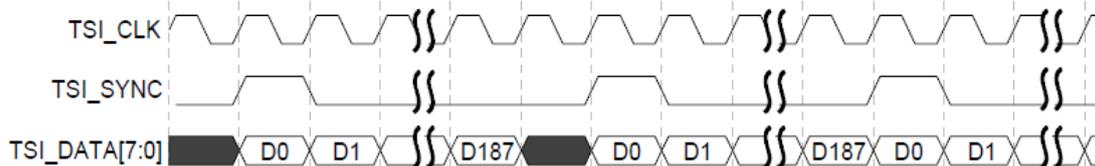
Fig. 18-4 Sync/Burst Parallel Mode

When active high, TSI_SYNC implies the first valid byte of a TS packet and remaining 187 valid bytes of a TS packet are upcoming within the following successive 187 clock cycles.

D. Nosync/Valid Parallel Mode

In this mode, TSI only takes uses of TSI_VALID to sample input parallel TS packet data.
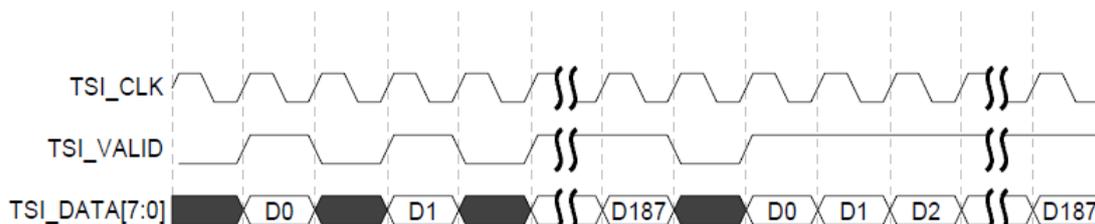
Fig. 18-5 Nosync/Valid Parallel Mode

When active high, TSI_VALID implies a valid byte of a TS packet.

18.3.2 TS output of TS Out Interface

TS out interface transmit the TS data in two mode: serial mode and parallel mode. In the serial mode, the bit order can be lsb-msb or msb-lsb.

The TS_SYNC will be active high when indicating the header of the TS packets, and it only lasts for one cycle. TS_VALID will be active high when the output TS data is valid. The output data is 188 byte TS packet data.

TS out interface also stamp the TS output stream with new PCR value, making PCR adjustment.

PCR is used to measure the transport rate.

$$PCR(i) = PCR\_base(i) \times 300 + PCR\_ext(i)$$

where:

$$PCR\_base(i) = ((system\_clock\_frequency \times t(i))\ DIV\ 300)\ \%\ 2^{33}$$

$$PCR\_ext(i) = ((system\_clock\_frequency \times t(i))\ DIV\ 1)\ \%\ 300$$

$$transport\_rate(i) = \frac{((i' - i'') \times system\_clock\_frequency)}{PCR(i') - PCR(i'')}$$

Where

i' is the index of the byte containing the last bit of the immediately following program_clock_reference_base field applicable to the program being decoded.

i is the is the index of any byte in the Transport Stream for $i'' < i < i'$.

i'' is the index of the byte containing the last bit of the most recent program_clock_reference_base field applicable to the program being decoded.

System clock is 27Mhz.

18.3.3 Demux and descrambling

Each PTI has 64 PID channels to deal with demultiplexing and descrambling operation.
The PTI can descramble the TS Packets which are scrambled with CSA v2.0 standard. The TS packets can be scrambled either in TS level or PES level.
The demux module can do the section filtering, pes filtering and es filtering, or directly output TS packets.

18.4 Register Description

18.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
TSP_GCFG	0x0000	W	0x00000000	Global Configuration Register
TSP_PVR_CTRL	0x0004	W	0x00000000	PVR Control Register
TSP_PVR_LEN	0x0008	W	0x00000000	PVR DMA Transaction Length
TSP_PVR_ADDR	0x000c	W	0x00000000	PVR DMA transaction starting address
TSP_PVR_INT_STS	0x0010	W	0x00000000	PVR DMA Interrupt Status Register
TSP_PVR_INT_ENA	0x0014	W	0x00000000	DMA Interrupt Enable Register
TSP_TSOUT_CTRL	0x0018	W	0x00000000	TS Out Control Register
TSP_PTIx_CTRL	0x0100	W	0x00000000	PTI Channel Control Register
TSP_PTIx_LLP_CFG	0x0104	W	0x00000000	LLP DMA Control Register
TSP_PTIx_LLP_BASE	0x0108	W	0x00000000	LLP Descriptor BASE Address
TSP_PTIx_LLP_WRITE	0x010c	W	0x00000000	LLP DMA Writing Software Descriptor Counter
TSP_PTIx_LLP_READ	0x0110	W	0x00000000	LLP DMA Reading Hardware Descriptor Counter
TSP_PTIx_PID_STS0	0x0114	W	0x00000000	PTI PID Channel Status 0 Register
TSP_PTIx_PID_STS1	0x0118	W	0x00000000	PTI PID Channel Status 1 Register
TSP_PTIx_PID_STS2	0x011c	W	0x00000000	PTI PID Channel Status 2 Register

Name	Offset	Size	Reset Value	Description
TSP_PTIx_PID_STS3	0x0120	W	0x00000000	PTI PID Channel Status 3 Register
TSP_PTIx_PID_INT_ENA0	0x0124	W	0x00000000	PID Interrupt Enable Register 0
TSP_PTIx_PID_INT_ENA1	0x0128	W	0x00000000	PID Interrupt Enable Register 1
TSP_PTIx_PID_INT_ENA2	0x012c	W	0x00000000	PID Interrupt Enable Register 2
TSP_PTIx_PID_INT_ENA3	0x0130	W	0x00000000	PID Interrupt Enable Register 3
TSP_PTIx_PCR_INT_STS	0x0134	W	0x00000000	PTI PCR Interrupt Status Register
TSP_PTIx_PCR_INT_ENA	0x0138	W	0x00000000	PTI PCR Interrupt Enable Register
TSP_PTIx_PCRn_CTRL	0x013c	W	0x00000000	PID PCR Control Register
TSP_PTIx_PCRn_H	0x015c	W	0x00000000	High Order PCR value
TSP_PTIx_PCRn_L	0x0160	W	0x00000000	Low Order PCR value
TSP_PTIx_DMA_STS	0x019c	W	0x00000000	LLP DMA Interrupt Status Register
TSP_PTIx_DMA_ENA	0x01a0	W	0x00000000	DMA Interrupt Enable Register
TSP_PTIx_DATA_FLAG0	0x01a4	W	0x00000000	PTI_PID_WRITE Flag 0
TSP_PTIx_DATA_FLAG1	0x01a8	W	0x00000000	PTI_PID_WRITE Flag 1
TSP_PTIx_LIST_FLAG	0x01ac	W	0x00000000	PTIx_LIST_WRITE Flag
TSP_PTIx_DST_STS0	0x01b0	W	0x00000000	PTI Destination Status Register
TSP_PTIx_DST_STS1	0x01b4	W	0x00000000	PTI Destination Status Register
TSP_PTIx_DST_ENA0	0x01b8	W	0x00000000	PTI Destination Interrupt Enable Register
TSP_PTIx_DST_ENA1	0x01bc	W	0x00000000	PTI Destination Interrupt Enable Register
TSP_PTIx_ECWn_H	0x0200	W	0x00000000	The Even Control Word High Order
TSP_PTIx_ECWn_L	0x0204	W	0x00000000	The Even Control Word Low Order
TSP_PTIx_OCWn_H	0x0208	W	0x00000000	The Odd Control Word High Order
TSP_PTIx_OCWn_L	0x020c	W	0x00000000	The Odd Control Word Low Order
TSP_PTIx_PIDn_CTRL	0x0300	W	0x00000000	PID Channel Control Register
TSP_PTIx_PIDn_BASE	0x0400	W	0x00000000	PTI Data Memory Buffer Base Address
TSP_PTIx_PIDn_TOP	0x0404	W	0x00000000	PTI Data Memory Buffer Top Address
TSP_PTIx_PIDn_WRITE	0x0408	W	0x00000000	PTI Data Memory Buffer Hardware Writing Address
TSP_PTIx_PIDn_READ	0x040c	W	0x00000000	PTI Data Memory Buffer Software Reading Address
TSP_PTIx_LISTn_BASE	0x0800	W	0x00000000	PTI List Memory Buffer Base Address
TSP_PTIx_LISTn_TOP	0x0804	W	0x00000000	PTI List Memory Buffer Top Address
TSP_PTIx_LISTn_WRITE	0x0808	W	0x00000000	PTI List Memory Buffer Hardware Writing Address
TSP_PTIx_LISTn_READ	0x080c	W	0x00000000	PTI List Memory Buffer Software Reading Address
TSP_PTIx_PIDn_CFG	0x0900	W	0x00000008	PID Demux Configure Register
TSP_PTIx_PIDn_FILT_0	0x0904	W	0x00000000	Fliter Word 0
TSP_PTIx_PIDn_FILT_1	0x0908	W	0x00000000	Fliter Word 1

Name	Offset	Size	Reset Value	Description
TSP_PTIx_PIDn_FILT_2	0x090c	W	0x00000000	Fliter Word 2
TSP_PTIx_PIDn_FILT_3	0x0910	W	0x00000000	Fliter Word 3

*Notes: <u>Size</u> : **B** - Byte (8 bits) access,   **HW** - Half WORD (16 bits) access,   **W** -WORD (32 bits) access*

18.4.2 Detail Register Description

TSP_GCFG
Address: Operational Base + offset (0x0000)
Global Configuration Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:4	RW	0x0	arbit_cnt DMA channel arbiter counter This field is used to adjust the priority of DMA channels to prevent one channel holds the highest priority for a long time. The 3-bit field sets the largest times for a DMA channel to hold the highest priority to send the bus request. After requested times reach this limit, the highest priority is passed to next DMA channel in order.
3	RW	0x0	tsout_on TS Output Module Switch 1: TS output module switched on 0: TS output module switched off
2	RW	0x0	pvr_on PVR Module Switch 1: PVR function turned on ; 0: PVR function turned off ;
1	RW	0x0	pti1_on PTI0 channel switch 1: PTI1 channel switched on 0: PTI1 channel switched off
0	RW	0x0	pti0_on PTI0 channel switch 1: PTI0 channel switched on 0: PTI1 channel switched off

TSP_PVR_CTRL
Address: Operational Base + offset (0x0004)
PVR Control Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	fixaddr_en Fix Address Mode Select 1: fixed address mode; 0: incrementing address mode;
5:4	RW	0x0	burst_mode PVR burst mode PVR DMA burst mode 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 2'b11: Reserverd
3:2	RW	0x0	source PVR Source Select TS source for PVR output. 00: non-PID-filtered TS packets in PTI0; 01: PID filtered TS packets in PTI0; 10: non-PID-filtered TS packets in PTI1; 11: PID-filtered TS packets in PTI1;
1	R/WSC	0x0	stop PVR stop Write 1 to stop DMA channel. DMA will complete current burst transfer and then stop. It may takes several cycles. 1: PVR Stop ; 0: no effect ;
0	R/WSC	0x0	start PVR start Write 1 to start PVR. This bit will be cleared if PVR is stopped or PVR transaction is completed. 1: start PVR 0: no effect.

TSP_PVR_LEN
Address: Operational Base + offset (0x0008)
PVR DMA Transaction Length

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	len Transaction Length Transaction Length

TSP_PVR_ADDR
Address: Operational Base + offset (0x000c)
PVR DMA transaction starting address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr PVR DMA transaction starting address PVR DMA transaction starting address

TSP_PVR_INT_STS
Address: Operational Base + offset (0x0010)
PVR DMA Interrupt Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	W1C	0x0	pvr_error PVR DMA transaction error 1: error response during PVR DMA transaction; 0: no error response during PVR DMA transaction;
0	W1C	0x0	pvr_done PVR DMA transaction done 1: PVR DMA transaction completed; 0: PVR DMA transaction not completed;

TSP_PVR_INT_ENA
Address: Operational Base + offset (0x0014)
DMA Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	pvr_error_ena PVR DMA Transcation Error Interrupt Enable 1: Error Interrupt Enabled 0: Error Interrupt Disabled
0	RW	0x0	pvr_done_ena PVR DMA Transaction Done Interrupt Enable 1: Done Interrupt Enabled 0: Done Interrupt Disabled

TSP_TSOUT_CTRL
Address: Operational Base + offset (0x0018)
TS Out Control Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	tso_sdo_sel TS serial data output 1: bit[0] use as serial data output ; 0: bit[7] use as serial data output ;

Bit	Attr	Reset Value	Description
5	RW	0x0	tso_clk_phase TS output clock phase 0: ts output clock; 1: inverse of ts output clock.
4	RW	0x0	mode TS Output mode Selection Output mode select: 0: Serial Mode 1: Parallel Mode
3	RW	0x0	bit_order ts output serial data byte order Indicates that the output serial data byte order, ignored in the parallel: 0: MSB to LSB 1: LSB to MSB
2:1	RW	0x0	source TS Output Source Select TS source for TS out. 00: non-PID-filtered TS packets in PTI0; 01: PID filtered TS packets in PTI0; 10: non-PID-filtered TS packets in PTI1; 11: PID-filtered TS packets in PTI1;
0	RW	0x0	start TS out start 1: to start TS out function ; 0: to stop TS out function;

TSP_PTIx_CTRL
Address: Operational Base + offset (0x0100)
PTI Channel Control Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	tsi_sdi_sel TS Serial Data Input Select 1: bit[0] use as serial input data 0: bit[7] use as serial input data
20:19	RW	0x0	tsi_error_handle TS ERROR Handle 00: don't output 01: set the error indicator to 1 10: don't care
18	RW	0x0	clk_phase_sel ts input clock phase select 1'b0: ts input clock 1'b1: inverse of ts input clock

Bit	Attr	Reset Value	Description
17:16	RW	0x0	demux_burst_mode Demux DMA Burst Mode Demux DMA Mode 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 2'b11: Reserved
15	RW	0x0	sync_bypass Bypass mode Selection 1'b1: Bypass mode, indicating that input TS packets will not be resynchronized and directly fed into the following modules; 1'b0: Synchronous mode, default, indicating that input TS packets will be resynchronized;
14	RW	0x0	cw_byteorder Control Word format Configuration 0: Default: first byte of the word is the highest byte 1: first byte of the word is the lowest byte
13	RW	0x0	cm_on CSA Conformance Mechanism Configuration CSA Conformance Mechanism 0: CM turned off 1: CM turned on
12:11	RW	0x0	tsi_mode TSI Input Mode Selection Input mode selection: 00: Serial Sync/valid Mode 01: Parallel Sync/valid Mode 10: Parallel Sync/burst Mode 11: Parallel Nosync/valid Mode
10	RW	0x0	tsi_bit_order input serial data order Indicates that the input serial data byte order, ignored in the parallel mode: 0: MSB to LSB 1: LSB to MSB
9	RW	0x0	tsi_sel TS Input Source Select Select input TS source 1'b1: HSADC ; 1'b0: internel memory ;

Bit	Attr	Reset Value	Description
8	RW	0x0	out_byteswap Output byteswap function When enabled, the word to be transferred to memory buffer "B4B3B2B1" is performed byteswapping to "B1B2B3B4".
7	RW	0x0	in_byteswap Input TS Word Byteswap When enabled, the input TS word "B4B3B2B1" is perfomed byteswapping to "B1B2B3B4".
6:4	RW	0x0	unsync_times TS Header Unsynchronized Times If synchronous mode is selected. This field sets the successive times of TS packet header error to re-lock TS header when TS is in locked status;
3:1	RW	0x0	sync_times TS Header Synchronized Times If synchronous mode is selected. This field sets the successive times of finding TS packet header to lock the TS header when TS is in unlocked status;
0	R/WSC	0x0	clear Software clear signal It will reset the core register . It will table several cycles. After reset done, soft_reset will be low. 1. reset; 0. no effect.

TSP_PTIx_LLP_CFG
Address: Operational Base + offset (0x0104)
LLP DMA Control Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:8	RW	0x0	threshold LLP Transfer Threshold The depth for LLP descriptors is 64. An interrupt will be asserted when transfer reaches the threshold set if DMA transfer interrupt is enabled. 00: 1/1 depth 01: 1/2 depth 10: 1/4 depth 11: 1/8 depth

Bit	Attr	Reset Value	Description
7:6	RW	0x0	burst_mode LLP DMA Burst Mode LLP DMA Burst Mode 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 2'b11: Reserverd
5	RW	0x0	hw_trigger Hardware Trigger Select 1. hardware trigger; 0. software trigger;
4	RW	0x0	fix_addr_en Fix Address Mode Select 1: fixed address mode; 0: incrementing address mode;
3	W1C	0x0	cfg_done LLP DMA Configuration Done When all descriptors of LLP are configured, write 1 to to this bit. The core will clear this bit when llp transction is finished ;
2	RW	0x0	pause LLP DMA Pause Write 1 to Pause DMA channel . DMA will complete current burst transfer and then pause. All register stay unchange. If software write 0 later , It will continue to work. It may take several cycles to pause. 1: pause; 0: continue to work ;
1	W1C	0x0	stop LLP DMA Stop Write 1 to stop DMA channel. DMA will complete current burst transter and then stop. It may takes several cycles. 1: stop ; 0: no effect ;
0	W1C	0x0	start LLP DMA start Write 1 to start DMA Channel , self clear after 1 cycle. 1: start ; 0: no effect

TSP_PTIx_LLP_BASE
Address: Operational Base + offset (0x0108)

LLP Descriptor BASE Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr LLP Descriptor BASE Address LLP Descriptor BASE address

TSP_PTIx_LLP_WRITE
Address: Operational Base + offset (0x010c)
LLP DMA Writing Software Descriptor Counter

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	counter LLP DMA Writing Software Descriptor Counter LLP DMA Writing Software Descriptor Counter

TSP_PTIx_LLP_READ
Address: Operational Base + offset (0x0110)
LLP DMA Reading Hardware Descriptor Counter

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	counter LLP DMA Reading Hardware Descriptor Counter LLP DMA Reading Hardware Descriptor Counter

TSP_PTIx_PID_STS0
Address: Operational Base + offset (0x0114)
PTI PID Channel Status 0 Register

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_done PID31 Channel Status 1 means done
30	W1C	0x0	pid30_done PID30 Channel Status 1 means done
29	W1C	0x0	pid29_done PID29 Channel Status 1 means done
28	W1C	0x0	pid28_done PID28 Channel Status 1 means done
27	W1C	0x0	pid27_done PID27 Channel Status 1 means done

Bit	Attr	Reset Value	Description
26	W1C	0x0	pid26_done PID26 Channel Status 1 means done
25	W1C	0x0	pid25_done PID25 Channel Status 1 means done
24	W1C	0x0	pid24_done PID24 Channel Status 1 means done
23	W1C	0x0	pid23_done PID23 Channel Status 1 means done
22	W1C	0x0	pid22_done PID22 Channel Status 1 means done
21	W1C	0x0	pid21_done PID21 Channel Status 1 means done
20	W1C	0x0	pid20_done PID20 Channel Status 1 means done
19	W1C	0x0	pid19_done PID19 Channel Status 1 means done
18	W1C	0x0	pid18_done PID18 Channel Status 1 means done
17	W1C	0x0	pid17_done PID17 Channel Status 1 means done
16	W1C	0x0	pid16_done PID16 Channel Status 1 means done
15	W1C	0x0	pid15_done PID15 Channel Status 1 means done
14	W1C	0x0	pid14_done PID14 Channel Status 1 means done
13	W1C	0x0	pid13_done PID13 Channel Status 1 means done
12	W1C	0x0	pid12_done PID12 Channel Status 1 means done

Bit	Attr	Reset Value	Description
11	W1C	0x0	pid11_done PID11 Channel Status 1 means done
10	W1C	0x0	pid10_done PID10 Channel Status 1 means done
9	W1C	0x0	pid9_done PID9 Channel Status 1 means done
8	W1C	0x0	pid8_done PID8 Channel Status 1 means done
7	W1C	0x0	pid7_done PID7 Channel Status 1 means done
6	W1C	0x0	pid6_done PID6 Channel Status 1 means done
5	W1C	0x0	pid5_done PID5 Channel Status 1 means done
4	W1C	0x0	pid4_done PID4 Channel Status 1 means done
3	W1C	0x0	pid3_done PID3 Channel Status 1 means done
2	RW	0x0	pid2_done PID2 Channel Status 1 means done
1	W1C	0x0	pid1_done PID1 Channel Status 1 means done
0	W1C	0x0	pid0_done PID0 Channel Status 1 means done

TSP_PTIx_PID_STS1
Address: Operational Base + offset (0x0118)
PTI PID Channel Status 1 Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	pid63_done PID63 Channel Status 1 means done

Bit	Attr	Reset Value	Description
30	W1C	0x0	pid62_done PID62 Channel Status 1 means done
29	W1C	0x0	pid61_done PID61 Channel Status 1 means done
28	W1C	0x0	pid60_done PID60 Channel Status 1 means done
27	W1C	0x0	pid59_done PID59 Channel Status 1 means done
26	W1C	0x0	pid58_done PID58 Channel Status 1 means done
25	W1C	0x0	pid57_done PID57 Channel Status 1 means done
24	W1C	0x0	pid56_done PID56 Channel Status 1 means done
23	W1C	0x0	pid55_done PID55 Channel Status 1 means done
22	W1C	0x0	pid54_done PID54 Channel Status 1 means done
21	W1C	0x0	pid53_done PID53 Channel Status 1 means done
20	W1C	0x0	pid52_done PID52 Channel Status 1 means done
19	W1C	0x0	pid51_done PID51 Channel Status 1 means done
18	W1C	0x0	pid50_done PID51 Channel Status 1 means done
17	W1C	0x0	pid49_done PID49 Channel Status 1 means done
16	W1C	0x0	pid48_done PID48 Channel Status 1 means done

Bit	Attr	Reset Value	Description
15	W1C	0x0	pid47_done PID47 Channel Status 1 means done
14	W1C	0x0	pid46_done PID46 Channel Status 1 means done
13	W1C	0x0	pid45_done PID45 Channel Status 1 means done
12	W1C	0x0	pid44_done PID44 Channel Status 1 means done
11	W1C	0x0	pid43_done PID43 Channel Status 1 means done
10	W1C	0x0	pid42_done PID42 Channel Status 1 means done
9	W1C	0x0	pid41_done PID41 Channel Status 1 means done
8	W1C	0x0	pid40_done PID40 Channel Status 1 means done
7	W1C	0x0	pid39_done PID39 Channel Status 1 means done
6	W1C	0x0	pid38_done PID38 Channel Status 1 means done
5	W1C	0x0	pid37_done PID37 Channel Status 1 means done
4	W1C	0x0	pid36_done PID36 Channel Status 1 means done
3	RW	0x0	pid35_done PID35 Channel Status 1 means done
2	W1C	0x0	pid34_done PID34 Channel Status 1 means done
1	W1C	0x0	pid33_done PID33 Channel Status 1 means done

Bit	Attr	Reset Value	Description
0	RW	0x0	pid32_done PID32 Channel Status 1 means done

TSP_PTIx_PID_STS2
Address: Operational Base + offset (0x011c)
PTI PID Channel Status 2 Register

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_error PID31 Error Interrupt Status 1 means error detected
30	W1C	0x0	pid30_error PID30 Error Interrupt Status 1 means error detected
29	W1C	0x0	pid29_error PID29 Error Interrupt Status 1 means error detected
28	W1C	0x0	pid28_error PID28 Error Interrupt Status 1 means error detected
27	W1C	0x0	pid27_error PID27 Error Interrupt Status 1 means error detected
26	W1C	0x0	pid26_error PID26 Error Interrupt Status 1 means error detected
25	W1C	0x0	pid25_error PID25 Error Interrupt Status 1 means error detected
24	W1C	0x0	pid24_error PID24 Error Interrupt Status 1 means error detected
23	W1C	0x0	pid23_error PID23 Error Interrupt Status 1 means error detected
22	W1C	0x0	pid22_error PID22 Error Interrupt Status 1 means error detected
21	W1C	0x0	pid21_error PID21 Error Interrupt Status 1 means error detected
20	W1C	0x0	pid20_error PID20 Error Interrupt Status 1 means error detected

Bit	Attr	Reset Value	Description
19	W1C	0x0	pid19_error PID19 Error Interrupt Status 1 means error detected
18	W1C	0x0	pid18_error PID18 Error Interrupt Status 1 means error detected
17	W1C	0x0	pid17_error PID17 Error Interrupt Status 1 means error detected
16	W1C	0x0	pid16_error PID16 Error Interrupt Status 1 means error detected
15	W1C	0x0	pid15_error PID15 Error Interrupt Status 1 means error detected
14	W1C	0x0	pid14_error PID14 Error Interrupt Status 1 means error detected
13	W1C	0x0	pid13_error PID13 Error Interrupt Status 1 means error detected
12	W1C	0x0	pid12_error PID12 Error Interrupt Status 1 means error detected
11	W1C	0x0	pid11_error PID11 Error Interrupt Status 1 means error detected
10	W1C	0x0	pid10_error PID10 Error Interrupt Status 1 means error detected
9	W1C	0x0	pid9_error PID9 Error Interrupt Status 1 means error detected
8	W1C	0x0	pid8_error PID8 Error Interrupt Status 1 means error detected
7	W1C	0x0	pid7_error PID7 Error Interrupt Status 1 means error detected
6	W1C	0x0	pid6_error PID6 Error Interrupt Status 1 means error detected
5	W1C	0x0	pid5_error PID5 Error Interrupt Status 1 means error detected

Bit	Attr	Reset Value	Description
4	W1C	0x0	pid4_error PID4 Error Interrupt Status 1 means error detected
3	W1C	0x0	pid3_error PID3 Error Interrupt Status 1 means error detected
2	W1C	0x0	pid2_error PID2 Error Interrupt Status 1 means error detected
1	W1C	0x0	pid1_error PID1 Error Interrupt Status 1 means error detected
0	W1C	0x0	pid0_error PID0 Error Interrupt Status 1 means error detected

TSP_PTIx_PID_STS3
Address: Operational Base + offset (0x0120)
PTI PID Channel Status 3 Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	pid63_error PID63 Error Interrupt Status
30	W1C	0x0	pid62_error PID62 Error Interrupt Status
29	W1C	0x0	pid61_error PID61 Error Interrupt Status
28	W1C	0x0	pid60_error PID60 Error Interrupt Status
27	W1C	0x0	pid59_error PID59 Error Interrupt Status
26	W1C	0x0	pid58_error PID58 Error Interrupt Status
25	W1C	0x0	pid57_error PID57 Error Interrupt Status
24	W1C	0x0	pid56_error PID56 Error Interrupt Status
23	W1C	0x0	pid55_error PID55 Error Interrupt Status
22	W1C	0x0	pid54_error PID54 Error Interrupt Status
21	W1C	0x0	pid53_error PID53 Error Interrupt Status
20	W1C	0x0	pid52_error PID52 Error Interrupt Status

Bit	Attr	Reset Value	Description
19	W1C	0x0	pid51_error PID51 Error Interrupt Status
18	W1C	0x0	pid50_error PID50 Error Interrupt Status
17	W1C	0x0	pid49_error PID49 Error Interrupt Status
16	W1C	0x0	pid48_error PID48 Error Interrupt Status
15	W1C	0x0	pid47_error PID47 Error Interrupt Status
14	W1C	0x0	pid46_error PID46 Error Interrupt Status
13	W1C	0x0	pid45_error PID45 Error Interrupt Status
12	W1C	0x0	pid44_error PID44 Error Interrupt Status
11	W1C	0x0	pid43_error PID43 Error Interrupt Status
10	W1C	0x0	pid42_error PID42 Error Interrupt Status
9	W1C	0x0	pid41_error PID41 Error Interrupt Status
8	W1C	0x0	pid40_error PID40 Error Interrupt Status
7	W1C	0x0	pid39_error PID39 Error Interrupt Status
6	W1C	0x0	pid38_error PID38 Error Interrupt Status
5	W1C	0x0	pid37_error PID37 Error Interrupt Status
4	W1C	0x0	pid36_error PID36 Error Interrupt Status
3	W1C	0x0	pid35_error PID35 Error Interrupt Status
2	W1C	0x0	pid34_error PID34 Error Interrupt Status
1	W1C	0x0	pid33_error PID33 Error Interrupt Status
0	W1C	0x0	pid32_error PID32 Error Interrupt Status

TSP_PTIx_PID_INT_ENA0
Address: Operational Base + offset (0x0124)
PID Interrupt Enable Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_done_ena PID31 Done Enable 1:enabled 0:disabled
30	RW	0x0	pid30_done_ena PID30 Done Enable 1:enabled 0:disabled
29	RW	0x0	pid29_done_ena PID29 Done Enable 1:enabled 0:disabled
28	RW	0x0	pid28_done_ena PID28 Done Enable 1:enabled 0:disabled
27	RW	0x0	pid27_done_ena PID27 Done Enable 1:enabled 0:disabled
26	RW	0x0	pid26_done_ena PID26 Done Enable 1:enabled 0:disabled
25	RW	0x0	pid25_done_ena PID25 Done Enable 1:enabled 0:disabled
24	RW	0x0	pid24_done_ena PID24 Done Enable 1:enabled 0:disabled
23	RW	0x0	pid23_done_ena PID23 Done Enable 1:enabled 0:disabled
22	RW	0x0	pid22_done_ena PID22 Done Enable 1:enabled 0:disabled
21	RW	0x0	pid21_done_ena PID21 Done Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
20	RW	0x0	pid20_done_ena PID20 Done Enable 1:enabled 0:disabled
19	RW	0x0	pid19_done_ena PID19 Done Enable 1:enabled 0:disabled
18	RW	0x0	pid18_done_ena PID18 Done Enable 1:enabled 0:disabled
17	RW	0x0	pid17_done_ena PID17 Done Enable
16	RW	0x0	pid16_done_ena PID16 Done Enable 1:enabled 0:disabled
15	RW	0x0	pid15_done_ena PID15 Done Enable 1:enabled 0:disabled
14	RW	0x0	pid14_done_ena PID14 Done Enable 1:enabled 0:disabled
13	RW	0x0	pid13_done_ena PID13 Done Enable 1:enabled 0:disabled
12	RW	0x0	pid12_done_ena PID12 Done Enable 1:enabled 0:disabled
11	RW	0x0	pid11_done_ena PID11 Done Enable 1:enabled 0:disabled
10	RW	0x0	pid10_done_ena PID10 Done Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
9	RW	0x0	pid9_done_ena PID9 Done Enable 1:enabled 0:disabled
8	RW	0x0	pid8_done_ena PID8 Done Enable 1:enabled 0:disabled
7	RW	0x0	pid7_done_ena PID7 Done Enable 1:enabled 0:disabled
6	RW	0x0	pid6_done_ena PID6 Done Enable 1:enabled 0:disabled
5	RW	0x0	pid5_done_ena PID5 Done Enable 1:enabled 0:disabled
4	RW	0x0	pid4_done_ena PID4 Done Enable 1:enabled 0:disabled
3	RW	0x0	pid3_done_ena PID3 Done Enable 1:enabled 0:disabled
2	RW	0x0	pid2_done_ena PID2 Done Enable 1:enabled 0:disabled
1	RW	0x0	pid1_done_ena PID1 Done Enable 1:enabled 0:disabled
0	RW	0x0	pid0_done_ena PID0 Done Enable 1:enabled 0:disabled

TSP_PTIx_PID_INT_ENA1
Address: Operational Base + offset (0x0128)
PID Interrupt Enable Register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	pid63_done PID63 Done Enable 1:enabled 0:disabled
30	RW	0x0	pid62_done PID62 Done Enable 1:enabled 0:disabled
29	RW	0x0	pid61_done PID61 Done Enable 1:enabled 0:disabled
28	RW	0x0	pid60_done PID60 Done Enable 1:enabled 0:disabled
27	RW	0x0	pid59_done PID59 Done Enable 1:enabled 0:disabled
26	RW	0x0	pid58_done PID58 Done Enable 1:enabled 0:disabled
25	RW	0x0	pid57_done PID57 Done Enable 1:enabled 0:disabled
24	RW	0x0	pid56_done PID56 Done Enable 1:enabled 0:disabled
23	RW	0x0	pid55_done PID55 Done Enable 1:enabled 0:disabled
22	RW	0x0	pid54_done PID54 Done Enable 1:enabled 0:disabled
21	RW	0x0	pid53_done PID53 Done Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
20	RW	0x0	pid52_done PID52 Done Enable 1:enabled 0:disabled
19	RW	0x0	pid51_done PID51 Done Enable 1:enabled 0:disabled
18	RW	0x0	pid50_done PID50 Done Enable 1:enabled 0:disabled
17	RW	0x0	pid49_done PID49 Done Enable 1:enabled 0:disabled
16	RW	0x0	pid48_done PID48 Done Enable 1:enabled 0:disabled
15	RW	0x0	pid47_done PID47 Done Enable 1:enabled 0:disabled
14	RW	0x0	pid46_done PID46 Done Enable 1:enabled 0:disabled
13	RW	0x0	pid45_done PID45 Done Enable 1:enabled 0:disabled
12	RW	0x0	pid44_done PID44 Done Enable 1:enabled 0:disabled
11	RW	0x0	pid43_done PID43 Done Enable 1:enabled 0:disabled
10	RW	0x0	pid42_done PID42 Done Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
9	RW	0x0	pid41_done PID41 Done Enable 1:enabled 0:disabled
8	RW	0x0	pid40_done PID40 Done Enable 1:enabled 0:disabled
7	RW	0x0	pid39_done PID39 Done Enable 1:enabled 0:disabled
6	RW	0x0	pid38_done PID38 Done Enable 1:enabled 0:disabled
5	RW	0x0	pid37_done PID37 Done Enable 1:enabled 0:disabled
4	RW	0x0	pid36_done PID36 Done Enable 1:enabled 0:disabled
3	RW	0x0	pid35_done PID35 Done Enable 1:enabled 0:disabled
2	RW	0x0	pid34_done PID34 Done Enable 1:enabled 0:disabled
1	RW	0x0	pid33_done PID33 Done Enable 1:enabled 0:disabled
0	RW	0x0	pid32_done PID32 Done Enable 1:enabled 0:disabled

TSP_PTIx_PID_INT_ENA2
Address: Operational Base + offset (0x012c)
PID Interrupt Enable Register 2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_error PID31 Error Interrupt Enable 1:enabled 0:disabled
30	RW	0x0	pid30_error PID30 Error Interrupt Enable 1:enabled 0:disabled
29	RW	0x0	pid29_error PID29 Error Interrupt Enable 1:enabled 0:disabled
28	RW	0x0	pid28_error PID28 Error Interrupt Enable 1:enabled 0:disabled
27	RW	0x0	pid27_error PID27 Error Interrupt Enable 1:enabled 0:disabled
26	RW	0x0	pid26_error PID26 Error Interrupt Enable 1:enabled 0:disabled
25	RW	0x0	pid25_error PID25 Error Interrupt Enable 1:enabled 0:disabled
24	RW	0x0	pid24_error PID24 Error Interrupt Enable 1:enabled 0:disabled
23	RW	0x0	pid23_error PID23 Error Interrupt Enable 1:enabled 0:disabled
22	RW	0x0	pid22_error PID22 Error Interrupt Enable 1:enabled 0:disabled
21	RW	0x0	pid21_error PID21 Error Interrupt Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
20	RW	0x0	pid20_error PID20 Error Interrupt Enable 1:enabled 0:disabled
19	RW	0x0	pid19_error PID19 Error Interrupt Enable 1:enabled 0:disabled
18	RW	0x0	pid18_error PID18 Error Interrupt Enable 1:enabled 0:disabled
17	RW	0x0	pid17_error PID17 Error Interrupt Enable 1:enabled 0:disabled
16	RW	0x0	pid16_error PID16 Error Interrupt Enable 1:enabled 0:disabled
15	RW	0x0	pid15_error PID15 Error Interrupt Enable 1:enabled 0:disabled
14	RW	0x0	pid14_error PID14 Error Interrupt Enable 1:enabled 0:disabled
13	RW	0x0	pid13_error PID13 Error Interrupt Enable 1:enabled 0:disabled
12	RW	0x0	pid12_error PID12 Error Interrupt Enable 1:enabled 0:disabled
11	RW	0x0	pid11_error PID11 Error Interrupt Enable 1:enabled 0:disabled
10	RW	0x0	pid10_error PID10 Error Interrupt Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
9	RW	0x0	pid9_error PID9 Error Interrupt Enable 1:enabled 0:disabled
8	RW	0x0	pid8_error PID8 Error Interrupt Enable 1:enabled 0:disabled
7	RW	0x0	pid7_error PID7 Error Interrupt Enable 1:enabled 0:disabled
6	RW	0x0	pid6_error PID6 Error Interrupt Enable 1:enabled 0:disabled
5	RW	0x0	pid5_error PID5 Error Interrupt Enable 1:enabled 0:disabled
4	RW	0x0	pid4_error PID4 Error Interrupt Enable 1:enabled 0:disabled
3	RW	0x0	pid3_error PID3 Error Interrupt Enable 1:enabled 0:disabled
2	RW	0x0	pid2_error PID2 Error Interrupt Enable 1:enabled 0:disabled
1	RW	0x0	pid1_error PID1 Error Interrupt Enable 1:enabled 0:disabled
0	RW	0x0	pid0_error PID0 Error Interrupt Enable 1:enabled 0:disabled

TSP_PTIx_PID_INT_ENA3
Address: Operational Base + offset (0x0130)
PID Interrupt Enable Register 3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	pid63_error PID63 Error Interrupt Enable 1:enabled 0:disabled
30	RW	0x0	pid62_error PID62 Error Interrupt Enable 1:enabled 0:disabled
29	RW	0x0	pid61_error PID61 Error Interrupt Enable 1:enabled 0:disabled
28	RW	0x0	pid60_error PID60 Error Interrupt Enable 1:enabled 0:disabled
27	RW	0x0	pid59_error PID59 Error Interrupt Enable 1:enabled 0:disabled
26	RW	0x0	pid58_error PID58 Error Interrupt Enable 1:enabled 0:disabled
25	RW	0x0	pid57_error PID57 Error Interrupt Enable 1:enabled 0:disabled
24	RW	0x0	pid56_error PID56 Error Interrupt Enable 1:enabled 0:disabled
23	RW	0x0	pid55_error PID55 Error Interrupt Enable 1:enabled 0:disabled
22	RW	0x0	pid54_error PID54 Error Interrupt Enable 1:enabled 0:disabled
21	RW	0x0	pid53_error PID53 Error Interrupt Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
20	RW	0x0	pid52_error PID52 Error Interrupt Enable 1:enabled 0:disabled
19	RW	0x0	pid51_error PID51 Error Interrupt Enable 1:enabled 0:disabled
18	RW	0x0	pid50_error PID50 Error Interrupt Enable 1:enabled 0:disabled
17	RW	0x0	pid49_error PID49 Error Interrupt Enable 1:enabled 0:disabled
16	RW	0x0	pid48_error PID48 Error Interrupt Enable 1:enabled 0:disabled
15	RW	0x0	pid47_error PID47 Error Interrupt Enable 1:enabled 0:disabled
14	RW	0x0	pid46_error PID46 Error Interrupt Enable 1:enabled 0:disabled
13	RW	0x0	pid45_error PID45 Error Interrupt Enable 1:enabled 0:disabled
12	RW	0x0	pid44_error PID44 Error Interrupt Enable 1:enabled 0:disabled
11	RW	0x0	pid43_error PID43 Error Interrupt Enable 1:enabled 0:disabled
10	RW	0x0	pid42_error PID42 Error Interrupt Enable 1:enabled 0:disabled

Bit	Attr	Reset Value	Description
9	RW	0x0	pid41_error PID41 Error Interrupt Enable 1:enabled 0:disabled
8	RW	0x0	pid40_error PID40 Error Interrupt Enable 1:enabled 0:disabled
7	RW	0x0	pid39_error PID39 Error Interrupt Enable 1:enabled 0:disabled
6	RW	0x0	pid38_error PID38 Error Interrupt Enable 1:enabled 0:disabled
5	RW	0x0	pid37_error PID37 Error Interrupt Enable 1:enabled 0:disabled
4	RW	0x0	pid36_error PID36 Error Interrupt Enable 1:enabled 0:disabled
3	RW	0x0	pid35_error PID35 Error Interrupt Enable 1:enabled 0:disabled
2	RW	0x0	pid34_error PID34 Error Interrupt Enable 1:enabled 0:disabled
1	RW	0x0	pid33_error PID33 Error Interrupt Enable 1:enabled 0:disabled
0	RW	0x0	pid32_error PID32 Error Interrupt Enable 1:enabled 0:disabled

TSP_PTIx_PCR_INT_STS
Address: Operational Base + offset (0x0134)
PTI PCR Interrupt Status Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	W1C	0x0	pcr7_done PCR7 Status 1: done; 0: not done;
6	W1C	0x0	pcr6_done PCR6 Status 1: done; 0: not done;
5	W1C	0x0	pcr5_done PCR5 Status 1: done; 0: not done;
4	W1C	0x0	pcr4_done PCR4 Status 1: done; 0: not done;
3	W1C	0x0	pcr3_done PCR3 Status 1: done; 0: not done;
2	W1C	0x0	pcr2_done PCR2 Status 1: done; 0: not done;
1	W1C	0x0	pcr1_done PCR1 Status 1: done; 0: not done;
0	W1C	0x0	pcr0_done PCR0 Status 1: done; 0: not done;

TSP_PTIx_PCR_INT_ENA
Address: Operational Base + offset (0x0138)
PTI PCR Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	pcr7_done_ena pcr7 done interrupt enable 1: enabled; 0: disabled;

Bit	Attr	Reset Value	Description
6	RW	0x0	pcr6_done_ena pcr6 done interrupt enable 1: enabled; 0: disabled;
5	RW	0x0	pcr5_done_ena pcr5 done interrupt enable 1: enabled; 0: disabled;
4	RW	0x0	pcr4_done_ena pcr4 done interrupt enable 1: enabled; 0: disabled;
3	RW	0x0	pcr3_done_ena pcr3 done interrupt enable 1: enabled; 0: disabled;
2	RW	0x0	pcr2_done_ena pcr2 done interrupt enable 1: enabled; 0: disabled;
1	RW	0x0	pcr1_done_ena pcr1 done interrupt enable 1: enabled; 0: disabled;
0	RW	0x0	pcr0_done_ena pcr0 done interrupt enable 1: enabled; 0: disabled;

TSP_PTIx_PCRn_CTRL
Address: Operational Base + offset (0x013c)
PID PCR Control Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:1	RW	0x0000	pid PCR Extraction PID number This 13-bit field sets the PID number that needs PCR extraction.
0	RW	0x0	on PCR Extraction Switch 1'b1: PCR extraction switched on ; 1'b0: PCR extraction switched off ;

TSP_PTIx_PCRn_H
Address: Operational Base + offset (0x015c)

High Order PCR value

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	pcr PCR[32] pcr[32]

TSP_PTIx_PCRn_L
Address: Operational Base + offset (0x0160)
Low Order PCR value

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pcr pcr[31:0] pcr[31:0]

TSP_PTIx_DMA_STS
Address: Operational Base + offset (0x019c)
LLP DMA Interrupt Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	W1C	0x0	llp_error LLP DMA Error Status 1: error response during DMA transaction; 0: no error response during DMA transaction;
0	W1C	0x0	llp_done LLP DMA Done Status 1: DMA transaction completed; 0: DMA transaction not completed;

TSP_PTIx_DMA_ENA
Address: Operational Base + offset (0x01a0)
DMA Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	llp_error_ena LLP DMA Error Interrupt Enable 1: enabled 0: disabled
0	RW	0x0	llp_done_ena LLP DMA Done Interrupt Enable 1: enabled 0: disabled

TSP_PTIx_DATA_FLAG0
Address: Operational Base + offset (0x01a4)
PTI_PID_WRITE Flag 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data_write_flag_0 From PID0 TO PID31

TSP_PTIx_DATA_FLAG1
Address: Operational Base + offset (0x01a8)
PTI_PID_WRITE Flag 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data_write_flag_1 From PID32 TO PID63

TSP_PTIx_LIST_FLAG
Address: Operational Base + offset (0x01ac)
PTIx_LIST_WRITE Flag

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	list_write_flag From PID0 TO PID15

TSP_PTIx_DST_STS0
Address: Operational Base + offset (0x01b0)
PTI Destination Status Register

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	demux_dma_status_0 From 0 to 31 channel

TSP_PTIx_DST_STS1
Address: Operational Base + offset (0x01b4)
PTI Destination Status Register

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	demux_dma_status_0 From 32 to 63 channel

TSP_PTIx_DST_ENA0
Address: Operational Base + offset (0x01b8)
PTI Destination Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	demux_dma_enable_0 From 0 to 31 channel

TSP_PTIx_DST_ENA1
Address: Operational Base + offset (0x01bc)
PTI Destination Interrupt Enable Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	demux_dma_enable_1 From 32 to 63 channel

TSP_PTIx_ECWn_H
Address: Operational Base + offset (0x0200)
The Even Control Word High Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ecw_h The Even Control Word High Order ECW[63:32]

TSP_PTIx_ECWn_L
Address: Operational Base + offset (0x0204)
The Even Control Word Low Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ecw_l The Even Control Word Low Order ECW[31:0]

TSP_PTIx_OCWn_H
Address: Operational Base + offset (0x0208)
The Odd Control Word High Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ocw_h The Odd Control Word High order OCW[63:32]

TSP_PTIx_OCWn_L
Address: Operational Base + offset (0x020c)
The Odd Control Word Low Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ocw_l The Odd Control Word Low Order OCW[31:0]

TSP_PTIx_PIDn_CTRL
Address: Operational Base + offset (0x0300)
PID Channel Control Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x0	cw_num Control Word Order Number This fields indicates the corresponding order number of control word to be used to descramble TS packets.
15:3	RW	0x0000	pid PID number This 13-bit sets the desired PID number to be processed by PTI channel.
2	RW	0x0	csa_on Descrambling Switch 1'b1: Descrambling function turned on; 1'b0: Descrambling function turned off;
1	R/WSC	0x0	clear PID Channel Clear Write 1 to clear PID channel. This bit will be set to 0 if the channel is clear.
0	R/WSC	0x0	en PID Channel Enable Write 1 to enable channel. Write 0 to this bit will not take any effect. This bit will be 0 when channel is cleared.

TSP_PTIx_PIDn_BASE
Address: Operational Base + offset (0x0400)
PTI Data Memory Buffer Base Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Base Address PTI Data Memory Buffer Base Address

TSP_PTIx_PIDn_TOP
Address: Operational Base + offset (0x0404)
PTI Data Memory Buffer Top Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Top Address PTI Data Memory Buffer Top Address

TSP_PTIx_PIDn_WRITE
Address: Operational Base + offset (0x0408)
PTI Data Memory Buffer Hardware Writing Address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	address PTI Data Memory Buffer Hardware Writing Address PTI Data Memory Buffer Hardware Writing Address

TSP_PTIx_PIDn_READ
Address: Operational Base + offset (0x040c)
PTI Data Memory Buffer Software Reading Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Software Reading Address PTI Data Memory Buffer Software Reading Address

TSP_PTIx_LISTn_BASE
Address: Operational Base + offset (0x0800)
PTI List Memory Buffer Base Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Software Reading Address PTI Data Memory Buffer Software Reading Address

TSP_PTIx_LISTn_TOP
Address: Operational Base + offset (0x0804)
PTI List Memory Buffer Top Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI List Memory Buffer Top Address PTI List Memory Buffer Top Address

TSP_PTIx_LISTn_WRITE
Address: Operational Base + offset (0x0808)
PTI List Memory Buffer Hardware Writing Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI List Memory Buffer Hardware Writing Address PTI List Memory Buffer Hardware Writing Address

TSP_PTIx_LISTn_READ
Address: Operational Base + offset (0x080c)
PTI List Memory Buffer Software Reading Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI List Memory Buffer Software Reading Address PTI List Memory Buffer Software Reading Address

TSP_PTIx_PIDn_CFG
Address: Operational Base + offset (0x0900)
PID Demux Configure Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	filter_en Filter Byte Enable The proper position of filter byte Enable. For Section filter. the 1st,4th,5th,..18th byte of section header are used to be filtered; For PES filter, the 4th,7th,8th...21th byte of pes header are used to be filtered.
15:12	RO	0x0	reserved
11	RW	0x0	scd_en Start Code Detection Switch Start code detection 1: enabled; 0: disabled; This bit is only valid when n < 16.
10	RW	0x0	cni_on Current Next Indicator Abort when current_next_indicator == 1'b1, 1'b1: abort ; 1'b0: do nothing ;
9:8	RW	0x0	filt_mode Section Filter Mode Filter Mode when the filter mode is configured as section filter. 2'b00: stop per unit; 2'b01: full stop; 2'b10: recycle, update when version number change 2'b11: reserverd

Bit	Attr	Reset Value	Description
7:6	RW	0x0	video_type Video filtering Type 2'b00: MPEG2 2'b01: H264 2'b10: VC-1 2'b11: Reserved
5:4	RW	0x0	filt_type Filter Type 2'b00: section filtering; 2'b01: pes filtering; 2'b10: es filtering; 2'b11: ts filtering; if n>=16, it is reserved as only section filtering, other values are invalid.
3	RW	0x1	cc_abort Continue Counter Error Abort when continuity counter error happens: 1: abort; 0: do nothing;
2	RW	0x0	tei_abort Ts_error_indicator Abort when ts_error_indicator == 1: 1'b1: abort ; 1'b0: do nothing;
1	RW	0x0	crc_abort CRC Error Abort This bit is valid only when crc_on == 1'b1. When crc error happens, 1'b1: abort ; 1'b0: do nothing.
0	RW	0x0	crc_on CRC Check 1'b1: CRC check function turned on 1'b0: CRC check function turned off

TSP_PTIx_PIDn_FILT_0
Address: Operational Base + offset (0x0904)
Fliter Word 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 6th byte of section header or 9th byte of pes header

Bit	Attr	Reset Value	Description
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 5th byte of section header or 8th byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 4th byte of section header or 7th byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 1st byte of section header or 4th byte of pes header

TSP_PTIx_PIDn_FILT_1
Address: Operational Base + offset (0x0908)
Fliter Word 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 10th byte of section header or 13rd byte of pes header
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 9th byte of section header or 12nd byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 8th byte of section header or 11st byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 7th byte of section header or 10th byte of pes header

TSP_PTIx_PIDn_FILT_2
Address: Operational Base + offset (0x090c)
Fliter Word 2

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 14th byte of section header or 17th byte of pes header

Bit	Attr	Reset Value	Description
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 13rd byte of section header or 16th byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 12nd byte of section header or 15th byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 11st byte of section header or 14th byte of pes header

TSP_PTIx_PIDn_FILT_3
Address: Operational Base + offset (0x0910)
Fliter Word 3

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 18th byte of section header or 21st byte of pes header
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 17th byte of section header or 20th byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 16th byte of section header or 19th byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 15th byte of section header or 18th byte of pes header

18.5 Interface Description

Table 18-1 TSP Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
ts_data0	I/O	IO_UART1BBsin_TS0data0_BBgpio5b0	GPIO5B_IOMUX[1:0]= 2'b10
ts_data1	I/O	IO_UART1BBsout_TS0data1_BBgpio5b1	GPIO5B_IOMUX[3:2]= 2'b10
ts_data2	I/O	IO_UART1BBctsn_TS0data2_BBgpio5b2	GPIO5B_IOMUX[5:4]= 2'b10
ts_data3	I/O	IO_UART1BBrtsn_TS0data3_BBgpio5b3	GPIO5B_IOMUX[7:6]= 2'b10
ts_data4	I/O	IO_SPI0clk_TS0data4_UART4EXPctsn_BBgpio5b4	GPIO5B_IOMUX[9:8]= 2'b10

Module Pin	IO	Pad Name	IOMUX Setting
ts_data5	I/O	IO_SPI0csn0_TS0data5_UART4EXPrtsn_BBgpio5b5	GPIO5C_IOMUX[11:10]= 2'b10
ts_data6	I/O	IO_SPI0txd_TS0data6_UART4EXPsout_BBgpio5b6	GPIO5B_IOMUX[13:12]= 2'b10
ts_data7	I/O	IO_SPI0rxd_TS0data7_UART4EXPsin_BBgpio5b7	GPIO5B_IOMUX[15:14]= 2'b10
ts_valid	I/O	IO_TS0valid_BBgpio5c1	GPIO5C_IOMUX[2]= 1'b1
ts_sync	I/O	IO_SPI0csn1_TS0sync_BBgpio5c0	GPIO5C_IOMUX[1:0]= 2'b10
ts_err	I/O	IO_TS0err_BBgpio5c3	GPIO5C_IOMUX[6]= 1'b1
ts_clk	I/O	IO_TS0clk_BBgpio5c2	GPIO5C_IOMUX[4]= 1'b1
hsadc_data0	I	IO_CIFdata2_HOSTdin0_HSADCdata0_DVPgpio2a0	GPIO2A_IOMUX[1:0]= 2'b11
hsadc_data1	I	IO_CIFdata3_HOSTdin1_HSADCdata1_DVPgpio2a1	GPIO2A_IOMUX[3:2]= 2'b11
hsadc_data2	I	IO_CIFdata4_HOSTdin2_HSADCdata2_DVPgpio2a2	GPIO2A_IOMUX[5:4]= 2'b11
hsadc_data3	I	IO_CIFdata5_HOSTdin3_HSADCdata3_DVPgpio2a3	GPIO2A_IOMUX[7:6]= 2'b11
hsadc_data4	I	IO_CIFdata6_HOSTckinp_HSADCdata4_DVPgpio2a4	GPIO2A_IOMUX[9:8]= 2'b11
hsadc_data5	I	IO_CIFdata7_HOSTckinn_HSADCdata5_DVPgpio2a5	GPIO2A_IOMUX[11:10]= 2'b11
hsadc_data6	I	IO_CIFdata8_HOSTdin4_HSADCdata6_DVPgpio2a6	GPIO2A_IOMUX[13:12]= 2'b11
hsadc_data7	I	IO_CIFdata9_HOSTdin5_HSADCdata7_DVPgpio2a7	GPIO2A_IOMUX[15:14]= 2'b11
hsadc_valid	I	IO_CIFhref_HOSTdin7_HSADCTSvalid_DVPgpio2b1	GPIO2B_IOMUX[3:2]= 2'b11
hsadc_sync	I	IO_CIFvsync_HOSTdin6_HSADCTSsync_DVPgpio2b0	GPIO2B_IOMUX[1:0]= 2'b11
hsadc_err	I	IO_CIFclkout_HOSTwkreq_HSADCTSfail_DVPgpio2b3	GPIO2B_IOMUX[7:6]= 2'b01
gps_clk	I	IO_CIFclkin_HOSTwkack_GPSclk_HSADCclkout_DVPgpio2b2	GPIO2B_IOMUX[5:4]= 2'b11
gpst1_clk	I	IO_UART3GPSctsn_GPSrfclk_GPST1clk_GPIO30gpio7b1	GPIO7B_IOMUX[3:2]= 2'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

18.6 Application Notes

18.6.1 Overall Operation Sequence

- Enable desired modules to work by writing correspond bit with '1' in TSP_GCFG. Note: it is important to do this step at first, otherwise writing the corresponding registers will not take effect.
- Set up TS configuration by writing corresponding registers.
- Wait for the interrupts to pick up the desired TS packets following the rules detailed in the following section.

Note: PTI1 addr = PTI0 addr + 0x1000;

18.6.2 TS Source

TS source can be chosen by writing the bit 9 of TSP_PTIx_CTRL(x=0,1), '1' for demodulator, '0' for local memory.

1.TS_IN Interface

Writing bit 10 of TSP_PTIx_CTRL to choose bit ordering, and writing bit [12:11] to choose input TS mode.

TS_IN interface supports 4 input TS stream mode: sync/valid serial mode, sync/valid parallel mode, sync/burst parallel mode, nosync/valid parallel mode.

2.Local Memory

PTI also can process the TS data read from local memory by using LLP DMA mode.
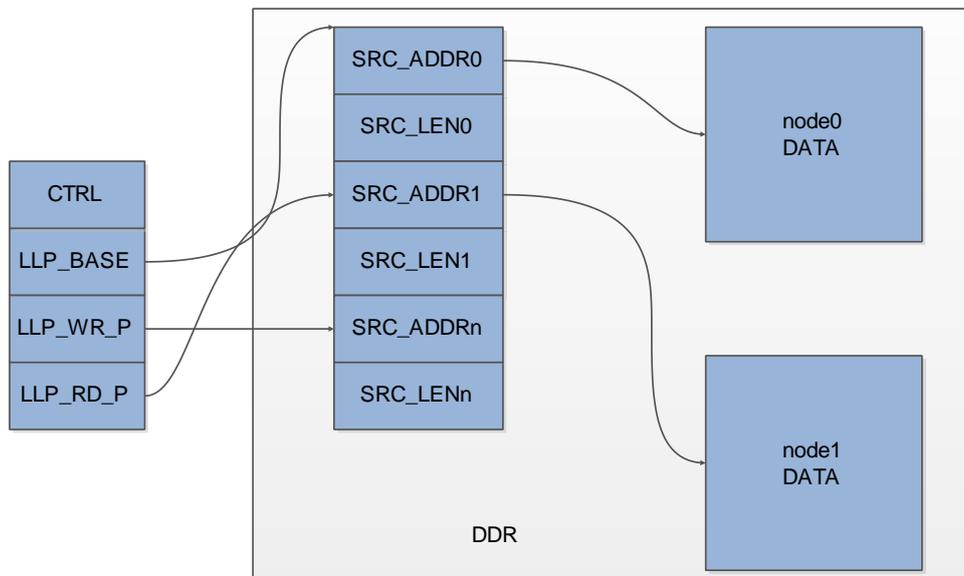
(1) Write PTIx_LLP_BASE with the list base address;

(2) Starting from the list base address, write the list nodes. One list node comprised of two words. The first word describes the TS data base address, the second one describes the length of TS data in unit of word.

(3) Write the PTIx_LLP_WRITE with the number of words that you have written in list memory. Note it is not the number of LLP nodes, so that the number you are writing should be an even one.

(4) Write PTIx_LLP_CFG with the configuration you want. Write the bit 0 with 1 to start LLP DMA. If all the list nodes are written, don't forget to write 1 to bit 3 to tell DMAC that the configuration is finished.

Note:

- *The MSB(bit7) of the 8-bit pointer in the PTIx_LLP_Write and PTIx_LLP_Read is used as the flag bit, and remaining 7 bits are used for addressing. Therefore the the pointer is referred to 7-bit space, not 8-bit space, and remember write the pointer with the correct flag bit. For example, if you have configured 63 LLP nodes and then you have to write the 64th LLP node starting from the list base address,*
- *PTIx_LLP_READ informs that how many words has been processed by LLP DMA. An interrupt may be generated when number of the processed words has reach to the threshold set in the PTIx_LLP_CFG.*
- *If you write the PTIx_LLP_Write several times in a complete DMA transaction, it is important to notice the flag bit of PTIx_LLP_Write, and never make the writing pointer catch up with the reading pointer.*

18.6.3 TS Synchronous Operation

Synchronous mode and Bypass mode can be switched by writing bit 15 of TSP_PTIx_CTRL. In the synchronous mode, 188/192/204 byte TS packets are supported and self-adjusted. Set up locked times in TSP_PTIx_CTRL to inform the successive times of TS packet header detection needs to lock the header of TS packets when in the unlocked mode, and set up unlocked times to informs the successive times of TS packet header error needs to re-lock header of TS packets in the locked mode. It is recommended to use 2-3 as the locked times to quickly and correctly locked the header, and 2-3 as unlocked times to avoid unnecessarily entering into unlocked searching mode.

In the bypass mode, the input TS data will not be re-synchronized and directly fed into the PTI channel.

18.6.4 Descrambling Operation

Descrambler can achieve PES or TS level descrambling which conforms to the CSA v2.0.

■ Enable the channel you want by writing 1 to bit 0 of TSP_PTIx_PIDn_CTRL (x=0~1, n= 0~64);

■ Set the desired PID number

■ Turn on descrambling function by setting 1 to bit 2. If the corresponding CW is available or TS is required to be left undescrambled, CSA_ON bit is set to 0;

■   Choose corresponding Control Word by setting bit[19:16], and 16 set Control Word are available to be chosen. Don't forget Control Word should be preprared before the descrambling function is enabled.

Note: If the enabled channel is needed to be disabled, write the CLEAR bit to disabled the channel rather than write '0' to EN bit.

18.6.5 Demux Operation

Refer to TSP_PTIx_PIDn_CFG for Demux operation. The software users should be familiar with the demux knowledge.

Users should create a separate memory buffer to receive the processed data for each desired PID channel, and write the base and top address information of the memory buffer into TSP_PTIx_PIDn_BASE and TSP_PTIx_PIDn respectively. Also initial writing address and reading address, normally the same as base address, are also needed to be written into TSP_PTIx_PIDn_WRITE and TSP_PTIx_PIDn_READ respectively. For ES/PES filter, another separate memory needs to be created to store list data, which is used to assist obtaining PES/ES data. List base address, top address, initial writing address and reading address are also needed to write into corresponding registers.

Note:
  1. For channel whose PID channel number larger than 15, the channels can only be used section filter. For others, there is no such limit. They can be configured as section filter, pes filter, es filter or ts filter.
  2. Data memory address boundary should be aligned with word-size, and list memory address boundary should be aligned with word size. If the memory buffer is not larger to store processed data so that writing address reaches the top address, TSP will return to the base address to write data. So fetch the data in time, don't make the writing address catches up with reading address. The list memory buffer has the same issue.

1.Demux data obtain

●   **TS filter**

To obtain TS data and section data, when an desired PID done interrupt is generated, read TSP_PTIx_PIDn_READ firstly to know the address that last reading stops, and then read TSP_PTIx_PIDn_WRITE to know the address that hardware has reached. For ts data, start from the TSP_PTIx_PIDn_READ address to get the TS packet data, and stop at the address you want. However, the ending address should not catch up with writing address. It is recommended to obtain the TS data in the unit of TS packet which is 47-word size. At last, don't forget to write the ending address into TSP_PTIx_PIDn_READ to leave a hint where current reading stops.

B. Section filter

Section filter can run three mode to meet different needs: stop-per-unit; full stop; recycle , update when version number change. The PID done interrupt will be generated after each part of a complete section is processed in the first mode, and the PID done will be generated only after the whole section is completed in the last two modes. In the frist two mode, the PID channel will be disabled after the whole section is completed. In the recycle mode, the channel will remain active and start a new section processing when the version number changes. Section filter also supports 16-byte filtering function, which can assign 1st , 4th to 18th byte to be filtered.

The process to obtain section data is similar to the process for TS data. After a PID done interrupt done is generated, refer to the corresponding PID error status register to check if the section data is correct. Read the frist word of the section start address to know the total length of the section according to the format of section data.

   Section Length = {First Word[11:8], First Word[23:16]};
   Total Length = Section Length;

Then start to fetch section data according to the total length. Again don't forget to write the stopped address.

C. PES/ES filter

PES filter supports 16-byte filtering function, which can assign 4th, 7th to 21st byte to be filtered. ES filter supports start code detection, including MPEG2 start code 0x000001b3, 0x00000100, VC-1 start code 0x0000010d, 0x000010f, H264 start code 0x00001.

To obtain the pes/es data, the assistant of list descriptor is needed.
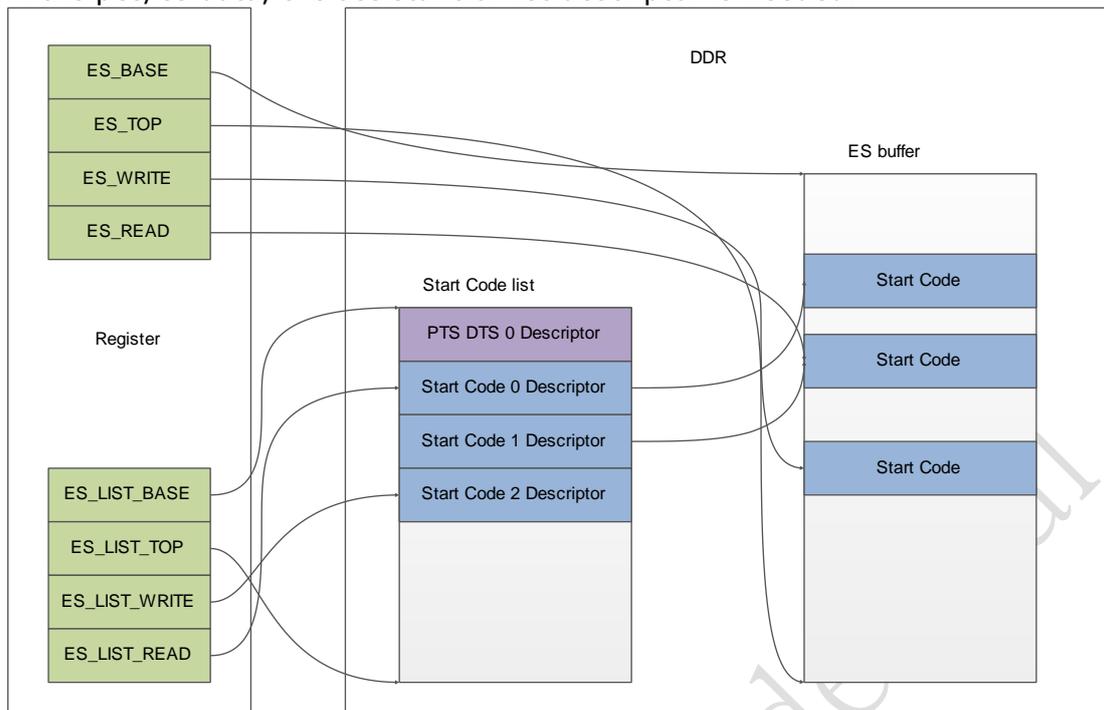
List memory buffer contains descriptors which contains information to obtain es/pes data which are stored in data memory buffer.

The descriptor stored in list memory buffer can be separated into two groups: PTS_DTS Descriptor and Start Code Descriptor. The descriptor is composed by 4 word content, word_0, word_1, word_2 and word_3. The word_x (x means the sequence number in a descriptor, and they are stored in the memory in sequence order). The format of the 4 words are listed as follows:

(1) start code descriptor
Word_0:

Word_0[29:28] indicates the attributes of the bytes of the pointed word. 2'b00 means the whole word belongs to the new ES/PES packet; 2'b01 means that word[7:0] belongs to the previous packet, and the remaining bytes belong to the new packet; 2'b10 means means that word[15:0] belongs to the previous packet, and the remaining bytes belong to the new packet; 2'b11 means 'b10 means means that word[23:0] belongs to the previous packet, and the remaining bytes belong to the new packet. This pointed word is the word where start code starts, word_2 describes the location of start code.

Word_0[27:24] is equal to 0x0 in the start code descriptor. Users can used to tell two kinds of descriptor.

If the video type is H.264, word_0[23:8] means first_mb_in slice, and word_0 means nal_nuit_type.

Word_1:

the start code of stream.

Word_2:

DDR offset address in the DDR of the word where the start code is located.

Word_3:

0x0

(2) PTS_DTS Descriptor

Word_0:

Word_0[29:28]: the same as start code descriptor
Word_0[27:24]: 0x1 in PTS_DTS descriptor.
Word_0[3]   : PTS[32];
Word_0[2]   : DTS[32];
Word_0[1:0]   : pts_dts_flag;

Word_1:
DDR offset address of the word that valid data starts.

Word_2:
PTS[31:0]

Word_3
DTS[31:0]

To obtain PES data or ES data when start code detection is disabled, use PTS_DTS descriptor. To obtain ES data when start code detection is enabled, use start code descriptor.
When a PID done interrupt is generated, make sure there is no corresponding PID error generated. Read the TSP_PTIx_LISTn_READ to know the list reading address in the last time. Start from here, read the 4-word descriptor one by one to know the offset of the packets. Refer to the offset in the DDR where in the data memory buffer to obtain data.   Finally write TSP_PTIx_LISTn_READ and TSP_PTIx_PIDn_READ with corresponding reading address.

18.6.6 TS Out Interface

All the configuration is done by writing TSP_TSOUT_CTRL. Before programming this register, make sure that you have enabled the TS OUT interface. If you want to disable TS out interface, write '0' to the START bit(bit 0) of TSP_TSOUT_CTRL, and then disable it in the TSP_GFCG.
Each PTI channel can provide TS out interface with PID-filtering TS Packets or non-PID-filtering TS packets, and therefore there are totally 4 sources can be chosen for TS out interface.

18.6.7 PVR

PVR module provide you with the function to record the programs you want. The 4 sources can be assigned with PVR, and they are the same as TS out interface.
Assign the PVR length and PVR address, and then configure TSP_PVR_CTRL to start PVR module. If you want to stop PVR function during recording, write '1' to STOP bit (bit 0) to to TSP_PVR_CTRL to stop it. Remember to take care of the status of PVR_ON bit of TSP_GFCG when programming the PVR-related registers.

18.6.8 PCR extraction

PCR extraction can be enabled by configure PTIx_PCRn_CTRL. Then if the PID-matched TS data contain PCR field, the 33-bit PCR_base field will be written corresponding PTIx_PCRn_H and PTIx_PCRn_L registers. An interrupt will be asserted if PCR interrupt is enabled.