Rockchip
RK3288
Technical Reference Manual

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Revision 1.0
Jun. 2015

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Revision History

Date	Revision	Description
2015-6-26	1.0	Update-Part1 System and System control
2014-10-22	0.7	Modify some chapters
2014-09-23	0.6	Modify some chapters
2014-09-04	0.5	Modify some chapters
2014-08-27	0.4	Modify some chapters
2014-03-18	0.2	Add some chapters
2014-02-25	0.1	Initial Release

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Chapter 1 Introduction

1.1 Overview

RK3288 is a low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A17 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3288 supports almost full-format; include H.265 decoder by 2160p@60fps, H.264 decoder by 2160p@24fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3288 completely compatible with OpenGL ES1.1/2.0/3.0, OpenCL 1.1 and DirectX 11. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3288 has high-performance dual channel external memory interface (DDR3/DDR3L/LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidth, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 MicroProcessor

- Quad-core ARM Cortex-A17 MPCore processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFP v3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the four CPUs
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 1MB unified L2 Cache
- Trustzone technology support
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Six separate power domains for every core to support internal power switch and externally turn on/off based on different application scenario
  - PD_A17_0: 1st Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_A17_1: 2nd Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_A17_2: 3rd Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_A17_3: 4th Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_SCU: SCU + L2 Cache controller, and including PD_A17_0, PD_A17_1, PD_A17_2, PD_A17_3, debug logic
- One isolated voltage domain to support DVFS

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1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
  - Internal SRAM for security and non-security access
- External off-chip memory①
  - Dual channel DDR3/DDR3L
  - Dual channel LPDDR2
  - Dual channel LPDDR3
  - Dual channel async Nand Flash(include LBA Nand)
  - Single channel async Nand Flash(include LBA Nand)
  - Dual channel sync ONFI/toggle Nand Flash

1.2.3 Internal Memory

- Internal BootRom
  - Size : 20KB
  - Support system boot from the following device :
    - 8bits Async Nand Flash
    - 8bits Toggle Nand Flash
    - SPI interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
- Internal SRAM
  - Size : 100KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB, … up to 96KB by 4KB step

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3-1333/DDR3L-1333/LPDDR2-800/LPDDR3-1066)
  - Compatible with JEDEC standard DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
  - Support 2 channel, each channel 16 or 32bits data widths
  - Support up to 2 ranks (chip selects) for each channel, totally 4GB(max) address space, maximum address space for one rank of channel 0 is also 4GB, which is software-configurable.
  - 16bits/32bits data width is software programmable
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/LPDDR2/LPDDR3 SDRAM; clock stop and deep power-down for LPDDR2 SDRAM
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and cke output signals , make SDRAM still in self-refresh state to prevent data missing.

- Nand Flash Interface
  - Support dual channel async Nand Flash, each channel 8bits, up to 4 banks
  - Support dual channel sync DDR Nand Flash, each channel 8bits, up to 4 banks
  - Support LBA Nand Flash in async or sync mode
  - Up to 60bits hardware ECC
  - For Toggle Nand Flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock

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rate is 75MHz
- For async Nand Flash, support configurable interface timing , maximum data rate is 16bit/cycle
- Embedded special DMA interface to do data transfer
- Also support data transfer together with general PERI_DMAC in SoC system

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.5 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.5
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535 Bytes
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3288
  - One oscillator with 24MHz clock input and 5 embedded PLLs
  - Up to 2.2GHz clock output for all PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 4 separate voltage domains
  - 12 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 8 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width

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- Counter clock is from apb bus clock
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Totally 16 defined-ranges of main timeout period

- Interrupt Controller
  - Support 3 PPI interrupt source and 112 SPI interrupt sources input from different components inside RK3288
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ) separatelyfor each Cortex-A17, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , BUS_DMAC is for bus system, PERI_DMAC is for peripheral system
  - BUS_DMAC features:
    - 6 channels totally
    - 6 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register config, designated as secure and non-secure
    - Support trustzone technology and programmable secure state for each DMA channel
  - PERI_DMAC features:
    - 7 channels totally
    - 9 hardware request from peripherals
    - 2 interrupt output
    - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside RK3288
    - Cortex-A17, support security and non-security mode, switch by software
    - BUS_DMAC, support some dedicated channels work only in security mode
    - eFuse, only accessed by Cortex-A17 in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)
  - Embedded encryption and decryption engine
    - Support AES-128/192/256 with ECB, CBC, OFB, CTR, CBC-MAC, CMAC, XCBC-MAC, XTS and CCM modes
    - Supports the DES (ECB and CBC modes) and TDES (EDE and DED) algorithms

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- Supports SHA-1, SHA-256 and SHA-512 modes, as well as HMAC
- Support all mathematical operations required to implement the PKA supported cryptosystems between 128 bits and 3136 bits in size (in steps of 32 bits)
- Support random bits generator from the ring oscillator
- Controll the AIB interface to the OTP memory and providing an interface for the CPU to access to the non-confidential trusted data
- Set the device's security lifecycle state according to the values of various flag words in the OTP memory
- Provide an firmware interface for secure boot, secure debug
- Provide a security processor sub-system based on an internal 32-bit CPU

- Support security boot
- Support security debug

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Embedded memory management unit(MMU)
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, AVS, VC-1, VP8, MVC
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 5.2 : 2160p@24fps (3840x2160)③
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 2160p@24fps (3840x2160)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - VP8 : 2160p@24fps (3840x2160)
  - AVS : 1080p@60fps (1920x1088)
  - MVC : 2160p@24fps (3840x2160)
  - For AVS, 4:4:4 sampling not supported
  - For H.264, image cropping not supported
  - For MPEG-4, GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

1.2.7 Video Encoder

- Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
- Only support I and P slices, not B slices
- Support error resilience based on constrained intra prediction and slices
- Input data format:
  - YCbCr 4:2:0 planar
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - CbYCrY 4:2:2 interleaved
  - RGB444 and BGR444
  - RGB555 and BGR555
  - RGB565 and BGR565
  - RGB888 and BRG888
  - RGB101010 and BRG101010
- Image size is from 96x96 to 1920x1088(Full HD)
- Maximum frame rate is up to 30fps@1920x1080③
- Bit rate supported is from 10Kbps to 20Mbps

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1.2.8 HEVC Decoder

- Main/Main10 HEVC/H.265 decoder , max to 4k 10bit 60FPS
- Support up to 4096x2304 resolution
- Embedded memory management unit(MMU)
- Stream error detector (28 IDs)
- Internal 128k cache for bandwidth reduction
- Multi-clock domains and auto clock-gating design for power saving

1.2.9 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate④ is up to 76million pixels per second
  - Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate④ up to 90million pixels per second
  - Embedded memory management unit(MMU)

1.2.10 Image Enhancement

- Image pre-processor
  - Only used together with HD video encoder inside RK3288, not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Video stabilization
  - Work in combined mode with HD video encoder inside RK3288 and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image Post-Processor (embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from image data stored in external memory

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- Input data format:
  - Any format generated by video decoder in combined mode
  - YCbCr 4:2:0 semi-planar
  - YCbCr 4:2:0 planar
  - YCbYCr 4:2:2
  - YCrYCb 4:2:2
  - CbYCrY 4:2:2
  - CrYCbY 4:2:2
- Output data format:
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - YCrYCb 4:2:2
  - CbYCrY 4:2:2
  - CrYCbY 4:2:2
  - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
- Input image size:
  - Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode: width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling:
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering) for 4/5/6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha + YUV444, big endian channel order with AYUV8888
  - 8bit alpha + 24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Enhancement-Processor (IEP)
  - Image format
    - Input data: XRGB/RGB565/YUV420/YUV422
    - Output data: ARGB/RGB565/YUV420/YUV422
    - The format ARGB/XRGB/RGB565/YUV support swap
    - Support YUV semi-planar/planar
    - Support BT601_l/BT601_f/BT709_l/BT709_f color space conversion
    - Support RGB dither up/down conversion
    - Support YUV up/down sampling conversion
    - Max source image resolution: 8192x8192
    - Max scaled image resolution: 4096x4096

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- Enhancement
  - Gamma adjustment with programmable mapping table
  - Hue/Saturation/Brightness/Contrast enhancement
  - Color enhancement with programmable coefficient
  - Detail enhancement with filter matrix up to 9x9
  - Edge enhancement with filter matrix up to 9x9
  - Programmable difference table for detail enhancement
  - Programmable distance table for detail and edge enhancement
- Noise reduction
  - Compression noise reduction with filter matrix up to 9x9
  - Programmable difference table for compression noise reduction
  - Programmable distance table for compression noise reduction
  - Spatial sampling noise reduction
  - Temporal sampling noise reduction
  - Optional coefficient for sampling noise reduction
- Scaling
  - Horizontal down-scaling with vertical down-scaling
  - Horizontal down-scaling with vertical up-scaling
  - Horizontal up-scaling with vertical down-scaling
  - Horizontal up-scaling with vertical up-scaling
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Deinterlace
  - Input 4 fields, output 2 frames mode
  - Input 4 fields, output 1 frames mode
  - Input 2 fields, output 1 frames mode
  - Programmable motion detection coefficient
  - Programmable high frequency factor
  - Programmable edge interpolation parameter
  - Source width up to 1920
- Interface
  - Programmable direct path to VOP
- Embedded memory management unit(MMU)

1.2.11 Graphics Engine

- 3D Graphics Engine :
  - ARM Mali-T764 GPU core
  - High performance OpenGL ES1.1/2.0/3.0, OpenCL 1.1, DirectX 11
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 256KB size
  - Image quality using double-precision FP64, and anti-aliasing

- 2D Graphics Engine :
  - BitBlit with Stretch Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4
  - Alpha blending modes including global alpha, per pixel alpha, porter-duff and fading
  - 8K x 8K input and 2K x 2K output raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Blending, scaling and rotation are supported in one pass for Bitbilt
  - Source format:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565

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- RGBA5551, RGBA4444
- YUV420 planar, YUV420 semi-planar
- YUV422 planar, YUV422 semi-planar
- BPP8, BPP4, BPP2, BPP1

- Destination formats:
  - ABGR8888, XBGR888, ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
  - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.2.12 Video IN/OUT

- Camera Interface(DVP interface only)
  - Support up to 5M pixels
  - 8bits BT656(PAL/NTSC) interface
  - 16bits BT601 DDR interface
  - 8bits/10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Camera Interface and Image Processer(Interface and Image Processing)
  - Maximum input resolution of 14M(4416x3312) pixels
  - Main scaler with pixel-accurate up- and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
  - Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
  - support of semiplanar NV21 color storage format
  - support of independent image cropping on main and self path
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable
  - quantization and Huffman tables
  - Windowing and frame synchronization
  - Frame skip support for video (e.g. MPEG-4) encoding
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
  - Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
  - Read port provided to read back a picture from system memory
  - Simultaneous picture read back, resizing and storing through self path while main
  - path captures the camera picture
  - Black level compensation
  - Four channel Lens shade correction (Vignetting)
  - Auto focus measurement
  - White balancing and black level measurement

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- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Global Tone Mapping with wide dynamic range unit (WDR)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction

- Display Interface
  - Embedded two channel display interfaces: VOP_BIG and VOP_LIT.
  - Parallel Display interface
    - Parallel RGB LCD Interface:
      - 30-bit(RGB101010),24-bit(RGB888),18-bit(RGB666), 15-bit(RGB565)
    - Serial RGB LCD Interface(optional):
      - 2x12-bit, 3x8-bit(RGB delta support), 3x8-bit+dummy
    - MCU LCD interface(optional):
      - i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
    - TV Interface: ITU-R BT.656(8-bit, 480i/576i/1080i)
    - DDR output interface:
      - parallel RGB and 2x12-bit serial RGB
      - Single or dual clock out
    - dither down:
      - allegro, FRC
      - gamma after dither
    - Max output resolution: 3840x2160 (for VOP_BIG), 2560x1600 (for VOP_LIT)
    - Scaning timing 8192x4096
  - Display process
    - Background layer:
      - programmable 24-bit color
    - Win0 (Video0) layer:
      - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
      - Support virtual display
      - 1/8 to 8 scaling-down and scaling-up engine:
        - Scale up using bicubic or bilinear;
        - Scale down using bilinear or average;
        - 4 Bicubic tables : precise,spline,catrom,mitchell;
        - coord 8bit, coe 8bit signed
      - x-mirror,y-mirror
    - Win1 (Video1) layer:
      - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
      - Support virtual display
      - 1/8 to 8 scaling-down and scaling-up engine
        - Scale up using bicubic or bilinear;
        - Scale down using bilinear otraverage;
        - 4 Bicubic tables : precise,spline,catrom,mitchell;
        - coord 8bit, coe 8bit signed
      - x-mirror,y-mirror
    - Win2 (UI 0) layer:
      - RGB888, ARGB888, RGB565, 1/2/4/8bpp
      - Support virtual display

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        - 4 display regions
        - x-mirror,y-mirror
    - Win3 (UI 1) layer:
        - RGB888, ARGB888, RGB565, 1/2/4/8bpp
        - Support virtual display
        - 4 display regions
        - x-mirror,y-mirror
    - Hardware cursor:
        - RGB888, ARGB888, RGB565, 1/2/4/8bpp
        - Support two size: 32x32,64x64,or 128x128
    - Overlay:
        - Win0/Win1/Win2/Win3 256 level alpha blending (support pre-multiplied alpha)
        - Win0/Win1/Win2/Win3 overlay position exchangeable
        - Win0/Win1/Win2/Win3 Transparency color key
        - Win0/Win1/Win2/Win3 global/per-pixel alpha
        - HWC 256 level alpha blending
        - HWC global/per-pixel alpha
- Others
    - 3 x 256 x 8 bits display LUTs
    - YcbCr2RGB(rec601-mpeg/rec601-jpeg/rec709/BT2020)and RGB2YcbCr
    - Support BCSH function
    - Support CABC function
    - QoS request signals
    - Gather transfer (Max 8)
    - Y/UV scheduler
    - Addr alignment
    - Support IEP direct path(win0/1/2/3)
    - Embedded memory management unit(MMU)
    - Support MIPI flow control

1.2.13 HDMI

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- For HDMI operation, support for the following:
    - Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
    - 3-D video formats
    - Up to 10-bit Deep Color modes
    - Up to 18 Gbps aggregate bandwidth
    - 13.5–600 MHz input reference clock
    - HPD input analog comparator
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- Support HDCP 1.4

1.2.14 LVDS (RK3288-C has not this function)

- Comply with the TIA/EIA-644-A LVDS standard
- Combine LVTTL IO, support LVDS/LVTTL data output
- Support reference clock frequency range from 10Mhz to 148.5Mhz
- Support LVDS RGB 30/24/18bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, every channel include 5 data lanes and 1 clock lane

1.2.15 MIPI PHY

- Embedded 3 MIPI PHY, MIPI 0 only for TX, MIPI 1 for TX and RX, MIPI 2 only for RX
- Support 4 data lane, providing up to 4Gbps data rate

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- Support 1080p @ 60fps output
- Lane operation ranging from 80 Mbps to 1 Gbps in forward direction

1.2.16 eDP PHY

- Support 4Kx2K @ 30fps
- Compliant with eDPTM Specification, version 1.1
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane(HBR2/HBR/RBR)
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10/12 bit per component video format
- Support VESA DMT and CVT timing standards
- Fully support EIA/CEA-861Dvideo timing and Info Frame structure
- Hot plug and unplug detection and link status monitor
- Support DDC/CI and MCCS command transmission when the monitor includes a display controller.
- Supports Panel Self Refresh(PSR)

1.2.17 Audio Interface

- I2S/PCM with 8ch
  - Up to 8 channels (4xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

1.2.18 Connectivity

- SDIO interface
  - Embedded 2 SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus width

- High-speed ADC stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface

- TS interface
  - Supports two TS input channels and one TS output channel.
  - Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
  - Supports serial and parallel output mode with PCR adjustment, and lsb-msb or msb-lsb bit ordering can be chosen in the serial output mode.
  - Supports 2 TS sources: demodulators and local memory.
  - Supports 2 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
    - 64 PID filters.
    - TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps

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        - 16 PES/ES filters with PTS/DTS extraction and ES start code detection.
        - 4/8 PCR extraction channels
        - 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
        - PID done and error interrupts for each channel
        - PCR/DTS/PTS extraction interrupt for each channel
    - Supports 1 PVR(Personal Video Recording) output channel.
    - 1 built-in multi-channel DMA Controller.

- PS2 interface
    - Support PS/2 data communication protocol
    - Support PS/2 master mode
    - Software programmable timing requirement to support max PS/2 clock frequency to 33KHZ
    - Support status to be queried for data communication error
    - Support interrupt mode for data communication finish
    - Support timeout mechnism for data communication
    - Support interrupt mode for data communication timeout

- Smart Card
    - support card activation and deactivation
    - support cold/warm reset
    - support Answer to Reset (ATR) response reception
    - support T0 for asynchronous half-duplex character transmission
    - support T1 for asynchronous half-duplex block transmission
    - support automatic operating voltage class selection
    - support adjustable clock rate and bit (baud) rate
    - support configurable automatic byte repetition

- Host interface
    - Low Pin Count interface(8 inputs/16 outputs or 16 inputs/8 outputs)
    - No mandatory Tri-State signals
    - All signals driven using source synchrounous clock.(2 DDR clock signals per direction for TX and RX paths)
    - Low latency throught serialization/deserialization
    - Transport clocks and bus clock are independent
    - Support Asymmetric(Host/Peripheral) communication operations
    - Support multiple outstanding transactions Reads,Writes and interrupts
    - Support Mirror Mode to enable self tett with identical device

- GPS Interface
    - Single chip, integrate GPS bb with cpu
    - 32 DMA channels for AHB master access
    - Complete 1-band, C/A, and NMEA-0183 compatibility
    - Support reference frequencies 16.368MHz
    - High sensitivity for indoor fixes
    - Low power consumption
    - Low cost with smaller size
    - Multi modes support both standalone GPS and A_GPS

- GMAC 10/100/1000M Ethernet Controller
    - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
    - Supports 10/100-Mbps data transfer rates with the RMII interfaces
    - Supports both full-duplex and half-duplex operation
        - Supports CSMA/CD Protocol for half-duplex operation
        - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
        - Supports IEEE 802.3x flow control for full-duplex operation

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        - Optional forwarding of received pause control frames to the user application in full-duplex operation
        - Back-pressure support for half-duplex operation
        - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation
    - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
    - Automatic CRC and pad generation controllable on a per-frame basis
    - Options for Automatic Pad/CRC Stripping on receive frames
    - Programmable InterFrameGap (40-96 bit times in steps of 8)
    - Supports a variety of flexible address filtering modes
    - Separate 32-bit status returned for transmission and reception packets
    - Supports IEEE 802.1Q VLAN tag detection for reception frames
    - Support detection of LAN wake-up frames and AMD Magic Packet frames
    - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
    - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams
    - Comprehensive status reporting for normal operation and transfers with errors
    - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
    - Handles automatic retransmission of Collision frames for transmission
    - Discards frames on late collision, excessive collisions, excessive deferral and underrun conditions

- SPI Controller
    - 3 on-chip SPI controller inside RK3288
    - Support serial-master and serial-slave mode, software-configurable
    - DMA-based or interrupt-based operation
    - Embedded two 32x16bits FIFO for TX and RX operation respectively
    - Support 2 chip-selects output in serial-master mode

- Uart Controller
    - 5 on-chip uart controller inside RK3288
    - DMA-based or interrupt-based operation
    - For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
    - Support 5bit,6bit,7bit,8bit serial data transmit or receive
    - Standard asynchronous communication bits such as start,stop and parity
    - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
    - Support non-integer clock divides for baud clock generation
    - Auto flow control mode is for all UART, except UART_DBG

- I2C controller
    - 6 on-chip I2C controller in RK3288
    - Multi-master I2C operation
    - Support 7bits and 10bits address mode
    - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
    - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
    - Totally 160 GPIOs
    - All of GPIOs can be used to generate interrupt to Cortex-A17
    - GPIO0 can be used to wakeup system from low-power mode
    - The pull direction(pullup or pulldown) for all of GPIOs are software-programmable

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- All of GPIOs are always in input direction in default after power-on-reset
- The drive strength for all of GPIOs is software-programmable

- USB Host2.0
  - Embedded 2 USB Host2.0 interfaces
  - USB host (ECHI controller) only supports USB2.0, does not support USB1.1.
    USB host (DW controller) support USB2.0/USB1.1.
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed (1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed (1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.2.19 Others

- Temperature Sensor(TS-ADC)
  - 3 bipolar-based temperature-sensing cell embedded
  - 3-channel 12-bits SAR ADC

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter

- eFuse
  - Two high-density electrical Fuse is integrated: 256bits (32x8) / 1024bits (32x32)
  - Support standby mode

Notes :① : DDR3/LPDDR2/LPDDR3 are not used simultaneously as well as async and sync ddr nand flash
② : In RK3288, Video decoder and encoder are not used simultaneously because of shared internal buffer
③ : Actual maximum frame rate will depend on the clock frequency and system bus performance
④ : Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3288.

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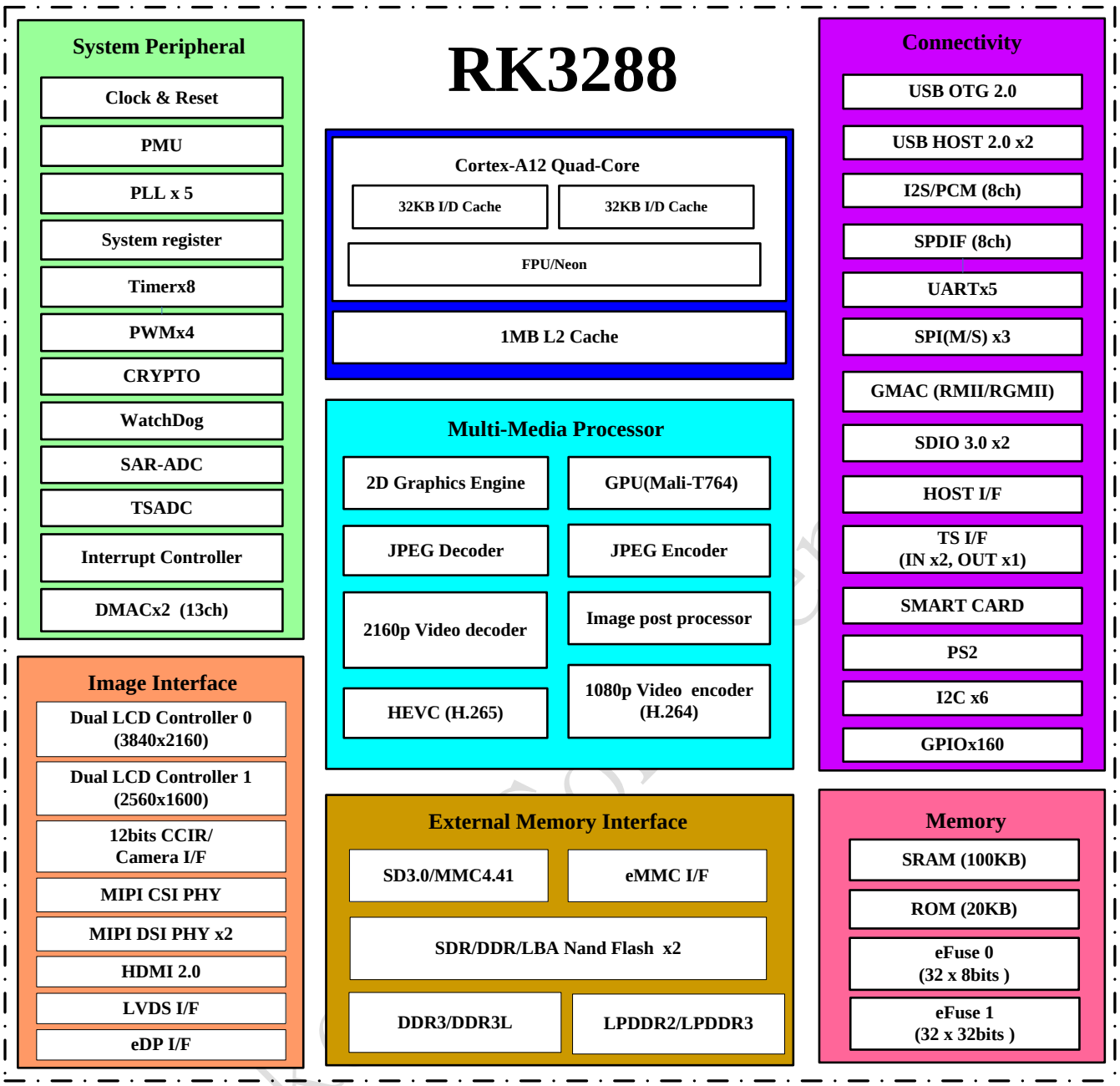

Fig. 1-1 RK3288 Block Diagram

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Chapter 2 System Overview

2.1 Address Mapping

RK3288 support to boot from internal bootrom, which support remap function by software programming. Remap is controlled by SGRF_SOC_CON0 bit[11].

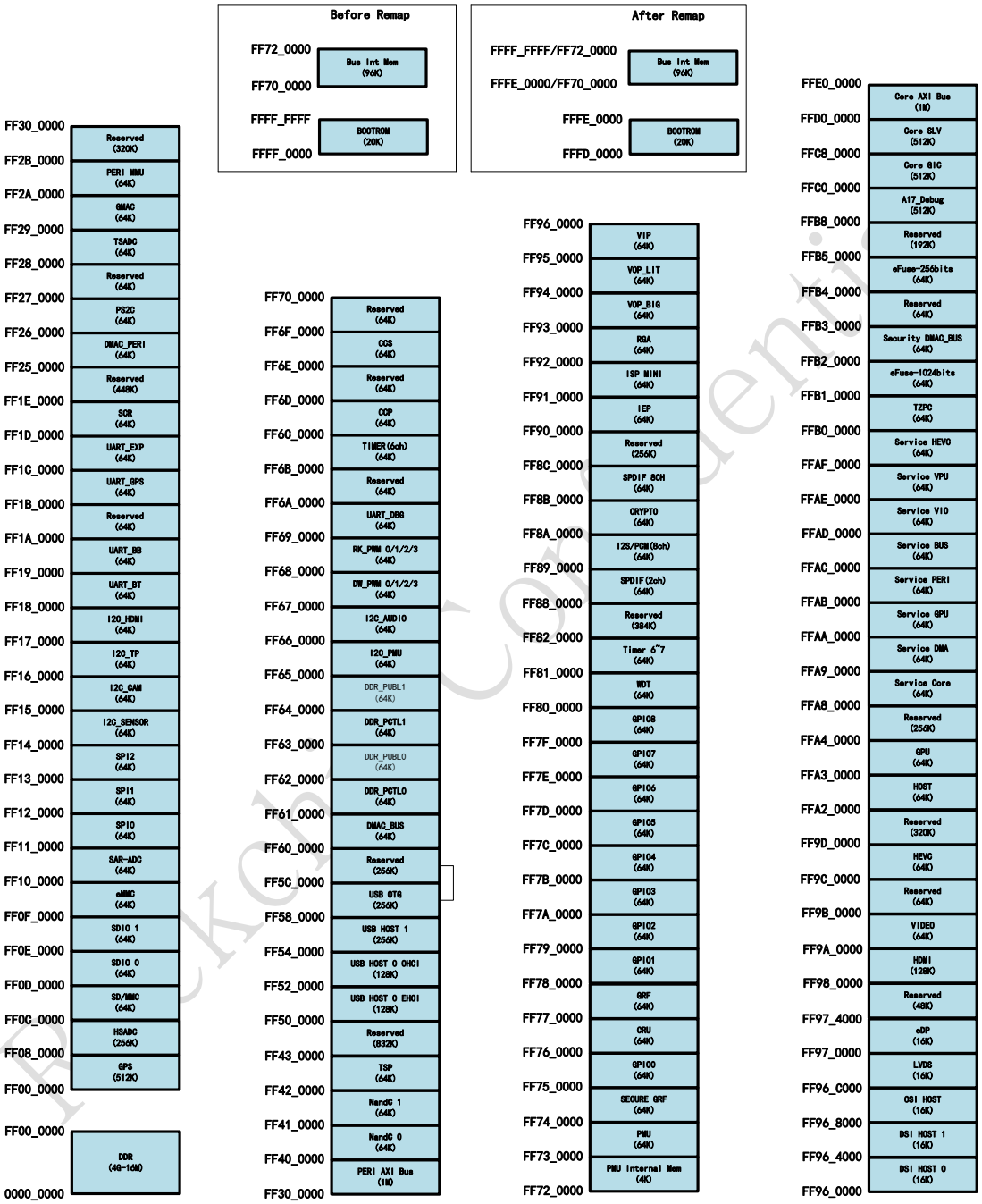

Fig. 2-1 RK3288 Address Mapping

2.2 System Boot

RK3288 provides system boot from off-chip devices such as SDMMC card, 8bits async nand flash or toggle nand flash, SPI nor or nand, and eMMC memory. When boot code is not ready in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal bootrom. The following is the whole boot procedure for boot

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code, which will be stored in bootrom in advance.

The following features are supports.

Support secure boot mode and non-secure boot mode
Support system boot from the following device:
8bits Async Nand Flash
8bits Toggle Nand Flash
SPI2_CS0 interface
eMMC interface
SDMMC Card
Support system code download by USB OTG

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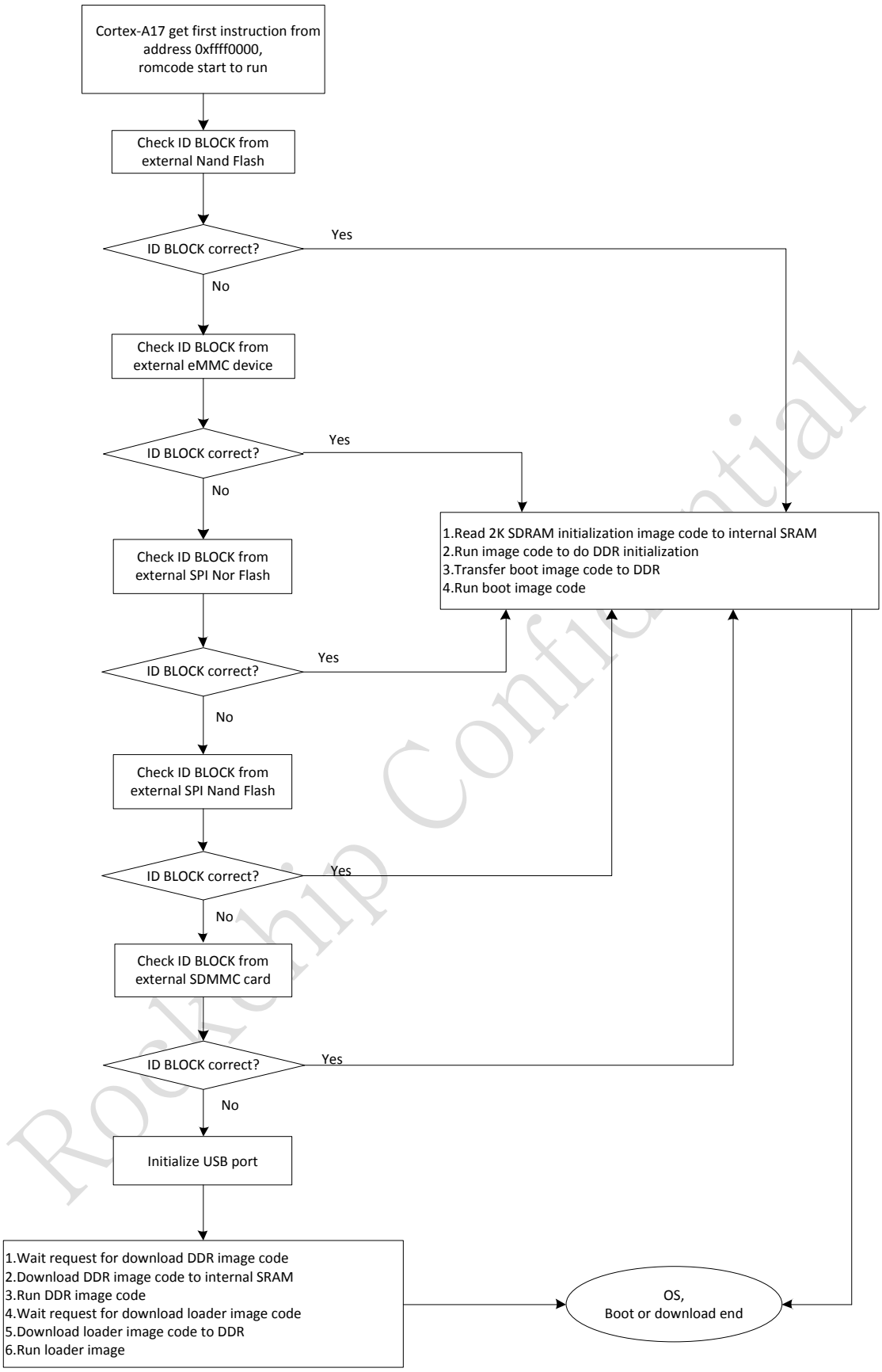

Fig. 2-2 RK3288 boot procedure flow

2.3 System Interrupt connection

RK3288 provides an general interrupt controller(GIC) for Cortex-A17 MPCore processor, which has 112 SPI (shared peripheral interrupts) interrupt sources and 3 PPI(Private peripheral

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interrupt) interrupt source and separately generates one nIRQ and one nFIQ to CPU. The triggered type for each interrupts is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table. For detailed GIC setting, please refer to Chapter 13.

Table 2-1 RK3288 Interrupt connection list

IRQ Type	IRQ ID	Source(spi)	Polarity
PPI	26	HYPERVISOR TIMER	High level
	27	VIRTUAL TIMER	High level
	29	SECURE PHYSICAL TIMER	High level
	30	NON-SECURE PHY TIMER	High level
SPI	32	DMAC_BUS (0)	High level
	33	DMAC_BUS (1)	High level
	34	DMAC_PERI (0)	High level
	35	DMAC_PERI (1)	High level
	36	UPCTL 0	High level
	37	UPCTL 1	High level
	38	GPU_IRQJOB	High level
	39	GPU_IRQMMU	High level
	40	GPU_IRQGPU	High level
	41	VIDEO ENCODER	High level
	42	VIDEO DECODER	High level
	43	VIDEO MMU	High level
	44	HEVC	High level
	45	VIP	High level
	46	ISP	High level
	47	VOP_BIG	High level
	48	VOP_LIT	High level
	49	IEP	High level
	50	RGA	High level
	51	DSI 0 HOST	High level
	52	DSI 1 HOST	High level
	53	CSI HOST 0	High level
	54	CSI HOST 1	High level
	55	USB OTG	High level
	56	USB HOST 0 EHCI	High level
	57	USB HOST 1	High level
	58	N/A	High level
	59	GMAC	High level
	60	GMAC PMT	High level
	61	GPS	High level
	62	GPS TIMER	High level
	63	HS-ADC/TSI	High level
	64	SD/MMC	High level
	65	SDIO 0	High level
	66	SDIO 1	High level
	67	eMMC	High level

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IRQ Type	IRQ ID	Source(spi)	Polarity
	68	SARADC	High level
	69	TSADC	High level
	70	NANDC 0	High level
	71	PERI MMU	High level
	72	NANDC 1	High level
	73	USB HOST 0 OHCI	High level
	74	TPS	High level
	75	SCR	High level
	76	SPI0	High level
	77	SPI1	High level
	78	SPI2	High level
	79	PS2C	High level
	80	CRYPTO	High level
	81	HOST PULSE 0	High level
	82	HOST PULSE 1	High level
	83	HOST 0	High level
	84	HOST 1	High level
	85	I2S/PCM (8ch)	High level
	86	SPDIF(8ch)	High level
	87	UART_BT	High level
	88	UART_BB	High level
	89	UART_DBG	High level
	90	UART_GPS	High level
	91	UART_EXP	High level
	92	I2C_PMU	High level
	93	I2C_AUDIO	High level
	94	I2C_SENSOR	High level
	95	I2C_CAM	High level
	96	I2C_TP	High level
	97	I2C_HDMI	High level
	98	TIMER 6CH 0	High level
	99	TIMER 6CH 1	High level
	100	TIMER 6CH 2	High level
	101	TIMER 6CH 3	High level
	102	TIMER 6CH 4	High level
	103	TIMER 6CH 5	High level
	104	TIMER 2CH 0	High level
	105	TIMER 2CH 1	High level
	106	PWM0	High level
	107	PWM1	High level
	108	PWM2	High level
	109	PWM3	High level
	110	RK_PWM	High level
	111	WDT	High level

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IRQ Type	IRQ ID	Source(spi)	Polarity
	112	PMU	High level
	113	GPIO0	High level
	114	GPIO1	High level
	115	GPIO2	High level
	116	GPIO3	High level
	117	GPIO4	High level
	118	GPIO5	High level
	119	GPIO6	High level
	120	GPIO7	High level
	121	GPIO8	High level
	122	AHB ARBITER0 (USB)	High level
	123	AHB ARBITER1 (EMEM)	High level
	124	AHB ARBITER2 (MMC)	High level
	125	USBOTG_ID	High level
	126	USBOTG_BVALID	High level
	127	USBOTG_LINESTATE	High level
	128	USBHOST0_LINESTATE	High level
	129	USBHOST1_LINESTATE	High level
	130	eDP DP	High level
	131	SDMMC_DETECT_N	High level
	132	SDIO0_DETECT_N	High level
	133	SDIO1_DETECT_N	High level
	134	HDMI WAKEUP	High level
	135	HDMI	High level
	136	CCP	High level
	137	CCS	High level
	138	SDMMC DETECT DUAL EDGE	High level
	139	GPIO7_B3 DUAL EDGE	High level
	140	GPIO7_C6_DUAL EDGE	High level
	141	GPIO8_A2_DUAL EDGE	High level
	142	eDP HDMI	High level
	143	HEVC MMU	High level
	183	PMUIRQ[0]	High level
	184	PMUIRQ[1]	High level
	185	PMUIRQ[2]	High level
	186	PMUIRQ[3]	High level

2.4 System DMA hardware request connection

RK3288 provides 2 DMA controllers: DMAC_BUS inside bus system and DMAC_PERI inside peripheral system. As for DMAC_BUS, there are 6 hardware request ports. Another, 15 hardware request ports are used in DMAC_PERI, the trigger type for each of them is high level, not programmable. For detailed descriptions of DMAC_BUS and DMAC_PERI, please refer to related section.

Table 2-2 RK3288 DMAC_BUS Hardware request connection list

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Req Number	Source	Polarity
0	I2S/PCM(8CH) TX	High level
1	I2S/PCM(8CH) RX	High level
2	SPDIF(2CH) TX	High level
3	SPDIF(8CH) TX	High level
4	UART_DBG TX	High level
5	UART_DBG RX	High level

Table 2-3 RK3288 DMAC_PERI Hardware request connection list

Req Number	Source	Polarity
0	HS-ADC/TSI	High level
1	UART_BT TX	High level
2	UART_BT RX	High level
3	UART_BB TX	High level
4	UART_BB RX	High level
5	N/A	N/A
6	N/A	N/A
7	UART_GPS TX	High level
8	UART_GPS RX	High level
9	UART_EXP TX	High level
10	UART_EXP RX	High level
11	SPI0 TX	High level
12	SPI0 RX	High level
13	SPI1 TX	High level
14	SPI1 RX	High level
15	SPI2 TX	High level
16	SPI2 RX	High level

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Chapter 3 Clock & Reset Unit (CRU)

3.1 Overview

The CRU is an APB slave module that is designed for generating all of the system clocks, resets of chip. CRU generates system clock from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset.

CRU supports the following features:

- Compliance to the AMBA APB interface
- Embedded five PLLs
- Flexible selection of clock source
- Supports the respective gating of all clocks
- Supports the respective software reset of all modules

3.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

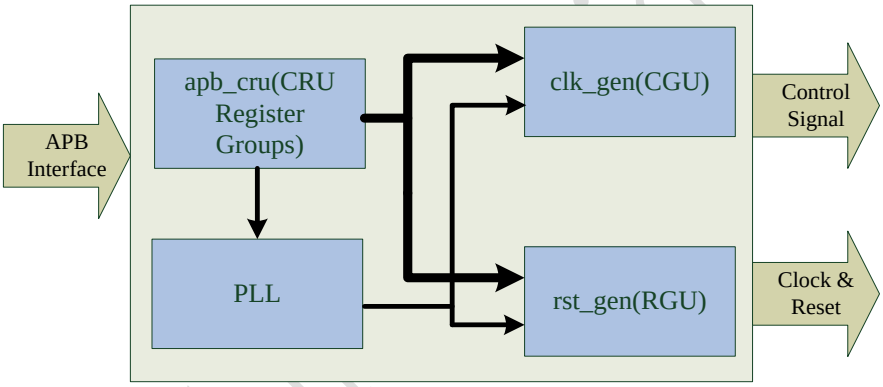

Fig. 3-1 CRU Architecture

3.3 System Reset Solution

The following diagrams show reset architecture in this block.

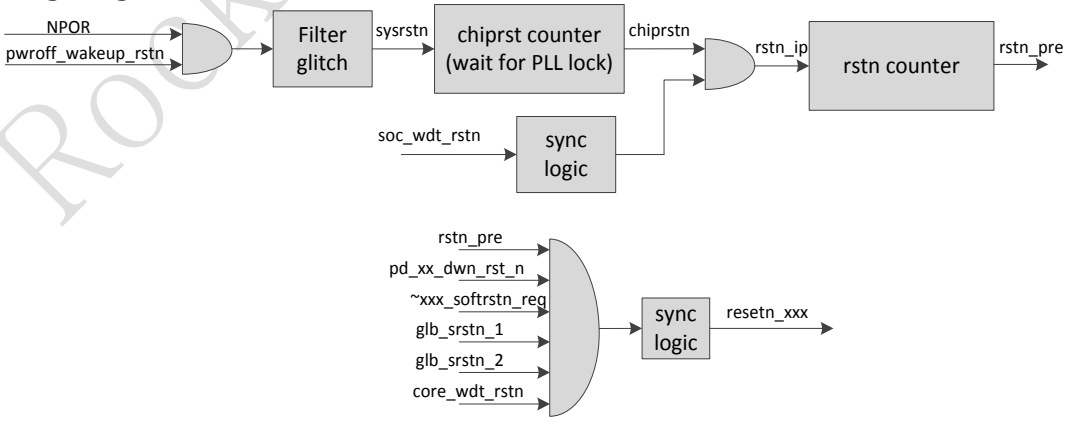

Fig. 3-2 Reset Architecture Diagram

Reset source of each reset signal includes hardware reset (NPOR), power-off mode wakeup reset (pwroff_wakeup_rstn), soc watch dog reset (soc_wdt_rstn), power domain power down reset (pd_xx_dwn_rst_n), software reset request (xxx_softrstn_req), global software reset1 (glb_srstn_1), global software reset2 (glb_srstn_2) and A9 core watch dog reset (core_wdt_rstn).

The 'xx' of pd_xx_dwn_rst_n represents core0, core1, core2, core3, cs, cpu, peri, vio, video or

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gpu. The 'xxx' of resetn_xxx and xxx_softrstn_req is the module name.
Pwroff_wakeup_rstn is the reset when wakeup from the power-off mode, it will reset the all SOC logic except internal PMU.
Soc_wdt_rstn is the reset from watch-dog IP in the SoC, but core_wdt_rstn is the reset from A9 core watch-dog block.
Glb_srstn_1 and glb_srstn_2 are the global software reset by programming CRU register. When writing register CRU_GLB_SRST_FST_VALUE as 0xfdb9, glb_srstn_1 will be asserted, and when writing register CRU_GLB_SRST_SND_VALUE as 0xeca8, glb_srstn_2 will be asserted. The two software resets will be self-clear by hardware. Glb_srstn_1 will reset the all logic except PMU_SYS_REG0~3. And Glb_srstn_2 will reset the all logic except PMU_SYS_REG0~3, GRF and all GPIOs.

3.4 Function Description

There are five PLLs:
ARM PLL, DDR PLL, CODEC PLL, GENERAL PLL and NEW PLL in CRU.
PLLs all can be set to slow mode or deep slow mode, directly output selectable 24MHz or 32.768kHz. When power on or changing PLL setting, we must force PLL into slow mode to ensure output stable clock.
To maximize the flexibility, some of clocks can select divider source from three PLLs (CODEC PLL, GENERAL PLL and NEW PLL).
To provide some specific frequency, another solution is integrated: fractional divider. In order to be sure the performance for divided clock, there is some usage limit, we can only get low frequency and divider factor must be larger than 20.
All clocks can be software gated and all reset can be software generated.

3.5 PLL Introduction

3.5.1 Overview

This chip uses 5GHz PLL for all four PLLs. The 5GHz PLL is a general purpose, high-performance PLL-based clock generator. The VCO operates from 440 MHz to 5000MHz, but the frequency range of 440 MHz to 2200MHz is recommended. It has a programmable output frequency, which ranges from 27.5 MHz to 5000 MHz configured through a 6-bit input divider, a 13-bit feedback divider and a 4-bit output divider. Around 50% duty cycle of output clocks can be achieved by enabling the output divider. It can also be used as a clock buffer through a bypass mode that bypasses and powers down the PLL. A full power-down mode is also available.
2.2GHz PLL supports the following features:

- Fully integrated, including loop filter
- Power supply: 1.0V single power supply
- VCO operating range: 440MHz – 5000MHz(440MHz – 2200MHz is recommended)
- Output frequency range: 27.5MHz – 5000MHz (27.5MHz – 2200MHz is recommended)
- Input frequency range: 269kHz – 5000MHz (269kHz – 2200MHz is recommended)
- PFD comparison frequency range: 269kHz – 5000MHz(269kHz – 2200MHz is recommended)
- Low power consumption: 3mA @ 1100MHz during normal operation
- Contains 6-bit input, 13-bit feedback and 4-bit output dividers
- Input divider value range: 1–64
- Feedback divider value range: 1–4096
- Output divider value range: 1, 2-16 (even only)
- Bandwidth adjustment of div. reference: 1–4096
- Output duty cycle: +/-5% (/1), +/-2% (/N)
- Period jitter (P-P) (max): +/-2.5% output cycle
- Reset pulse width (min): 5us
- Lock time (min allowed): 500 div. reference cycles
- Freq. overshot (full-~/half-~) (max): 40%/50%
- Ref. input jitter (long-term, P-P) (max): 2% div. reference cycle
- Reference H/L pulse width (min) : 230ps

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Bypass and Power-down mode
Lock detector

3.5.2 Block diagram

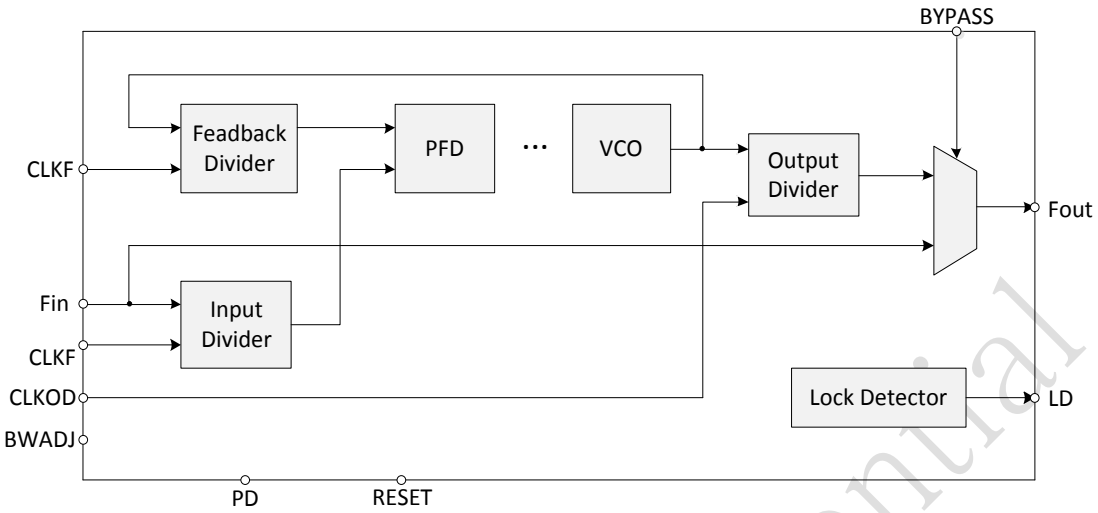

Fig. 3-3 PLL Block Diagram

3.5.3 Operation mode

Locked
The positive edges of the PLL feedback and reference signals are phase aligned in normal operation. Because the feedback signal is internal, NO phase relationship is guaranteed between RCLK and CLKOUT. The output clock frequency is programmable through the divider setting of CLKR[5:0], CLKF[12:0] and CLKOD[3:0].

Reset (RESET=1)
The PLL outputs a fixed free-running frequency in the range of 20MHz to 200MHz for a divide by 1 output depending on the specific PLL type.

Power-down (PWRDN=1)
All analog circuitry in the PLL is turned off so as to only dissipate leakage current. The digital dividers are not affected.

Bypass (BYPASS=1)
The reference input is bypassed directly to the outputs.

Test (TEST=1)
The reference input drives all dividers cascaded one after the other for production testing.

3.5.4 PLL Bandwidth Adjustment

The loop bandwidth (BW) of the PLL can be adjusted using BWADJ[11:0]. The bandwidth is given by: BW = nom_BW*sqrt(NF / 2 / NB), where nom_BW is approximately given by: nom_BW = Fref / (NR*20), and Fref is the reference clock frequency. The damping factor (D) is approximately given by: D = nom_D*sqrt(NF / 2 / NB), where nom_D is approximately 1. Because the damping factor changes with bandwidth settings, the bandwidth is practically limited to: nom_BW/sqrt(2) < BW < nom_BW*sqrt(2), in order to limit the damping factor range to 0.7 - 1.4. The -3dB bandwidth (Fbw_3dB) is approximately given by: Fbw_3dB = 2.4 * nom_BW * (NF / 2 / NB). The recommended setting for NB is NF / 2, which will yield the nominal bandwidth. Note that nom_BW and nom_D are chosen to result in optimal PLL loop dynamics.

3.6 Register Description

This section describes the control/status registers of the design.

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3.6.1 CRU Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_APLL_CON0	0x0000	W	0x00000b01	ARM PLL configuration register0
CRU_APLL_CON1	0x0004	W	0x000003e7	ARM PLL configuration register1
CRU_APLL_CON2	0x0008	W	0x000001f3	ARM PLL configuration register2
CRU_APLL_CON3	0x000c	W	0x00000008	ARM PLL configuration register3
CRU_DPLL_CON0	0x0010	W	0x00000b03	DDR PLL configuration register0
CRU_DPLL_CON1	0x0014	W	0x0000031f	DDR PLL configuration register1
CRU_DPLL_CON2	0x0018	W	0x0000018f	DDR PLL configuration register2
CRU_DPLL_CON3	0x001c	W	0x00000008	DDR PLL configuration register3
CRU_CPLL_CON0	0x0020	W	0x00000b03	CODEC PLL configuration register0
CRU_CPLL_CON1	0x0024	W	0x000002ff	CODEC PLL configuration register1
CRU_CPLL_CON2	0x0028	W	0x0000017f	CODEC PLL configuration register2
CRU_CPLL_CON3	0x002c	W	0x00000008	CODEC PLL configuration register3
CRU_GPLL_CON0	0x0030	W	0x00000b01	GENERAL PLL configuration register0
CRU_GPLL_CON1	0x0034	W	0x00000251	GENERAL PLL configuration register1
CRU_GPLL_CON2	0x0038	W	0x00000128	GENERAL PLL configuration register2
CRU_GPLL_CON3	0x003c	W	0x00000008	GENERAL PLL configuration register3
CRU_NPLL_CON0	0x0040	W	0x00000b03	NEW PLL configuration register0
CRU_NPLL_CON1	0x0044	W	0x000003e7	NEW PLL configuration register1
CRU_NPLL_CON2	0x0048	W	0x000001f3	NEW PLL configuration register2
CRU_NPLL_CON3	0x004c	W	0x00000008	NEW PLL configuration register3
CRU_MODE_CON	0x0050	W	0x00000000	System work mode control register
CRU_CLKSEL0_CON	0x0060	W	0x00000031	Internal clock select and divide register0
CRU_CLKSEL1_CON	0x0064	W	0x0000b109	Internal clock select and divide register1
CRU_CLKSEL2_CON	0x0068	W	0x00000020	Internal clock select and divide register2
CRU_CLKSEL3_CON	0x006c	W	0x00000200	Internal clock select and divide register3
CRU_CLKSEL4_CON	0x0070	W	0x00000300	Internal clock select and divide register4
CRU_CLKSEL5_CON	0x0074	W	0x00000200	Internal clock select and divide register5
CRU_CLKSEL6_CON	0x0078	W	0x00000101	Internal clock select and divide register6
CRU_CLKSEL7_CON	0x007c	W	0x0bb8ea60	Internal clock select and divide register7
CRU_CLKSEL8_CON	0x0080	W	0x0bb8ea60	Internal clock select and divide register8

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL9_CON	0x0084	W	0x0bb8ea60	Internal clock select and divide register9
CRU_CLKSEL10_CON	0x0088	W	0x0000a101	Internal clock select and divide register10
CRU_CLKSEL11_CON	0x008c	W	0x00002780	Internal clock select and divide register11
CRU_CLKSEL12_CON	0x0090	W	0x00008080	Internal clock select and divide register12
CRU_CLKSEL13_CON	0x0094	W	0x00000200	Internal clock select and divide register13
CRU_CLKSEL14_CON	0x0098	W	0x00000200	Internal clock select and divide register14
CRU_CLKSEL15_CON	0x009c	W	0x00000200	Internal clock select and divide register15
CRU_CLKSEL16_CON	0x00a0	W	0x00000200	Internal clock select and divide register16
CRU_CLKSEL17_CON	0x00a4	W	0x0bb8ea60	Internal clock select and divide register17
CRU_CLKSEL18_CON	0x00a8	W	0x0bb8ea60	Internal clock select and divide register18
CRU_CLKSEL19_CON	0x00ac	W	0x0bb8ea60	Internal clock select and divide register19
CRU_CLKSEL20_CON	0x00b0	W	0x0bb8ea60	Internal clock select and divide register20
CRU_CLKSEL21_CON	0x00b4	W	0x00000b00	Internal clock select and divide register21
CRU_CLKSEL22_CON	0x00b8	W	0x00000900	Internal clock select and divide register22
CRU_CLKSEL23_CON	0x00bc	W	0x001f05dc	Internal clock select and divide register23
CRU_CLKSEL24_CON	0x00c0	W	0x00001700	Internal clock select and divide register24
CRU_CLKSEL25_CON	0x00c4	W	0x00000707	Internal clock select and divide register25
CRU_CLKSEL26_CON	0x00c8	W	0x00000ec0	Internal clock select and divide register26
CRU_CLKSEL27_CON	0x00cc	W	0x00000700	Internal clock select and divide register27
CRU_CLKSEL28_CON	0x00d0	W	0x00000f03	Internal clock select and divide register28
CRU_CLKSEL29_CON	0x00d4	W	0x00000742	Internal clock select and divide register29
CRU_CLKSEL30_CON	0x00d8	W	0x00000000	Internal clock select and divide register30

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL31_CON	0x00dc	W	0x00000000	Internal clock select and divide register31
CRU_CLKSEL32_CON	0x00e0	W	0x00000101	Internal clock select and divide register32
CRU_CLKSEL33_CON	0x00e4	W	0x00000303	Internal clock select and divide register33
CRU_CLKSEL34_CON	0x00e8	W	0x00008000	Internal clock select and divide register34
CRU_CLKSEL35_CON	0x00ec	W	0x00000303	Internal clock select and divide register35
CRU_CLKSEL36_CON	0x00f0	W	0x00000000	Internal clock select and divide register36
CRU_CLKSEL37_CON	0x00f4	W	0x00001ef3	Internal clock select and divide register37
CRU_CLKSEL38_CON	0x00f8	W	0x00000303	Internal clock select and divide register38
CRU_CLKSEL39_CON	0x00fc	W	0x00000007	Internal clock select and divide register39
CRU_CLKSEL40_CON	0x0100	W	0x00000200	Internal clock select and divide register40
CRU_CLKSEL41_CON	0x0104	W	0x0bb8ea60	Internal clock select and divide register41
CRU_CLKSEL42_CON	0x0108	W	0x00000000	Internal clock select and divide register42
CRU_CLKGATE0_CON	0x0160	W	0x00000000	Internal clock gating control register0
CRU_CLKGATE1_CON	0x0164	W	0x00000000	Internal clock gating control register1
CRU_CLKGATE2_CON	0x0168	W	0x00000000	Internal clock gating control register2
CRU_CLKGATE3_CON	0x016c	W	0x00000000	Internal clock gating control register3
CRU_CLKGATE4_CON	0x0170	W	0x00000000	Internal clock gating control register4
CRU_CLKGATE5_CON	0x0174	W	0x00000000	Internal clock gating control register5
CRU_CLKGATE6_CON	0x0178	W	0x00000000	Internal clock gating control register6
CRU_CLKGATE7_CON	0x017c	W	0x00000000	Internal clock gating control register7
CRU_CLKGATE8_CON	0x0180	W	0x00000000	Internal clock gating control register8
CRU_CLKGATE9_CON	0x0184	W	0x00000000	Internal clock gating control register9

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Name	Offset	Size	Reset Value	Description
CRU_CLKGATE10_CON	0x0188	W	0x00000000	Internal clock gating control register10
CRU_CLKGATE11_CON	0x018c	W	0x00000000	Internal clock gating control register11
CRU_CLKGATE12_CON	0x0190	W	0x00000000	Internal clock gating control register12
CRU_CLKGATE13_CON	0x0194	W	0x00000000	Internal clock gating control register13
CRU_CLKGATE14_CON	0x0198	W	0x00000000	Internal clock gating control register14
CRU_CLKGATE15_CON	0x019c	W	0x00000000	Internal clock gating control register15
CRU_CLKGATE16_CON	0x01a0	W	0x00000000	Internal clock gating control register16
CRU_CLKGATE17_CON	0x01a4	W	0x00000000	Internal clock gating control register17
CRU_CLKGATE18_CON	0x01a8	W	0x00000000	Internal clock gating control register18
CRU_GLB_SRST_FST_VALUE	0x01b0	W	0x00000000	The first global software reset config value
CRU_GLB_SRST_SND_VALUE	0x01b4	W	0x00000000	The second global software reset config value
CRU_SOFTRST0_CON	0x01b8	W	0x00000000	Internal software reset control register0
CRU_SOFTRST1_CON	0x01bc	W	0x00000000	Internal software reset control register1
CRU_SOFTRST2_CON	0x01c0	W	0x00000000	Internal software reset control register2
CRU_SOFTRST3_CON	0x01c4	W	0x00000000	Internal software reset control register3
CRU_SOFTRST4_CON	0x01c8	W	0x00000000	Internal software reset control register4
CRU_SOFTRST5_CON	0x01cc	W	0x00000000	Internal software reset control register5
CRU_SOFTRST6_CON	0x01d0	W	0x00000000	Internal software reset control register6
CRU_SOFTRST7_CON	0x01d4	W	0x00000000	Internal software reset control register7
CRU_SOFTRST8_CON	0x01d8	W	0x00000000	Internal software reset control register8
CRU_SOFTRST9_CON	0x01dc	W	0x00000000	Internal software reset control register9
CRU_SOFTRST10_CON	0x01e0	W	0x00000000	Internal software reset control register10

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Name	Offset	Size	Reset Value	Description
CRU_SOFTRST11_CON	0x01e4	W	0x00000000	Internal software reset control register11
CRU_MISC_CON	0x01e8	W	0x00000000	SCU control register
CRU_GLB_CNT_TH	0x01ec	W	0x00000064	global reset wait counter threshold
CRU_GLB_RST_CON	0x01f0	W	0x00000000	global reset trigger select
CRU_GLB_RST_ST	0x01f8	W	0x00000000	global reset status
CRU_SDMMC_CON0	0x0200	W	0x00000002	sdmmc control0
CRU_SDMMC_CON1	0x0204	W	0x00000000	sdmmc control1
CRU_SDIO0_CON0	0x0208	W	0x00000002	sdio0 control0
CRU_SDIO0_CON1	0x020c	W	0x00000000	sdio0 control1
CRU_SDIO1_CON0	0x0210	W	0x00000002	sdio1 control0
CRU_SDIO1_CON1	0x0214	W	0x00000000	sdio1 control1
CRU_EMMC_CON0	0x0218	W	0x00000002	emmc control0
CRU_EMMC_CON1	0x021c	W	0x00000000	emmc control1

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

3.6.2 Detail Register Description

CRU_APLL_CON0
Address: Operational Base + offset (0x0000)
ARM PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKR + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x1	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_APLL_CON1

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Address: Operational Base + offset (0x0004)
ARM PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x03e7	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_APLL_CON2
Address: Operational Base + offset (0x0008)
ARM PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x1f3	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_APLL_CON3
Address: Operational Base + offset (0x000c)
ARM PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_DPLL_CON0
Address: Operational Base + offset (0x0010)
DDR PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKR + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x3	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_DPLL_CON1
Address: Operational Base + offset (0x0014)
DDR PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x031f	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_DPLL_CON2
Address: Operational Base + offset (0x0018)
DDR PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x18f	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_DPLL_CON3
Address: Operational Base + offset (0x001c)
DDR PLL configuration register3

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Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_CPLL_CON0
Address: Operational Base + offset (0x0020)
CODEC PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKR + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x3	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_CPLL_CON1
Address: Operational Base + offset (0x0024)
CODEC PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock

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Bit	Attr	Reset Value	Description
30:13	RO	0x0	reserved
12:0	RW	0x02ff	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_CPLL_CON2
Address: Operational Base + offset (0x0028)
CODEC PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x17f	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_CPLL_CON3
Address: Operational Base + offset (0x002c)
CODEC PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_GPLL_CON0
Address: Operational Base + offset (0x0030)
GENERAL PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKR + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x1	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_GPLL_CON1
Address: Operational Base + offset (0x0034)
GENERAL PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x0251	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_GPLL_CON2
Address: Operational Base + offset (0x0038)
GENERAL PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x128	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_GPLL_CON3
Address: Operational Base + offset (0x003c)
GENERAL PLL configuration register3

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Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_NPLL_CON0
Address: Operational Base + offset (0x0040)
NEW PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKR + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x3	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_NPLL_CON1
Address: Operational Base + offset (0x0044)
NEW PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock

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Bit	Attr	Reset Value	Description
30:13	RO	0x0	reserved
12:0	RW	0x03e7	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_NPLL_CON2
Address: Operational Base + offset (0x0048)
NEW PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x1f3	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_NPLL_CON3
Address: Operational Base + offset (0x004c)
NEW PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_MODE_CON
Address: Operational Base + offset (0x0050)
System work mode control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	npll_work_mode NEW PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpll_work_mode GENERAL PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
11:10	RO	0x0	reserved
9:8	RW	0x0	cpll_work_mode CODEC PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7:6	RO	0x0	reserved
5:4	RW	0x0	dpll_work_mode DDR PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
3:2	RO	0x0	reserved
1:0	RW	0x0	apll_work_mode ARM PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz

CRU_CLKSEL0_CON
Address: Operational Base + offset (0x0060)
Internal clock select and divide register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	core_clk_pll_sel CORE clock pll source selection 1'b0: select ARM PLL 1'b1: select GENERAL PLL
14:13	RO	0x0	reserved
12:8	RW	0x00	a17_core_div_con Control A17 core clock divider frequency clk_core=clk_src/(div_con+1)
7:4	RW	0x3	aclk_core_mp_div_con Control core MP AXI clock divider frequency clk=clk_src/(div_con+1)

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Bit	Attr	Reset Value	Description
3:0	RW	0x1	aclk_core_m0_div_con Control core M0 AXI clock divider frequency clk=clk_src/(div_con+1)

CRU_CLKSEL1_CON
Address: Operational Base + offset (0x0064)
Internal clock select and divide register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	bus_aclk_pll_sel pd_bus axi clock pll source selection 1'b0: select CODEC PLL 1'b1: select GENERAL PLL
14:12	RW	0x3	pd_bus_pclk_div_con Control pd_bus APB clock divider frequency clk=clk_src/(div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x1	pd_bus_hclk_div_con Control pd_bus AHB clock divider frequency 2'b00: aclk_bus:hclk_bus = 1:1 2'b01: aclk_bus:hclk_bus = 2:1 2'b11: aclk_bus:hclk_bus = 4:1
7:3	RW	0x01	pd_bus_aclk_div_con Control pd_bus aclk divider frequency clk=clk_src/(div_con+1)
2:0	RW	0x1	pd_bus_clk_div_con1 Control pd_bus AXI clock divider1 frequency clk=clk_src/(div_con+1)

CRU_CLKSEL2_CON
Address: Operational Base + offset (0x0068)
Internal clock select and divide register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	testout_div_con test out clk divider frequency clk_testout=testout_clk_src/(testout_div_con+1)
7:6	RO	0x0	reserved
5:0	RW	0x20	tsadc_div_con Control tsadc divider frequency clk_tsadc=tsadc_clk_src/(tsadc_div_con+1)

CRU_CLKSEL3_CON
Address: Operational Base + offset (0x006c)
Internal clock select and divide register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart4_clk_sel Control UART4 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart4_div_con Control UART4 divider frequency clk_uart0=uart_clk_src/(uart0_div_con+1)

CRU_CLKSEL4_CON
Address: Operational Base + offset (0x0070)
Internal clock select and divide register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	i2s_pll_sel Control I2S PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	i2s0_outclk_sel Control I2S clock work frequency selection 1'b0: select clk_i2s 1'b1: select 12MHz
11:10	RO	0x0	reserved
9:8	RW	0x3	i2s0_clk_sel Control I2S clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select clock from IO input 2'b11: select 12MHz from osc input
7	RO	0x0	reserved
6:0	RW	0x00	i2s0_pll_div_con Control I2S PLL output divider freuency i2s1_div_clk=i2s1_div_src/(i2s1_pll_div_con+1)

CRU_CLKSEL5_CON
Address: Operational Base + offset (0x0074)
Internal clock select and divide register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	spdif_pll_sel Control SPDIF PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:10	RO	0x0	reserved
9:8	RW	0x2	spdif_clk_sel Control SPDIF clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 12MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	spdif_pll_div_con Control SPDIF PLL output divider freuency spdif_div_clk=spdif_div_src/(spdif_pll_div_con+1)

CRU_CLKSEL6_CON
Address: Operational Base + offset (0x0078)
Internal clock select and divide register6

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	isp_jpeg_pll_sel Control ISP jpeg PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
13:8	RW	0x01	isp_jpeg_div_con Control isp jpeg divider freuency jpeg_div_clk=jpeg_div_src/(isp_jpeg_div_con+1)
7:6	RW	0x0	isp_pll_sel Control ISP PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5:0	RW	0x01	isp_div_con Control isp divider freuency isp_div_clk=isp_div_src/(isp_pll_div_con+1)

CRU_CLKSEL7_CON
Address: Operational Base + offset (0x007c)
Internal clock select and divide register7

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart4_frac_factor Control uart4 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL8_CON
Address: Operational Base + offset (0x0080)
Internal clock select and divide register8

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	i2s0_frac_factor Control I2S fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL9_CON
Address: Operational Base + offset (0x0084)
Internal clock select and divide register9

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Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	spdif_frac_factor Control SPDIF fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL10_CON
Address: Operational Base + offset (0x0088)
Internal clock select and divide register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	peri_pll_sel Control peripheral clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14	RO	0x0	reserved
13:12	RW	0x2	peri_pclk_div_con Control the divider ratio between aclk_periph and pclk_periph 2'b00: aclk_periph:pclk_periph = 1:1 2'b01: aclk_periph:pclk_periph = 2:1 2'b10: aclk_periph:pclk_periph = 4:1 2'b11: aclk_periph:pclk_periph = 8:1
11:10	RO	0x0	reserved
9:8	RW	0x1	peri_hclk_div_con Control the divider ratio between aclk_periph and hclk_periph 2'b00: aclk_periph:hclk_periph = 1:1 2'b01: aclk_periph:hclk_periph = 2:1 2'b10: aclk_periph:hclk_periph = 4:1
7:5	RO	0x0	reserved
4:0	RW	0x01	peri_aclk_div_con Control periphral clock divider frequency aclk_periph=periph_clk_src/(peri_aclk_div_con+1)

CRU_CLKSEL11_CON
Address: Operational Base + offset (0x008c)
Internal clock select and divide register11

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x27	reserved
7:6	RW	0x2	mmc0_pll_sel Control mmc0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
5:0	RW	0x00	mmc0_div_con Control SDMMC0 divider frequency clk_sdmmc0=general_pll_clk/(mmc0_div_con+1)

CRU_CLKSEL12_CON
Address: Operational Base + offset (0x0090)
Internal clock select and divide register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x2	emmc_pll_sel Control emmc clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
13:8	RW	0x00	emmc_div_con Control EMMC divider frequency clk_emmc=general_pll_clk/(emmc_div_con+1)
7:6	RW	0x2	sdio0_pll_sel Control sdio0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
5:0	RW	0x00	sdio0_div_con Control SDIO0 divider frequency clk_sdio=general_pll_clk/(sdio_div_con+1)

CRU_CLKSEL13_CON
Address: Operational Base + offset (0x0094)
Internal clock select and divide register13

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	uart_pll_sel Control UART1~4 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:13	RW	0x0	uart0_src_sel UART0 clock source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 480M USBPHY clock 2'b11: select new pll clock
12:11	RW	0x0	usbphy_480m_sel USBPHY 480M clock source selection 2'b00: select HOST0 USB pll clock 2'b01: select HOST1 USB pll clock 2'b10: select OTG USB pll clock
10	RO	0x0	reserved
9:8	RW	0x2	uart0_clk_sel Control UART0 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart0_div_con Control UART0 divider frequency clk_uart0=uart_clk_src/(uart0_div_con+1)

CRU_CLKSEL14_CON
Address: Operational Base + offset (0x0098)
Internal clock select and divide register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	uart1_clk_sel Control UART1 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart1_div_con Control UART1 divider frequency clk_uart1=uart_clk_src/(uart1_div_con+1)

CRU_CLKSEL15_CON
Address: Operational Base + offset (0x009c)
Internal clock select and divide register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart2_clk_sel Control UART2 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart2_div_con Control UART2 divider frequency clk_uart2=uart_clk_src/(uart2_div_con+1)

CRU_CLKSEL16_CON
Address: Operational Base + offset (0x00a0)
Internal clock select and divide register16

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	uart3_clk_sel Control UART3 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart3_div_con Control UART3 divider frequency clk_uart3=uart_clk_src/(uart3_div_con+1)

CRU_CLKSEL17_CON
Address: Operational Base + offset (0x00a4)
Internal clock select and divide register17

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart0_frac_factor Control UART0 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL18_CON
Address: Operational Base + offset (0x00a8)
Internal clock select and divide register18

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart1_frac_factor Control UART1 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL19_CON
Address: Operational Base + offset (0x00ac)
Internal clock select and divide register19

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart2_frac_factor Control UART2 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL20_CON
Address: Operational Base + offset (0x00b0)
Internal clock select and divide register20

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Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart3_frac_factor Control UART3 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL21_CON
Address: Operational Base + offset (0x00b4)
Internal clock select and divide register21

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x0b	mac_div_con Control EMAC divider frequency clk_mac_ref=mac_clk_src/(mac_div_con+1)
7:5	RO	0x0	reserved
4	RW	0x0	rmii_extclk_sel Control RMII external clock selection 1'b0: select internal divider clock 1'b1: select external input clock
3:2	RO	0x0	reserved
1:0	RW	0x0	mac_pll_sel Control EMAC clock PLL source selection 2'b00: select new pll clock 2'b01: select codec pll clock 2'b10: select general pll clock

CRU_CLKSEL22_CON
Address: Operational Base + offset (0x00b8)
Internal clock select and divide register22

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x09	hsadc_div_con Control HSADC divider frequency clk_hsadc=hsadc_clk_src/(hsadc_div_con+1)

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Bit	Attr	Reset Value	Description
7	RW	0x0	hsadc_inv_sel Control HSADC inverter clock 1'b0: select buffer output 1'b1: select inverter output
6:5	RO	0x0	reserved
4	RW	0x0	hsadc_clk_sel Control HSADC clock work frequency selection 1'b0: select divider ouput from pll divider 1'b1: select external input clock
3:2	RO	0x0	reserved
1	RW	0x0	wifi_pll_sel Control wifi clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
0	RW	0x0	hsadc_pll_sel Control HSADC clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock

CRU_CLKSEL23_CON
Address: Operational Base + offset (0x00bc)
Internal clock select and divide register23

Bit	Attr	Reset Value	Description
31:0	RW	0x001f05dc	wifi_frac_factor Control wifi fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL24_CON
Address: Operational Base + offset (0x00c0)
Internal clock select and divide register24

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x17	saradc_div_con Control SARADC clock divider frequency clk_saradc=24MHz/(saradc_div_con+1)
7:0	RO	0x0	reserved

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CRU_CLKSEL25_CON
Address: Operational Base + offset (0x00c4)
Internal clock select and divide register25

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	spi1_pll_sel Control spi1 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:8	RW	0x07	spi1_div_con Control SPI1 clock divider frequency clk_spi1=general_pll_clk/(spi1_div_con+1)
7	RW	0x0	spi0_pll_sel Control spi0 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
6:0	RW	0x07	spi0_div_con Control SPI0 clock divider frequency clk_spi0=general_pll_clk/(spi0_div_con+1)

CRU_CLKSEL26_CON
Address: Operational Base + offset (0x00c8)
Internal clock select and divide register26

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	cif_clk_out_sel CIF clock output selection 1'b0: select PLL divout 1'b1: select 24MHz
14	RO	0x0	reserved
13:9	RW	0x07	cif_clk_div_con cif clock divider frequency clk=clk_src/(div_con+1)
8	RW	0x0	cif_clk_pll_sel CIF clock pll source selection 1'b0: select codec PLL 1'b1: select general PLL

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Bit	Attr	Reset Value	Description
7:6	RW	0x3	crypto_div_con crypto clock divider frequency clk=clk_src/(div_con+1)
5:3	RO	0x0	reserved
2	RW	0x0	ddr_clk_pll_sel DDR clock pll source selection 1'b0: select DDR PLL 1'b1: select GENERAL PLL
1:0	RW	0x0	ddr_div_con Control DDR divider frequency 2'b00: clk_ddr_src:clk_ddrphy = 1:1 2'b01: clk_ddr_src:clk_ddrphy = 2:1 2'b11: clk_ddr_src:clk_ddrphy = 4:1

CRU_CLKSEL27_CON
Address: Operational Base + offset (0x00cc)
Internal clock select and divide register27

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x07	lcdc0_div_con Control LCDC0 clock divider frequency clk_lcdc0=lcdc0_clk_src/(lcdc0_div_con+1)
7:2	RO	0x0	reserved
1:0	RW	0x0	lcdc0_pll_sel Control LCDC0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock

CRU_CLKSEL28_CON
Address: Operational Base + offset (0x00d0)
Internal clock select and divide register28

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15	RW	0x0	edp_24m_sel eDP 24M clock source selection 1'b00: select 27M clock 1'b01: select 24M clock
14:13	RO	0x0	reserved
12:8	RW	0x0f	hclk_vio_div_con VIO AHB clock divider frequency clk=clk_src/(div_con+1)
7:6	RW	0x0	edp_pll_sel eDP clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5:0	RW	0x03	edp_div_con eDP clock divider frequency clk=clk_src/(div_con+1)

CRU_CLKSEL29_CON
Address: Operational Base + offset (0x00d4)
Internal clock select and divide register29

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x07	lcdc1_div_con Control LCDC1 clock divider frequency clk_lcdc1=lcdc1_clk_src/(lcdc1_div_con+1)
7:6	RW	0x1	lcdc1_pll_sel Control LCDC1 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5	RO	0x0	reserved
4	RW	0x0	cif_clkin_inv_sel CIF clkin invert selection 1'b0: normal 1'b1: invert
3	RW	0x0	isp_clkin_inv_sel ISP clkin invert selection 1'b0: normal 1'b1: invert
2	RW	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x2	reserved

CRU_CLKSEL30_CON
Address: Operational Base + offset (0x00d8)
Internal clock select and divide register30

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	rga_core_clk_pll_sel rga func clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
13	RO	0x0	reserved
12:8	RW	0x00	rga_core_clk_div_con rga func clock divider frequency clk_rga_func = clk_rga_func_src/(rga_core_clk_div_con+1)
7:6	RW	0x0	rga_aclk_pll_sel Control rga AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
5	RO	0x0	reserved
4:0	RW	0x00	rga_aclk_div_con Control rga AXI clock divider frequency aclk_lcdc1=lcdc1_aclk_src/(rga_aclk_div_con+1)

CRU_CLKSEL31_CON
Address: Operational Base + offset (0x00dc)
Internal clock select and divide register31

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	vio1_aclk_pll_sel Control VIO1 AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock

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Bit	Attr	Reset Value	Description
13	RO	0x0	reserved
12:8	RW	0x00	vio1_aclk_div_con Control VIO1 AXI clock divider frequency aclk_vio1=vio1_aclk_src/(vio1_aclk_div_con+1)
7:6	RW	0x0	vio0_aclk_pll_sel Control VIO0 AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
5	RO	0x0	reserved
4:0	RW	0x00	vio0_aclk_div_con Control VIO0 AXI clock divider frequency aclk_vio0=vio0_aclk_src/(vio0_aclk_div_con+1)

CRU_CLKSEL32_CON
Address: Operational Base + offset (0x00e0)
Internal clock select and divide register32

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	vdpu_aclk_pll_sel Control VDPU AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
13	RO	0x0	reserved
12:8	RW	0x01	vdpu_aclk_div_con Control VDPU AXI clock divider frequency aclk_vdpu=vdpu_aclk_src/(vdpu_aclk_div_con+1)
7:6	RW	0x0	vepu_aclk_pll_sel Control VEPU AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
5	RO	0x0	reserved
4:0	RW	0x01	vepu_aclk_div_con Control VEPU AXI clock divider frequency aclk_vepu=vepu_aclk_src/(vepu_aclk_div_con+1)

CRU_CLKSEL33_CON

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Address: Operational Base + offset (0x00e4)
Internal clock select and divide register33

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x03	alive_pclk_div_con alive apb clock divider frequency alive_pclk =alive_pclk_src/(alive_pclk_div_con+1)
7:5	RO	0x0	reserved
4:0	RW	0x03	pmu_pclk_div_con pmu apb clock divider frequency pmu_pclk =pmu_pclk_src/(pmu_pclk_div_con+1)

CRU_CLKSEL34_CON
Address: Operational Base + offset (0x00e8)
Internal clock select and divide register34

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x2	sdio1_pll_sel Control sdio1 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
13:8	RW	0x00	sdio1_div_con Control SDIO1 divider frequency clk_sdio=general_pll_clk/(sdio_div_con+1)
7:6	RW	0x0	gpu_aclk_pll_sel Control GPU AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock 2'b11: select new pll clock
5	RO	0x0	reserved
4:0	RW	0x00	gpu_aclk_div_con Control GPU AXI clock divider frequency aclk_gpu=gpu_aclk_src/(gpu_aclk_div_con+1)

CRU_CLKSEL35_CON

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Address: Operational Base + offset (0x00ec)
Internal clock select and divide register35

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	tspout_clk_pll_sel Control tspout clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock 2'b11: select 27MHz IO input
13	RO	0x0	reserved
12:8	RW	0x03	tspout_clk_div_con Control tspout clock divider frequency clk=clk_src/(clk_div_con+1)
7:6	RW	0x0	tsp_clk_pll_sel Control tsp clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5	RO	0x0	reserved
4:0	RW	0x03	tsp_clk_div_con Control tsp clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKSEL36_CON
Address: Operational Base + offset (0x00f0)
Internal clock select and divide register36

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	clk_core3_div_con Control clk_core3 clock divider frequency clk=clk_src/(clk_div_con+1)
11	RO	0x0	reserved
10:8	RW	0x0	clk_core2_div_con Control clk_core2 clock divider frequency clk=clk_src/(clk_div_con+1)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	clk_core1_div_con Control clk_core1 clock divider frequency clk=clk_src/(clk_div_con+1)
3	RO	0x0	reserved
2:0	RW	0x0	clk_core0_div_con Control clk_core0 clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKSEL37_CON
Address: Operational Base + offset (0x00f4)
Internal clock select and divide register37

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:9	RW	0x0f	pclk_core_dbg_div_con Control core debg APB bus clock divider frequency clk=clk_src/(clk_div_con+1)
8:4	RW	0x0f	atclk_core_div_con Control core ATB BUS clock divider frequency clk=clk_src/(clk_div_con+1)
3	RO	0x0	reserved
2:0	RW	0x3	clk_l2ram_div_con Control clk_l2ram clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKSEL38_CON
Address: Operational Base + offset (0x00f8)
Internal clock select and divide register38

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	nandc1_clk_pll_sel Control nandc1 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x03	nandc1_clk_div_con Control nandc1 clock divider frequency clk_nandc=nandc_clk_src/(nandc_clk_div_con+1)
7	RW	0x0	nandc0_clk_pll_sel Control nandc0 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
6:5	RO	0x0	reserved
4:0	RW	0x03	nandc0_clk_div_con Control nandc0 clock divider frequency clk_nandc=nandc_clk_src/(nandc_clk_div_con+1)

CRU_CLKSEL39_CON
Address: Operational Base + offset (0x00fc)
Internal clock select and divide register39

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	aclk_hevc_pll_sel HEVC AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
13	RO	0x0	reserved
12:8	RW	0x00	aclk_hevc_div_con HEVC AXI clock divider frequency clk=clk_src/(clk_div_con+1)
7	RW	0x0	spi2_pll_sel Control spi2 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
6:0	RW	0x07	spi2_div_con Control SPI2 clock divider frequency clk=clk_src/(div_con+1)

CRU_CLKSEL40_CON
Address: Operational Base + offset (0x0100)
Internal clock select and divide register40

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:12	RW	0x0	hclk_hevc_div_con HEVC AHB clock divider frequency clk=clk_src/(clk_div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x2	spdif_8ch_clk_sel Control SPDIF 8ch clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 12MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	spdif_8ch_pll_div_con Control SPDIF 8ch PLL output divider freuency spdif_div_clk=spdif_div_src/(spdif_pll_div_con+1)

CRU_CLKSEL41_CON
Address: Operational Base + offset (0x0104)
Internal clock select and divide register41

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	spdif_8ch_frac_factor Control SPDIF 8ch fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL42_CON
Address: Operational Base + offset (0x0108)
Internal clock select and divide register42

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	clk_hevc_core_pll_sel HEVC CORE clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	clk_hevc_core_div_con HEVC CORE clock divider frequency clk=clk_src/(clk_div_con+1)
7:6	RW	0x0	clk_hevc_cabac_pll_sel HEVC CABAC clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5	RO	0x0	reserved
4:0	RW	0x00	clk_hevc_cabac_div_con HEVC CABAC clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKGATE0_CON

Address: Operational Base + offset (0x0160)

Internal clock gating control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	clk_acc_efuse_gate_en acc efuse clock disable. When HIGH, disable clock
11	RW	0x0	pd_bus_cpll_clk_gate_en pd_bus clock CPLL path clock disable. When HIGH, disable clock
10	RW	0x0	pd_bus_gpll_clk_gate_en pd_bus clock GPLL path clock disable. When HIGH, disable clock
9	RW	0x0	ddr_gpll_clk_gate_en DDR clock GPLL path clock disable. When HIGH, disable clock
8	RW	0x0	ddr_dpll_clk_gate_en DDR clock DPLL path clock disable. When HIGH, disable clock
7	RW	0x0	aclk_bus_2pmu_gate_en pd_bus AXI clock to pd_pmu clock disable. When HIGH, disable clock
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	pclk_bus_gate_en pd_bus APB clock(pclk_cpu_pre) disable. When HIGH, disable clock
4	RW	0x0	hclk_bus_gate_en pd_bus AHB clock disable. When HIGH, disable clock
3	RW	0x0	aclk_bus_gate_en pd_bus AXI clock disable. When HIGH, disable clock
2	RW	0x0	core_gpll_clk_gate_en CORE clock GPLL path clock disable. When HIGH, disable clock
1	RW	0x0	core_apll_clk_gate_en CORE clock APLL path clock disable. When HIGH, disable clock
0	RO	0x0	reserved

CRU_CLKGATE1_CON
Address: Operational Base + offset (0x0164)
Internal clock gating control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_uart3_frac_src_gate_en UART3 fraction divider source clock disable. When HIGH, disable clock
14	RW	0x0	clk_uart3_src_gate_en UART3 source clock disable. When HIGH, disable clock
13	RW	0x0	clk_uart2_frac_src_gate_en UART2 fraction divider source clock disable. When HIGH, disable clock
12	RW	0x0	clk_uart2_src_gate_en UART2 source clock disable. When HIGH, disable clock
11	RW	0x0	clk_uart1_frac_src_gate_en UART1 fraction divider source clock disable. When HIGH, disable clock
10	RW	0x0	clk_uart1_src_gate_en UART1 source clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	clk_uart0_frac_src_gate_en UART0 fraction divider source clock disable. When HIGH, disable clock
8	RW	0x0	clk_uart0_src_gate_en UART0 source clock disable. When HIGH, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	clk_timer5_gate_en Timer5 clock(clk_timer5) disable. When HIGH, disable clock
4	RW	0x0	clk_timer4_gate_en Timer4 clock(clk_timer4) disable. When HIGH, disable clock
3	RW	0x0	clk_timer3_gate_en Timer3 clock(clk_timer3) disable. When HIGH, disable clock
2	RW	0x0	clk_timer2_gate_en Timer2 clock(clk_timer2) disable. When HIGH, disable clock
1	RW	0x0	clk_timer1_gate_en Timer1 clock(clk_timer1) disable. When HIGH, disable clock
0	RW	0x0	clk_timer0_gate_en Timer0 clock(clk_timer0) disable. When HIGH, disable clock

CRU_CLKGATE2_CON
Address: Operational Base + offset (0x0168)
Internal clock gating control register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	clk_uart4_frac_src_gate_en UART4 fraction divider source clock disable. When HIGH, disable clock
12	RW	0x0	clk_uar4_src_gate_en UART4 source clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
11	RW	0x0	clk_spi2_src_gate_en SPI2 source clock disable. When HIGH, disable clock
10	RW	0x0	clk_spi1_src_gate_en SPI1 source clock disable. When HIGH, disable clock
9	RW	0x0	clk_spi0_src_gate_en SPI0 source clock disable. When HIGH, disable clock
8	RW	0x0	clk_saradc_src_gate_en SARADC source clock disable. When HIGH, disable clock
7	RW	0x0	clk_tsadc_src_gate_en TSADC source clock disable. When HIGH, disable clock
6	RW	0x0	clk_hsadc_src_gate_en Field0000 Abstract When HIGH, disable clock
5	RW	0x0	clk_mac_src_gate_en MAC source clock disable. When HIGH, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_periph_gate_en PERIPH system APB clock(pclk_periph) disable. When HIGH, disable clock
2	RW	0x0	hclk_periph_gate_en PERIPH system AHB clock(hclk_periph) disable. When HIGH, disable clock
1	RW	0x0	aclk_periph_gate_en PERIPH system AXI clock(aclk_periph) disable. When HIGH, disable clock
0	RW	0x0	clk_periph_src_gate_en PERIPH system source clock disable. When HIGH, disable clock

CRU_CLKGATE3_CON
Address: Operational Base + offset (0x016c)
Internal clock gating control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15	RW	0x0	clk_isp_jpeg_gate_en ISP jpeg source clock disable. When HIGH, disable clock
14	RW	0x0	clk_isp_gate_en ISP clock clock disable. When HIGH, disable clock
13	RW	0x0	clk_edp_gate_en eDP clock clock disable. When HIGH, disable clock
12	RW	0x0	clk_edp_24m_gate_en eDP 24M ref clock clock disable. When HIGH, disable clock
11	RW	0x0	aclk_vdpu_src_gate_en VDPU AXI source clock disable. When HIGH, disable clock
10	RW	0x0	hclk_vpu_gate_en VPU AHB source clock disable. When HIGH, disable clock
9	RW	0x0	aclk_vepu_src_gate_en VEPU AXI source clock disable. When HIGH, disable clock
8	RO	0x0	reserved
7	RW	0x0	clk_cif_out_gate_en CIF output clock disable. When HIGH, disable clock
6	RW	0x0	reserved
5	RW	0x0	aclk_rga_src_gate_en RGA AXI souce clock disable. When HIGH, disable clock
4	RW	0x0	clk_rga_core_src_gate_en RGA func souce clock disable. When HIGH, disable clock
3	RW	0x0	dclk_lcdc1_src_gate_en LCDC1 DCLK source clock disable. When HIGH, disable clock
2	RW	0x0	aclk_lcdc1_src_gate_en LCDC1 AXI source clock disable. When HIGH, disable clock
1	RW	0x0	dclk_lcdc0_src_gate_en LCDC0 DCLK source clock disable. When HIGH, disable clock
0	RW	0x0	aclk_lcdc0_src_gate_en LCDC0 AXI source clock disable. When HIGH, disable clock

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CRU_CLKGATE4_CON
Address: Operational Base + offset (0x0170)
Internal clock gating control register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	testclk_gate_en Test output clock disable When HIGH, disable clock
14	RW	0x0	clk_jtag_gate_en JTAG clock disable. When HIGH, disable clock
13	RW	0x0	clk_ddrphy1_gate_en DDRPHY1 clock disable. When HIGH, disable clock
12	RW	0x0	clk_ddrphy0_gate_en DDRPHY0 clock disable. When HIGH, disable clock
11	RW	0x0	clk_tspout_gate_en TSP output clock disable. When HIGH, disable clock
10	RW	0x0	clk_tsp_gate_en TSP clock disable. When HIGH, disable clock
9	RW	0x0	clk_spdif_8ch_gate_en SPDIF 8ch clock disable. When HIGH, disable clock
8	RW	0x0	clk_spdif_8ch_frac_src_gate_en SPDIF 8ch fraction divider source clock disable. When HIGH, disable clock
7	RW	0x0	clk_spdif_8ch_src_gate_en SPDIF 8ch source clock disable. When HIGH, disable clock
6	RW	0x0	clk_spdif_gate_en SPDIF clock disable. When HIGH, disable clock
5	RW	0x0	clk_spdif_frac_src_gate_en SPDIF fraction divider source clock disable. When HIGH, disable clock
4	RW	0x0	clk_spdif_src_gate_en SPDIF source clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	clk_i2s0_gate_en I2S clock disable. When HIGH, disable clock
2	RW	0x0	clk_i2s0_frac_src_gate_en I2S fraction divider source clock disable. When HIGH, disable clock
1	RW	0x0	clk_i2s0_src_gate_en I2S source clock disable. When HIGH, disable clock
0	RW	0x0	clk_i2s0_out_gate_en I2S output clock disable. When HIGH, disable clock

CRU_CLKGATE5_CON
Address: Operational Base + offset (0x0174)
Internal clock gating control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_mipidsi_24m_gate_en mipi dsi 24M clock disable. When HIGH, disable clock
14	RW	0x0	clk_usbphy480m_gate_en usbphy480M clock disable. When HIGH, disable clock
13	RW	0x0	ps2c_clk_gate_en PS2 controlor clock disable. When HIGH, disable clock
12	RW	0x0	hdmi_hdcp_clk_gate_en HDMI HDCP clock disable. When HIGH, disable clock
11	RW	0x0	hdmi_cec_clk_gate_en HDMI CEC clock disable. When HIGH, disable clock
10	RW	0x0	clk_pvtm_gpu_gate_en pd_gpu PVTM clock disable. When HIGH, disable clock
9	RW	0x0	clk_pvtm_core_gate_en pd_core PVTM clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	pclk_pmu_gate_en pd_pmu APB bus clock disable. When HIGH, disable clock
7	RW	0x0	clk_gpu_gate_en gpu clock disable. When HIGH, disable clock
6	RW	0x0	clk_nandc1_gate_en nandc1 clock disable. When HIGH, disable clock
5	RW	0x0	clk_nandc0_gate_en nandc0 clock disable. When HIGH, disable clock
4	RW	0x0	clk_crypto_gate_en crypto clock disable. When HIGH, disable clock
3	RW	0x0	clk_mac_refout_gate_en MAC ref output clock clock disable. When HIGH, disable clock
2	RW	0x0	clk_mac_ref_gate_en MAC ref clock clock disable. When HIGH, disable clock
1	RW	0x0	clk_mac_tx_gate_en MAC tx clock clock disable. When HIGH, disable clock
0	RW	0x0	clk_mac_rx_gate_en MAC rx clock clock disable. When HIGH, disable clock

CRU_CLKGATE6_CON
Address: Operational Base + offset (0x0178)
Internal clock gating control register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_i2c4_gate_en I2C4 APB clock disable. When HIGH, disable clock
14	RW	0x0	pclk_i2c3_gate_en I2C3 APB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
13	RW	0x0	pclk_i2c1_gate_en I2C1 APB clock disable. When HIGH, disable clock
12	RW	0x0	pclk_uart_exp_gate_en UART_exp APB clock disable. When HIGH, disable clock
11	RW	0x0	pclk_uart_gps_gate_en UART_gps APB clock disable. When HIGH, disable clock
10	RO	0x0	reserved
9	RW	0x0	pclk_uart_bb_gate_en UART_bb APB clock disable. When HIGH, disable clock
8	RW	0x0	pclk_uart_bt_gate_en UART_bt APB clock disable. When HIGH, disable clock
7	RW	0x0	pclk_ps2c0_gate_en PS2C0 APB clock disable. When HIGH, disable clock
6	RW	0x0	pclk_spi2_gate_en SPI2 APB clock disable. When HIGH, disable clock
5	RW	0x0	pclk_spi1_gate_en SPI1 APB clock disable. When HIGH, disable clock
4	RW	0x0	pclk_spi0_gate_en SPI0 APB clock disable. When HIGH, disable clock
3	RW	0x0	aclk_dmac_peri_gate_en DMAC peri AXI clock disable. When HIGH, disable clock
2	RW	0x0	aclk_peri_axi_matrix_gate_en Peripheral matrix axi clock disable. When HIGH, disable clock
1	RW	0x0	pclk_peri_axi_matrix_gate_en Peripheral matrix apb clock disable. When HIGH, disable clock
0	RW	0x0	hclk_peri_matrix_gate_en Peripheral matrix ahb clock disable. When HIGH, disable clock

CRU_CLKGATE7_CON
Address: Operational Base + offset (0x017c)
Internal clock gating control register7

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_nand1_gate_en NAND1 AHB clock disable. When HIGH, disable clock
14	RW	0x0	hclk_nand0_gate_en NAND0 AHB clock disable. When HIGH, disable clock
13	RW	0x0	hclk_mmc_peri_gate_en arbiter in peri_ahb_mmc module AHB clock disable. When HIGH, disable clock
12	RW	0x0	hclk_emem_peri_gate_en arbiter in peri_ahb_emem module AHB clock disable. When HIGH, disable clock
11	RW	0x0	aclk_peri_niu_gate_en NIU in peripheral power domain AXI clock disable. When HIGH, disable clock
10	RW	0x0	hclk_peri_ahb_arbi_gate_en AHB arbiter in peripheral power domain AHB clock disable. When HIGH, disable clock
9	RW	0x0	hclk_usb_peri_gate_en USB arbiter AHB clock disable. When HIGH, disable clock
8	RW	0x0	reserved
7	RW	0x0	hclk_host1_gate_en HOST1 AHB clock disable. Field0000 Description
6	RW	0x0	hclk_host0_gate_en HOST0 AHB clock disable. Field0000 Description
5	RW	0x0	pmu_hclk_otg0_gate_en USB OTG PMU AHB clock disable. When HIGH, disable clock
4	RW	0x0	hclk_otg0_gate_en USB OTG AHB clock disable. When HIGH, disable clock
3	RW	0x0	pclk_sim_gate_en SIM APB clock disable. When HIGH, disable clock
2	RW	0x0	pclk_tsadc_gate_en TSADC APB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	pclk_saradc_gate_en SARADC APB clock disable. When HIGH, disable clock
0	RW	0x0	pclk_i2c5_gate_en I2C5 APB clock disable. When HIGH, disable clock

CRU_CLKGATE8_CON
Address: Operational Base + offset (0x0180)
Internal clock gating control register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	aclk_peri_mmu_gate_en PERI_MMU aclk clock disable. When HIGH, disable clock
11	RW	0x0	clk_27m_tsp_gate_en 27M_TSP clock disable. When HIGH, disable clock
10	RW	0x0	clk_hsadc_1_tsp_gate_en HSADC_1_TSP clock disable. When HIGH, disable clock
9	RW	0x0	clk_hsadc_0_tsp_gate_en HSADC_0_TSP clock disable. When HIGH, disable clock
8	RW	0x0	hclk_tsp_gate_en TSP AHB clock disable. When HIGH, disable clock
7	RW	0x0	hclk_hsadc_gate_en HSADC AHB clock disable. When HIGH, disable clock
6	RW	0x0	hclk_emmc_gate_en EMMC AHB clock disable. When HIGH, disable clock
5	RW	0x0	hclk_sdio1_gate_en SDIO1 AHB clock disable. When HIGH, disable clock
4	RW	0x0	hclk_sdio0_gate_en SDIO0 AHB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_sdmmc_gate_en SDMMC AHB clock disable. When HIGH, disable clock
2	RW	0x0	hclk_gps_gate_en GPS hclk clock disable. When HIGH, disable clock
1	RW	0x0	pclk_gmac_gate_en GMAC pclk clock disable. When HIGH, disable clock
0	RW	0x0	aclk_gmac_gate_en GMAC aclk clock disable. When HIGH, disable clock

CRU_CLKGATE9_CON
Address: Operational Base + offset (0x0184)
Internal clock gating control register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:2	RO	0x0	reserved
1	RW	0x0	hclk_video_clock_en VIDEO AHB clock disable. When HIGH, disable clock
0	RW	0x0	aclk_video_gate_en VIDEO AXI clock disable. When HIGH, disable clock

CRU_CLKGATE10_CON
Address: Operational Base + offset (0x0188)
Internal clock gating control register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_publ0_gate_en DDR0 PUBL apb clock disable When HIGH, disable clock

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Bit	Attr	Reset Value	Description
14	RW	0x0	pclk_ddrupctl0_gate_en DDRUPCTL0 apb clock disable When HIGH, disable clock
13	RW	0x0	aclk_strc_sys_gate_en aclk_strc_sys (CPU Structure system) clock disable. When HIGH, disable clock
12	RW	0x0	aclk_dmac_bus_gate_en DMAC_BUS aclk clock disable. When HIGH, disable clock
11	RW	0x0	hclk_spdif_8ch_gate_en hclk_spdif_8ch clock disable. When HIGH, disable clock
10	RW	0x0	hclk_spdif_gate_en hclk_spdif clock disable. When HIGH, disable clock
9	RW	0x0	hclk_rom_gate_en hclk_rom clock disable. When HIGH, disable clock
8	RW	0x0	hclk_i2s_8ch_gate_en hclk_i2s_8ch AHB clock disable. When HIGH, disable clock
7	RW	0x0	clk_intmem2_gate_en intmem2 clock disable. When HIGH, disable clock
6	RW	0x0	clk_intmem1_gate_en intmem1 clock disable. When HIGH, disable clock
5	RW	0x0	clk_intmem0_gate_en intmem0 clock disable. When HIGH, disable clock
4	RW	0x0	aclk_intmem_gate_en intmem axi clock disable. When HIGH, disable clock
3	RW	0x0	pclk_i2c2_gate_en pclk_i2c2 disable. When HIGH, disable clock
2	RW	0x0	pclk_i2c0_gate_en pclk_i2c0 disable. When HIGH, disable clock
1	RW	0x0	pclk_timer_gate_en pclk_timer disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	pclk_pwm_gate_en pclk_pwm disable. When HIGH, disable clock

CRU_CLKGATE11_CON
Address: Operational Base + offset (0x018c)
Internal clock gating control register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	pclk_rkpwm_gate_en pclk_rkpwm disable. When HIGH, disable clock
10	RW	0x0	pclk_efuse_256_gate_en EFUSE256 APB clock disable. When HIGH, disable clock
9	RW	0x0	pclk_uart_dbg_gate_en UART_DBG APB clock disable. When HIGH, disable clock
8	RW	0x0	aclk_ccp_gate_en CCP aclk clock disable. When HIGH, disable clock
7	RW	0x0	hclk_crypto_gate_en CRYPTO sclk clock disable. When HIGH, disable clock
6	RW	0x0	aclk_crypto_gate_en CRYPTO mclk clock disable. When HIGH, disable clock
5	RW	0x0	nclk_ddrupctl1_gate_en DDR Controller PHY clock disable. When HIGH, disable clock
4	RW	0x0	nclk_ddrupctl0_gate_en DDR Controller PHY clock disable. When HIGH, disable clock
3	RW	0x0	pclk_tzpc_gate_en TZPC APB clock disable. When HIGH, disable clock
2	RW	0x0	pclk_efuse_1024_gate_en EFUSE1024 APB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	pclk_publ1_gate_en DDR1 PUBL apb clock disable When HIGH, disable clock
0	RW	0x0	pclk_ddrupctl1_gate_en DDRUPCTL1 apb clock disable When HIGH, disable clock

CRU_CLKGATE12_CON

Address: Operational Base + offset (0x0190)

Internal clock gating control register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	pclk_core_niu_gate_en core NIU APB bus clock disable. When HIGH, disable clock
10	RW	0x0	cs_dbg_clk_gate_en coresight debug clock disable. When HIGH, disable clock
9	RW	0x0	dbg_core_clk_gate_en core debug clock disable. When HIGH, disable clock
8	RW	0x0	dbg_src_clk_gate_en Debug source clock disable. When HIGH, disable clock
7	RW	0x0	atclk_core_gate_en core ATB bus clock disable. When HIGH, disable clock
6	RW	0x0	aclk_mp_gate_en core MP AXI bus clock disable. When HIGH, disable clock
5	RW	0x0	aclk_core_m0_gate_en CORE m0 AXI bus clock disable. When HIGH, disable clock
4	RW	0x0	l2_ram_clk_gate_en L2 RAM clock disable. When HIGH, disable clock
3	RW	0x0	core3_clk_gate_en core3 clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	core2_clk_gate_en core2 clock disable. When HIGH, disable clock
1	RW	0x0	coer1_clk_gate_en core1 clock disable. When HIGH, disable clock
0	RW	0x0	core0_clk_gate_en core0 clock disable. When HIGH, disable clock

CRU_CLKGATE13_CON
Address: Operational Base + offset (0x0194)
Internal clock gating control register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_hevc_core_gate_en HEVC CORE clock disable. When HIGH, disable clock
14	RW	0x0	clk_hevc_cabac_gate_en HEVC cabac clock disable. When HIGH, disable clock
13	RW	0x0	aclk_hevc_gate_en HEVC AXI clock disable. When HIGH, disable clock
12	RW	0x0	clk_wifi_gate_en wifi/gps/bt 3in1 16.384M clock disable. When HIGH, disable clock
11	RW	0x0	clk_lcdc_pwm1_gate_en lcdc_pwm1 clock disable. When HIGH, disable clock
10	RW	0x0	clk_lcdc_pwm0_gate_en lcdc_pwm0 clock disable. When HIGH, disable clock
9	RW	0x0	reserved
8	RW	0x0	clk_c2c_host_gate_en C2C HOST clock disable. When HIGH, disable clock
7	RW	0x0	clk_otg_adp_gate_en OTG adp clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
6	RW	0x0	clk_otgphy2_gate_en OTGPHY2 clock(clk_otgphy2) disable. When HIGH, disable clock
5	RW	0x0	clk_otgphy1_gate_en OTGPHY1 clock(clk_otgphy1) disable. When HIGH, disable clock
4	RW	0x0	clk_otgphy0_gate_en OTGPHY0 clock(clk_otgphy0) disable. When HIGH, disable clock
3	RW	0x0	clk_emmc_src_gate_en EMMC source clock disable. When HIGH, disable clock
2	RW	0x0	clk_sdio1_src_gate_en SDIO1 source clock disable. When HIGH, disable clock
1	RW	0x0	clk_sdio0_src_gate_en SDIO0 source clock disable. When HIGH, disable clock
0	RW	0x0	clk_mmc0_src_gate_en SDMMC0 source clock disable. When HIGH, disable clock

CRU_CLKGATE14_CON
Address: Operational Base + offset (0x0198)
Internal clock gating control register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	pclk_alive_niu_gate_en ALIVE_NIU pclk disable When HIGH, disable clock
11	RW	0x0	pclk_grf_gate_en GRF pclk disable When HIGH, disable clock
10:9	RO	0x0	reserved
8	RW	0x0	pclk_gpio8_gate_en GPIO8 pclk disable When HIGH, disable clock

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Bit	Attr	Reset Value	Description
7	RW	0x0	pclk_gpio7_gate_en GPIO7 pclk disable When HIGH, disable clock
6	RW	0x0	pclk_gpio6_gate_en GPIO6 pclk disable When HIGH, disable clock
5	RW	0x0	pclk_gpio5_gate_en GPIO5 pclk disable When HIGH, disable clock
4	RW	0x0	pclk_gpio4_gate_en GPIO4 pclk disable When HIGH, disable clock
3	RW	0x0	pclk_gpio3_gate_en GPIO3 pclk disable When HIGH, disable clock
2	RW	0x0	pclk_gpio2_gate_en GPIO2 pclk disable When HIGH, disable clock
1	RW	0x0	pclk_gpio1_gate_en GPIO1 pclk disable When HIGH, disable clock
0	RO	0x0	reserved

CRU_CLKGATE15_CON
Address: Operational Base + offset (0x019c)
Internal clock gating control register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_vip_gate_en VIP hclk disable When HIGH, disable clock
14	RW	0x0	aclk_vip_gate_en VIP aclk disable When HIGH, disable clock
13	RW	0x0	aclk_vio2_noc_gate_en VIO2_NOC aclk disable When HIGH, disable clock
12	RW	0x0	aclk_vio1_noc_gate_en VIO1_NOC aclk disable When HIGH, disable clock

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Bit	Attr	Reset Value	Description
11	RW	0x0	aclk_vio0_noc_gate_en VIO0_NOC aclk disable When HIGH, disable clock
10	RW	0x0	hclk_vio_noc_gate_en VIO_NOC hclk disable When HIGH, disable clock
9	RW	0x0	hclk_vio_ahb_arbi_gate_en VIO_AHB_ARBI hclk disable When HIGH, disable clock
8	RW	0x0	hclk_lcdc1_gate_en LCDC1 hclk disable When HIGH, disable clock
7	RW	0x0	aclk_lcdc1_gate_en LCDC1 aclk disable When HIGH, disable clock
6	RW	0x0	hclk_lcdc0_gate_en LCDC0 hclk disable When HIGH, disable clock
5	RW	0x0	aclk_lcdc0_gate_en LCDC0 aclk disable When HIGH, disable clock
4	RW	0x0	aclk_lcdc_iep_gate_en LCDC_IEP aclk disable When HIGH, disable clock
3	RW	0x0	hclk_iep_gate_en IEP hclk disable When HIGH, disable clock
2	RW	0x0	aclk_iep_gate_en IEP aclk disable When HIGH, disable clock
1	RW	0x0	hclk_rga_gate_en RGA hclk disable When HIGH, disable clock
0	RW	0x0	aclk_rga_gate_en RGA aclk disable When HIGH, disable clock

CRU_CLKGATE16_CON

Address: Operational Base + offset (0x01a0)

Internal clock gating control register16

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	pclk_vio2_h2p_gate_en VIO2_H2P pclk disable When HIGH, disable clock
10	RW	0x0	hclk_vio2_h2p_gate_en VIO2_H2P hclk disable When HIGH, disable clock
9	RW	0x0	pclk_hdmi_ctrl_gate_en HDMI_CTRL pclk disable When HIGH, disable clock
8	RW	0x0	pclk_edp_ctrl_gate_en EDP_CTRL pclk disable When HIGH, disable clock
7	RW	0x0	pclk_lvds_phy_gate_en LVDS_PHY pclk disable When HIGH, disable clock
6	RW	0x0	pclk_mipi_csi_gate_en MIPI_CSI pclk disable When HIGH, disable clock
5	RW	0x0	pclk_mipi_dsi1_gate_en MIPI_DSI1 pclk disable When HIGH, disable clock
4	RW	0x0	pclk_mipi_dsi0_gate_en MIPI_DSI0 pclk disable When HIGH, disable clock
3	RW	0x0	pclkin_isp_gate_en ISP pclkin disable When HIGH, disable clock
2	RW	0x0	aclk_isp_gate_en ISP aclk disable When HIGH, disable clock
1	RW	0x0	hclk_isp_gate_en ISP hclk disable When HIGH, disable clock
0	RW	0x0	pclkin_vip_gate_en VIP pclkin disable When HIGH, disable clock

CRU_CLKGATE17_CON
Address: Operational Base + offset (0x01a4)

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Internal clock gating control register17

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:5	RO	0x0	reserved
4	RW	0x0	pclk_gpio0_gate_en GPIO0 pclk disable When HIGH, disable clock
3	RO	0x0	Reserved
2	RW	0x0	pclk_pmu_noc_gate_en PMU_NOC pclk disable When HIGH, disable clock
1	RW	0x0	pclk_intmem1_gate_en INTMEM1 pclk disable When HIGH, disable clock
0	RW	0x0	pclk_pmu_gate_en PMU pclk disable When HIGH, disable clock

CRU_CLKGATE18_CON

Address: Operational Base + offset (0x01a8)

Internal clock gating control register18

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:1	RO	0x0	reserved
0	RW	0x0	aclk_gpu_gate_en GPU aclk disable When HIGH, disable clock

CRU_GLB_SRST_FST_VALUE

Address: Operational Base + offset (0x01b0)

The first global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_fst_value The first global software reset config value If config 0xfdb9, it will generate first global software reset.

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CRU_GLB_SRST_SND_VALUE
Address: Operational Base + offset (0x01b4)
The second global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_snd_value The second global software reset config value If config 0xeca8, it will generate second global software reset.

CRU_SOFTRST0_CON
Address: Operational Base + offset (0x01b8)
Internal software reset control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	core3_dbg_srstn_req Core3 CPU debug software reset request. When HIGH, reset relative logic
14	RW	0x0	core2_dbg_srstn_req Core2 CPU debug software reset request. When HIGH, reset relative logic
13	RW	0x0	core1_dbg_srstn_req Core1 CPU debug software reset request. When HIGH, reset relative logic
12	RW	0x0	core0_dbg_srstn_req Core0 CPU debug software reset request. When HIGH, reset relative logic
11	RW	0x0	topdbg_srstn_req CPU top debug software reset request. When HIGH, reset relative logic
10	RW	0x0	l2c_srstn_req L2 controller software reset request. When HIGH, reset relative logic
9	RW	0x0	pd_bus_str_sys_asrstn_req PD BUS NOC AXI software reset request. When HIGH, reset relative logic
8	RW	0x0	pd_core_str_sys_asrstn_req PD CORE NOC AXI software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
7	RW	0x0	core3_po_srstn_req Core3 CPU PO software reset request. When HIGH, reset relative logic
6	RW	0x0	core2_po_srstn_req Core2 CPU PO software reset request. When HIGH, reset relative logic
5	RW	0x0	core1_po_srstn_req Core1 CPU PO software reset request. When HIGH, reset relative logic
4	R/WSC	0x0	core0_po_srstn_req Core0 CPU PO software reset request. When HIGH, reset relative logic
3	RW	0x0	core3_srstn_req Core3 CPU software reset request. When HIGH, reset relative logic
2	RW	0x0	core2_srstn_req Core2 CPU software reset request. When HIGH, reset relative logic
1	RW	0x0	core1_srstn_req Core1 CPU software reset request. When HIGH, reset relative logic
0	R/WSC	0x0	core0_srstn_req Core0 CPU software reset request. When HIGH, reset relative logic

CRU_SOFTRST1_CON
Address: Operational Base + offset (0x01bc)
Internal software reset control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	efuse_psrstn_req EFUSE APB software reset request. When HIGH, reset relative logic
14	RW	0x0	timer5_srstn_req Timer5 software reset request. When HIGH, reset relative logic
13	RW	0x0	timer4_srstn_req Timer4 software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
12	RW	0x0	timer3_srstn_req Timer3 software reset request. When HIGH, reset relative logic
11	RW	0x0	timer2_srstn_req Timer2 software reset request. When HIGH, reset relative logic
10	RW	0x0	timer1_srstn_req Timer1 software reset request. When HIGH, reset relative logic
9	RW	0x0	timer0_srstn_req Timer0 software reset request. When HIGH, reset relative logic
8	RW	0x0	spdif_srstn_req SPDIF software reset request. When HIGH, reset relative logic
7	RW	0x0	i2s_srstn_req I2S software reset request. When HIGH, reset relative logic
6	RW	0x0	timer_psrstn_req Timer APB software reset request. When HIGH, reset relative logic
5	RW	0x0	spdif_8ch_srstn_req SPDIF 8ch software reset request. When HIGH, reset relative logic
4	RW	0x0	rom_srstn_req ROM software reset request. When HIGH, reset relative logic
3	RW	0x0	intmem_srstn_req Internal memory software reset request. When HIGH, reset relative logic
2	RW	0x0	dma1_srstn_req DMA1 software reset request. When HIGH, reset relative logic
1	RW	0x0	efuse_256bit_psrstn_req 256bit EFUSE APB software reset request. When HIGH, reset relative logic
0	RW	0x0	pd_bus_ahb_arbitor_srstn_req pd_bus ahb arbitor software reset request. pd_cpu AHB arbitor reset control When HIGH, reset relative logic

CRU_SOFTRST2_CON
Address: Operational Base + offset (0x01c0)
Internal software reset control register2

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	i2c5_srstn_req I2C5 software reset request. When HIGH, reset relative logic
14	RW	0x0	i2c4_srstn_req I2C4 software reset request. When HIGH, reset relative logic
13	RW	0x0	i2c3_srstn_req I2C3 software reset request. When HIGH, reset relative logic
12	RW	0x0	i2c2_srstn_req I2C2 software reset request. When HIGH, reset relative logic
11	RW	0x0	i2c1_srstn_req I2C1 software reset request. When HIGH, reset relative logic
10	RW	0x0	i2c0_srstn_req I2C0 software reset request. When HIGH, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	gpio8_srstn_req GPIO8 software reset request. When HIGH, reset relative logic
7	RW	0x0	gpio7_srstn_req GPIO7 software reset request. When HIGH, reset relative logic
6	RW	0x0	gpio6_srstn_req GPIO6 software reset request. When HIGH, reset relative logic
5	RW	0x0	gpio5_srstn_req GPIO5 software reset request. When HIGH, reset relative logic
4	RW	0x0	gpio4_srstn_req GPIO4 software reset request. When HIGH, reset relative logic
3	RW	0x0	gpio3_srstn_req GPIO3 software reset request. When HIGH, reset relative logic
2	RW	0x0	gpio2_srstn_req GPIO2 software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
1	RW	0x0	gpio1_srstn_req GPIO1 software reset request. When HIGH, reset relative logic
0	RW	0x0	gpio0_srstn_req GPIO0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST3_CON
Address: Operational Base + offset (0x01c4)
Internal software reset control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	usb_peri_srstn_req USB PERIPH software reset request. When HIGH, reset relative logic
14	RW	0x0	emem_peri_srstn_req EMEM ahb bus software reset request. When HIGH, reset relative logic
13	RW	0x0	reserved
12	RW	0x0	periph_niu_srstn_req PERIPH NIU software reset request. When HIGH, reset relative logic
11	RW	0x0	periphsys_psrstn_req PERIPH APB software reset request. pd_peri bus matrix apb softreset When HIGH, reset relative logic
10	RW	0x0	periphsys_hsrstn_req PERIPH AHB software reset request. pd_peri bus matrix ahb softreset When HIGH, reset relative logic
9	RW	0x0	periphsys_asrstn_req PERIPH AXI software reset request. pd_peri bus matrix axi softreset When HIGH, reset relative logic
8	RW	0x0	pmu_srstn_req PMU software reset request. When HIGH, reset relative logic
7	RW	0x0	grf_srstn_req GRF software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
6	RW	0x0	pmu_psrstn_req PMU APB bus software reset request. When HIGH, reset relative logic
5	RW	0x0	tpiu_atsrstn_req TPIU ATB software reset request. When HIGH, reset relative logic
4	RW	0x0	dap_sys_srstn_req DAP system software reset request. When HIGH, reset relative logic
3	RW	0x0	dap_srstn_req DAP software reset request. When HIGH, reset relative logic
2	RW	0x0	periph_mmu_srstn_req PERIPH MMU software reset request. When HIGH, reset relative logic
1	RW	0x0	mmc_peri_srstn_req pd_peri mmc AHB bus software reset request. emmc, sdio, sdmmc AHB arbitor reset control When HIGH, reset relative logic
0	RW	0x0	pwm_srstn_req PWM software reset request. When HIGH, reset relative logic

CRU_SOFTRST4_CON
Address: Operational Base + offset (0x01c8)
Internal software reset control register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	nandc1_srstn_req NANDC1 software reset request. When HIGH, reset relative logic
13	RW	0x0	nandc0_srstn_req NANDC0 software reset request. When HIGH, reset relative logic
12	RW	0x0	hsadc_srstn_req HSADC software reset request. When HIGH, reset relative logic
11:9	RW	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	usb_host0_srstn_req USB HOST0 AHB software reset request. When HIGH, reset relative logic
7	RW	0x0	ccp_srstn_req CCP software reset request. When HIGH, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	rk_pwm_srstn_req RK_PWM software reset request. When HIGH, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	gps_srstn_req GPS software reset request. When HIGH, reset relative logic
2	RW	0x0	mac_srstn_req MAC software reset request. When HIGH, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	dma2_srstn_req DMA2 software reset request. When HIGH, reset relative logic

CRU_SOFTRST5_CON
Address: Operational Base + offset (0x01cc)
Internal software reset control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	RW	0x0	pd_pmu_niu_psrstn_req pd_pmu niu APB software reset request. When HIGH, reset relative logic
9	RW	0x0	pd_pmu_intmem_psrstn_req pd_pmu internal memory apb software reset request. When HIGH, reset relative logic
8	RW	0x0	pd_alive_niu_psrstn_req pd_alive niu APB software reset request. When HIGH, reset relative logic
7	RW	0x0	saradc_srstn_req SARADC software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
6	RO	0x0	reserved
5	RW	0x0	spi2_srstn_req SPI2 software reset request. When HIGH, reset relative logic
4	RW	0x0	spi1_srstn_req SPI1 software reset request. When HIGH, reset relative logic
3	RW	0x0	spi0_srstn_req SPI0 software reset request. When HIGH, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	tzpc_srstn_req TZPC software reset request. When HIGH, reset relative logic

CRU_SOFTRST6_CON
Address: Operational Base + offset (0x01d0)
Internal software reset control register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	edp_srstn_req eDP software reset request. When HIGH, reset relative logic
14	RW	0x0	isp_srstn_req ISP software reset request. When HIGH, reset relative logic
13	RW	0x0	rga_hsrstn_req RGA AHB software reset request. When HIGH, reset relative logic
12	RW	0x0	rga_asrstn_req RGA AXI software reset request. When HIGH, reset relative logic
11	RW	0x0	iep_hsrstn_req IEP AHB software reset request. When HIGH, reset relative logic
10	RW	0x0	iep_asrstn_req IEP AXI software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
9	RW	0x0	rga_core_srstn_req RGA func software reset request. When HIGH, reset relative logic
8	RW	0x0	vip_srstn_req VIP software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
7	RW	0x0	vio1_niu_asrstn_req VIO1 NIU AXI software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
6	RW	0x0	lcdc0_dsrstn_req LCDC0 DCLK software reset request. When HIGH, reset relative logic
5	RW	0x0	lcdc0_hsrstn_req LCDC0 AHB software reset request. When HIGH, reset relative logic
4	RW	0x0	lcdc0_asrstn_req LCDC0 AXI software reset request. When HIGH, reset relative logic
3	RW	0x0	vio_niu_hsrstn_req VIO NIU AHB software reset request. When HIGH, reset relative logic
2	RW	0x0	vio0_niu_asrstn_req VIO0 NIU AXI software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
1	RW	0x0	rga_niu_asrstn_req RGA NIU AXI software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
0	RW	0x0	vio_arbi_hsrstn_req VIO arbitor AHB software reset request. When HIGH, reset relative logic

CRU_SOFTRST7_CON

Address: Operational Base + offset (0x01d4)

Internal software reset control register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13	RW	0x0	gpu_pvtm_srstn_req gpu pvtm software reset request. When HIGH, reset relative logic
12	RW	0x0	core_pvtm_srstn_req core pvtm software reset request. When HIGH, reset relative logic
11:10	RO	0x0	reserved
9	RW	0x0	hdmi_srstn_req HDMI software reset request. When HIGH, reset relative logic
8	RW	0x0	gpu_srstn_req GPU core software reset request. When HIGH, reset relative logic
7	RW	0x0	lvds_con_srstn_req LVDS controller software reset request. When HIGH, reset relative logic
6	RW	0x0	lvds_phy_psrstn_req LVDS PHY APB software reset request. When HIGH, reset relative logic
5	RW	0x0	mipicsi_psrstn_req MIPi CSI APB software reset request. When HIGH, reset relative logic
4	RW	0x0	mipidsi1_psrstn_req MIPi DSI1 APB software reset request. When HIGH, reset relative logic
3	RW	0x0	mipidsi0_psrstn_req MIPi DSI0 APB software reset request. When HIGH, reset relative logic
2	RW	0x0	vio_h2p_hsrstn_req VIO ahb to apb bridge AHB software reset request. When HIGH, reset relative logic
1	RW	0x0	vcodec_hsrstn_req VCODEC AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	vcodec_asrstn_req VCODEC AXI software reset request. When HIGH, reset relative logic

CRU_SOFTRST8_CON
Address: Operational Base + offset (0x01d8)
Internal software reset control register8

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	acc_efuse_srstn_req acc efuse software reset request. When HIGH, reset relative logic
13	RW	0x0	usb_adp_srstn_req OTG adp clock software reset request. When HIGH, reset relative logic
12	RW	0x0	usbhost1c_srstn_req USBHOST1 controller software reset request. When HIGH, reset relative logic
11	RW	0x0	usbhost1phy_srstn_req USBHOST1 PHY software reset request. When HIGH, reset relative logic
10	RW	0x0	usbhost1_hsrstn_req USBHOST1 AHB BUS software reset request. When HIGH, reset relative logic
9	RW	0x0	usbhost0c_srstn_req USBHOST0 controller software reset request. When HIGH, reset relative logic
8	RW	0x0	usbhost0phy_srstn_req USBHOST0 PHY software reset request. When HIGH, reset relative logic
7	RW	0x0	usbhost0_hsrstn_req USBHOST0 AHB BUS software reset request. When HIGH, reset relative logic
6	RW	0x0	usbotgc_srstn_req USBOTG controller software reset request. When HIGH, reset relative logic
5	RW	0x0	usbotgphy_srstn_req USBOTG PHY software reset request. When HIGH, reset relative logic
4	RW	0x0	usbotg_hsrstn_req USBOTG AHB BUS software reset request. When HIGH, reset relative logic
3	RW	0x0	emmc_srstn_req EMMC software reset request. When HIGH, reset relative logic
2	RW	0x0	sdio1_srstn_req SDIO1 software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
1	RW	0x0	sdio0_srstn_req SDIO0 software reset request. When HIGH, reset relative logic
0	RW	0x0	mmc0_srstn_req SDMMC0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST9_CON
Address: Operational Base + offset (0x01dc)
Internal software reset control register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	tsadc_psrstn_req TSADC APB software reset request. When HIGH, reset relative logic
14:11	RO	0x0	reserved
10	RW	0x0	hevc_srstn_req HEVC software reset request. When HIGH, reset relative logic
9	RW	0x0	rga_h2p_brg_srstn_req RGA AHB to APB bridge software reset request. When HIGH, reset relative logic
8	RW	0x0	vio1_h2p_brg_srstn_req VIO1 AHB to APB bridge software reset request. When HIGH, reset relative logic
7	RW	0x0	vio0_h2p_brg_srstn_req VIO0 AHB to APB bridge software reset request. When HIGH, reset relative logic
6	RW	0x0	lcdcpwm1_srstn_req lcdc_pwm1 software reset request. When HIGH, reset relative logic
5	RW	0x0	lcdcpwm0_srstn_req lcdc_pwm0 software reset request. When HIGH, reset relative logic
4	RW	0x0	gic_srstn_req GIC software reset request. When HIGH, reset relative logic
3	RW	0x0	pd_core_mp_axi_srstn_req pd_croe periph axi software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
2	RW	0x0	pd_core_apb_noc_srstn_req pd_core APB software reset request. When HIGH, reset relative logic
1	RW	0x0	pd_core_ahb_noc_srstn_req PD_CORE AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	coresight_srstn_req coresight software reset request. When HIGH, reset relative logic

CRU_SOFTRST10_CON
Address: Operational Base + offset (0x01e0)
Internal software reset control register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	c2c_host_srstn_req c2c host clk domain software reset request. When HIGH, reset relative logic
14	RW	0x0	crypto_srstn_req crypto working clk domain software reset request. When HIGH, reset relative logic
13:12	RO	0x0	reserved
11	RW	0x0	ddrmsch1_srstn_req DDR1 memory scheduler software reset request. When HIGH, reset relative logic
10	RW	0x0	ddrmsch0_srstn_req DDR0 memory scheduler software reset request. When HIGH, reset relative logic
9	RW	0x0	ddrphy1_ctl_srstn_req DDR1 PUB software reset request. When HIGH, reset relative logic
8	RW	0x0	ddrctrl1_psrstn_req DDR controller1 APB software reset request. When HIGH, reset relative logic
7	RW	0x0	ddrctrl1_srstn_req DDR controller1 software reset request. When HIGH, reset relative logic
6	RW	0x0	ddrphy1_psrstn_req DDR PHY1 APB software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
5	RW	0x0	ddrphy1_srstn_req DDR PHY1 software reset request. When HIGH, reset relative logic
4	RW	0x0	ddrphy0_ctl_srstn_req DDR0 PUB software reset request. When HIGH, reset relative logic
3	RW	0x0	ddrctrl0_psrstn_req DDR controller0 APB software reset request. When HIGH, reset relative logic
2	RW	0x0	ddrctrl0_srstn_req DDR controller0 software reset request. When HIGH, reset relative logic
1	RW	0x0	ddrphy0_psrstn_req DDR PHY0 APB software reset request. When HIGH, reset relative logic
0	RW	0x0	ddrphy0_srstn_req DDR PHY0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST11_CON
Address: Operational Base + offset (0x01e4)
Internal software reset control register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	tsp_27m_srstn_req TSP 27M lock domain software reset request. When HIGH, reset relative logic
14	RW	0x0	tsp_clkin1_srstn_req TSP clockin1 software reset request. When HIGH, reset relative logic
13	RW	0x0	tsp_clkin0_srstn_req TSP clockin 0 software reset request. When HIGH, reset relative logic
12	RW	0x0	tsp_srstn_req tsp software reset request. When HIGH, reset relative logic
11	RW	0x0	ps2c_srstn_req ps2 controlor software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
10	RW	0x0	simc_srstn_req cim card controlor software reset request. When HIGH, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	uart4_srstn_req UART4 software reset request. When HIGH, reset relative logic
6	RW	0x0	uart3_srstn_req UART3 software reset request. When HIGH, reset relative logic
5	RW	0x0	uart2_srstn_req UART2 software reset request. When HIGH, reset relative logic
4	RW	0x0	uart1_srstn_req UART1 software reset request. When HIGH, reset relative logic
3	RW	0x0	uart0_srstn_req UART0 software reset request. When HIGH, reset relative logic
2	RW	0x0	lcdc1_dsrstn_req LCDC1 DCLK software reset request. When HIGH, reset relative logic
1	RW	0x0	lcdc1_hsrstn_req LCDC1 AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	lcdc1_asrstn_req LCDC1 AXI software reset request. When HIGH, reset relative logic

CRU_MISC_CON
Address: Operational Base + offset (0x01e8)
SCU control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	testclk_sel Output clock selection for test 4'b0000: aclk_periph 4'b0001: clk_core 4'b0010: aclk_vio0 4'b0011: clk_ddrphy 4'b0100: aclk_vcodec 4'b0101: aclk_gpu 4'b0110: clk_rga_core 4'b0111: aclk_cpu 4'b1000: 24MHz 4'b1001: 27MHz 4'b1010: 32KHz 4'b1011: clk_wifi(16.368MHz) 4'b1100: dclk_lcdc0 4'b1101: dclk_lcdc1 4'b1110: clk_isp_jpeg 4'b1111: clk_isp
7:0	RO	0x0	reserved

CRU_GLB_CNT_TH
Address: Operational Base + offset (0x01ec)
global reset wait counter threshold

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x064	glb_rst_cnt_th Global soft reset counter threshold

CRU_GLB_RST_CON
Address: Operational Base + offset (0x01f0)
global reset trigger select

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x0	pmu_glb_srst_ctrl pmu reset by global soft reset select 2'b00: pmu reset by first global soft reset 2'b01: pmu reset by second global soft reset 2'b10: pmu not reset by any global soft reset
1	RW	0x0	wdt_glb_srst_ctrl watch_dog trigger global soft reset select 1'b0: watch_dog trigger second global reset 1'b1: watch_dog trigger first global reset

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Bit	Attr	Reset Value	Description
0	RW	0x0	tsadc_glb_srst_ctrl TSADC trigger global soft reset select 1'b0: tsadc trigger second global reset 1'b1: tsadc trigger first global reset

CRU_GLB_RST_ST
Address: Operational Base + offset (0x01f8)
global reset status

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	W1C	0x0	snd_glb_wdt_rst_st second global watch_dog triggered reset flag 1'b0: last hot reset is not second global watch_dog triggered reset 1'b1: last hot reset is second global watch_dog triggered reset
4	W1C	0x0	fst_glb_wdt_rst_st first global watch_dog triggered reset flag 1'b0: last hot reset is not first global watch_dog triggered reset 1'b1: last hot reset is first global watch_dog triggered reset
3	W1C	0x0	snd_glb_tsadc_rst_st second global TSADC triggered reset flag 1'b0: last hot reset is not second global TSADC triggered reset 1'b1: last hot reset is second global TSADC triggered reset
2	W1C	0x0	fst_glb_tsadc_rst_st first global TSADC triggered reset flag 1'b0: last hot reset is not first global TSADC triggered reset 1'b1: last hot reset is first global TSADC triggered reset
1	W1C	0x0	snd_glb_rst_st second global rst flag 1'b0: last hot reset is not second global rst 1'b1: last hot reset is second global rst
0	W1C	0x0	fst_glb_rst_st first global rst flag 1'b0: last hot reset is not first global rst 1'b1: last hot reset is first global rst

CRU_SDMMC_CON0*
Address: Operational Base + offset (0x0200)
sdmmc control0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	sdmmc_drv_sel sdmmc drive select sdmmc drive select
10:3	WO	0x00	sdmmc_drv_delaynum sdmmc drive delay number sdmmc drive delay number
2:1	WO	0x1	sdmmc_drv_degree sdmmc drive degree sdmmc drive degree
0	WO	0x0	sdmmc_init_state sdmmc initial state sdmmc initial state

CRU_SDMMC_CON1*
Address: Operational Base + offset (0x0204)
sdmmc control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	sdmmc_sample_sel sdmmc sample select sdmmc sample select
9:2	WO	0x00	sdmmc_sample_delaynum sdmmc sample delay number sdmmc sample delay number
1:0	WO	0x0	sdmmc_sample_degree sdmmc sample degree sdmmc sample degree

CRU_SDIO0_CON0*
Address: Operational Base + offset (0x0208)
sdio0 control0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	sdio0_drv_sel sdio0 drive select sdio0 drive select
10:3	WO	0x00	sdio0_drv_delaynum sdio0 drive delay number sdio0 drive delay number
2:1	WO	0x1	sdio0_drv_degree sdio0 drive degree sdio0 drive degree
0	WO	0x0	sdio0_init_state sdio0 initial state sdio0 initial state

CRU_SDIO0_CON1*
Address: Operational Base + offset (0x020c)
sdio0 control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	sdio0_sample_sel sdio0 sample select sdio0 sample select
9:2	WO	0x00	sdio0_sample_delaynum sdio0 sample delay number sdio0 sample delay number
1:0	WO	0x0	sdio0_sample_degree sdio0 sample degree sdio0 sample degree

CRU_SDIO1_CON0*
Address: Operational Base + offset (0x0210)
sdio1 control0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	sdio1_drv_sel sdio1 drive select sdio1 drive select
10:3	WO	0x00	sdio1_drv_delaynum sdio1 drive delay number sdio1 drive delay number
2:1	WO	0x1	sdio1_drv_degree sdio1 drive degree sdio1 drive degree
0	WO	0x0	sdio1_init_state sdio1 initial state sdio1 initial state

CRU_SDIO1_CON1*
Address: Operational Base + offset (0x0214)
sdio1 control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	sdio1_sample_sel sdio1 sample select sdio1 sample select
9:2	WO	0x00	sdio1_sample_delaynum sdio1 sample delay number sdio1 sample delay number
1:0	WO	0x0	sdio1_sample_degree sdio1 sample degree sdio1 sample degree

CRU_EMMC_CON0*
Address: Operational Base + offset (0x0218)
emmc control0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	emmc_drv_sel emmc drive select emmc drive select
10:3	WO	0x00	emmc_drv_delaynum emmc drive delay number emmc drive delay number
2:1	WO	0x1	emmc_drv_degree emmc drive degree emmc drive degree
0	WO	0x0	emmc_init_state emmc initial state emmc initial state

CRU_EMMC_CON1*
Address: Operational Base + offset (0x021c)
emmc control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	emmc_sample_sel emmc sample select emmc sample select
9:2	WO	0x00	emmc_sample_delaynum emmc sample delay number emmc sample delay number
1:0	WO	0x0	emmc_sample_degree emmc sample degree emmc sample degree

**Notes: CRU_SDMMC_CON0/1, CRU_SDIO1_CON0/1, CRU_SDIO0_CON0/1, CRU_EMMC_CON0/1, detail description please refer to chapter1 of part3 Mobile Storage Host Controller 1.6.10.*

3.7 Timing Diagram

Power on reset timing is shown as follow:

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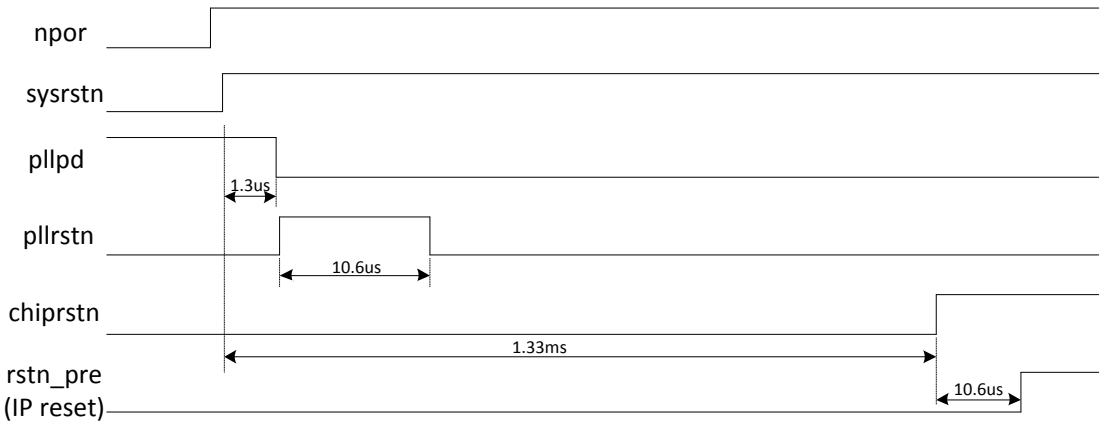

Fig. 3-4 Chip Power On Reset Timing Diagram

Npor is hardware reset signal from out-chip and power-off mode wakeup reset from PMU, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the power down signal (pllpd) must be high when reset, and maintains high for more then 1us when sysrstn de-active. Then PLL reset signals (pllrstn) are asserted for about 10.6us, and PLLs start to lock when pllrstn de-assert, and consume about 1330us to lock. So the system will wait about 1330us, then de-active reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 256 cycles (10.7us) to de-active signal rstn_pre, which is used to generate power on reset of all IP.

3.8 Application Notes

3.8.1 PLL usage

PLL output frequency configuration

The output frequency Fout is related to the input frequency Fin by:

Fout = ((Fin /NR) * NF)/ NO

Fout is clock output of PLL, and Fin is clock input of PLL from external oscillators (24MHz). Another, other factors such as NF, NR, NO can be configured by programming CRU_APLL_CONi, CRU_DPLL_CONi, CRU_CPLL_CONi and CRU_GPLL_CONi registers (i=0,1,2), and their value will affect Fout as follows.

(1) CLKR: A 6-bit bus that selects the values 1-64 for the reference divider (NR)

NR = CLKR[5:0] + 1

Example:

/1 pgm 000000
/4 pgm 000011
/8 pgm 000111

(2) CLKF: A 13-bit bus that selects the values 1-4096 for the PLL multiplication factor (NF)

NF = CLKF[12:0] + 1

Example:

X1 pgm 0000000000000
X2 pgm 0000000000001
X4096 pgm 0111111111111

(3) CLKOD: A 4-bit bus that selects the value1,2-16(even only) for the PLL post VCO divider (NO)

NO = CLKOD[3:0] + 1

Example:

/1 pgm 0000
/2 pgm 0001
/4 pgm 0011
/8 pgm 0111

BWADJ: A 12-bit bus that selects the values 1-4096 for the bandwidth divider (NB)

NB = BWADJ[11:0] + 1

Example:

/1 pgm 000000000000

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/4 pgm 000000000011
/8 pgm 000000000111
The recommended setting of NB: NB = NF / 2.

PLL frequency range requirement
If different CLKR, CLKF and CLKOD configuration value cause internal out of range, unpredicted result will be caused.
Fin value range requirement: 269kHz – 5000MHz
Fref = Fin/NR value range requirement: 269kHz – 5000MHz
Fvco = (Fin/NR)*NF value range requirement: 440MHz – 5000MHz
Fout = ((Fin/NR)*NF)/NO value range requirement: 27.5MHz – 5000MHz

PLL setting consideration
Optimization of the PLL settings for jitter < +/- 2.5% of the output period/sq rt(NO) require running the VCO at maximum frequency and dividing down using the NO divider to get the required Fout, i.e. maximum NO.
Optimization for minimum power (Fvco/1100MHz * 3.3 mA) requires setting the VCO frequency at the minimum frequency and using the lowest NO setting.
These two values, minimum jitter or minimum power will determine your choice of settings.
A larger value of input divider NR gives a longer lock time, and higher long term as well as period jitter. It is better to use a lower value of NR where possible.

3.8.2 PLL frequency change method

When the PLL settings are changed, it has to reset PLL by programming registers CRU_APLL_CON3, CRU_DPLL_CON3, CRU_CPLL_CON3, CRU_GPLL_CON3, CRU_NPLL_CON3, and reserve at least 5us after valid settings, referring to the following figure.

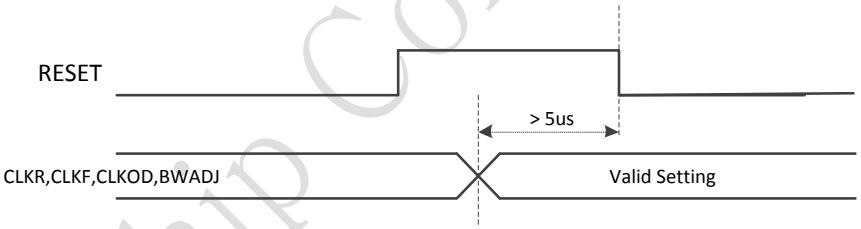

Fig. 3-5 PLL setting change timing

Before set some factors such as NR/NF/NO/BS to change PLL output frequency, you must change chip from normal to slow mode by programming CRU_MODE_CON. Then until PLL is lock state by checking GRF_SOC_STATUS0[8:5] register, or after delay about (NR * 500) / Fin, you can change PLL into normal mode.

3.8.3 Fractional divider usage

To get specific frequency, clocks of I2S, SPDIF, UART, HSADC can be generated by fractional divider. Generally you must set that denominator is 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock like I2S, UART and HSADC.
All the fractional divider has auto-gating control. When fractional divider is not selected, the divider clock is gated. So fractional divider must be selected before changing configuration.

3.8.4 Global software reset

Two global software resets are designed in this chip, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-deasserted by hardware.
TSADC, WDT and PMU also can trigger glb_srstn_1 or glb_srstn_2.
CRU_GLB_RST_CON controls which global soft-reset will be triggered.
After global reset, the reset trigger source can be check in CRU_GLB_RST_ST.

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glb_srstn_1 resets almost all chip logic except PMU_SYS_REG0~3, which can be used to store something when reset.
glb_srstn_2 resets almost all chip logic except PMU_SYS_REG0~3, GRF and GPIOs.

3.8.5 Pre-shift for test

Pre-shift registers is designed in this chip for flexible test.
The key configuration registers can be shifted with a initial value in testmode. The pre-shift registers including 191 bit pre_shift_test_reg.
The following table describes the pre-shift registers of the design.

Name	Bit number	Default value	Description
armpll_clkr	pre_shift_test_reg[5:0]	6'd0	armpll_clkr control
armpll_clkf	pre_shift_test_reg[18:6]	13'd199	armpll_clkf control
armpll_bwadj	pre_shift_test_reg[30:19]	12'd49	armpll_bwadj control
armpll_clkod	pre_shift_test_reg[35:31]	5'd1	armpll_clkod control
ddrpll_clkr	pre_shift_test_reg[41:36]	6'd1	ddrpll_clkr control
ddrpll_clkf	pre_shift_test_reg[54:42]	13'd99	ddrpll_clkf control
ddrpll_bwadj	pre_shift_test_reg[66:55]	12'd49	ddrpll_bwadj control
ddrpll_clkod	pre_shift_test_reg[71:67]	5'd5	ddrpll_clkod control
codecpll_clkr	pre_shift_test_reg[77:72]	6'd1	codecpll_clkr control
codecpll_clkf	pre_shift_test_reg[90:78]	13'd99	codecpll_clkf control
codecpll_bwadj	pre_shift_test_reg[102:91]	12'd49	codecpll_bwadj control
codecpll_clkod	pre_shift_test_reg[107:103]	5'd5	codecpll_clkod control
generalpll_clkr	pre_shift_test_reg[113:108]	6'd1	generalpll_clkr control
generalpll_clkf	pre_shift_test_reg[126:114]	13'd99	generalpll_clkf control
generalpll_bwadj	pre_shift_test_reg[138:127]	12'd49	generalpll_bwadj control
generalpll_clkod	pre_shift_test_reg[143:139]	5'd5	generalpll_clkod control
newpll_clkr	pre_shift_test_reg[149:144]	6'd1	newpll_clkr control
newpll_clkf	pre_shift_test_reg[162:150]	13'd99	newpll_clkf control
newpll_bwadj	pre_shift_test_reg[174:163]	12'd49	newpll_bwadj control
newpll_clkod	pre_shift_test_reg[179:175]	5'd5	newpll_clkod control
testclk_sel	pre_shift_test_reg[182:180]	3'd0	testclk_out select in testmode
aclk_core_m_div_con	pre_shift_test_reg[185:183]	3'd1	Aclk_m divider configuration in testmode
Io_sr	pre_shift_test_reg[186]	1'd1	IO slew rate
io_drive	pre_shift_test_reg[188:187]	2'b10	IO drive configuration
Io_vsel	pre_shift_test_reg[189]	1'd0	IO voltage select
Io_smt	pre_shift_test_reg[190]	1'd0	IO smt control

Pre-shift relative controls IO are as follow.

Name	IO	Description
Pre_shift_datain	IO_UART3GPSsout_GPSsig_HSADCT1data1_GPIO30gpio7b0	Pre-shift data in
Pre_shift_en	IO_UART3GPSctsn_GPSrfclk_GPST1clk_GPIO30gpio7b1	Pre-shift enable
Pre_shift_clk	IO_UART3GPSrtsn_USBdrvvbus0_GPIO30gpio7b2	Pre-shift clock
Pre-shift_default_select	IO_USBdrvvbus1_EDPhotplug_GPIO30gpio7b3	1'b0: pre_shift use default value; 1'b1: pre_shift use shift in value;
Pre-shift_select	IO_ISPshutteren_SPI1clk_GPIO30gpio7b4	1'b0: disable, testmode do not use pre-shift config value; use internal 6

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		configs. 1'b1: enable, testmode use pre-shift config value;

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Chapter 4 General Register Files (GRF)

4.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control. The GRF is divided into two sections, one is GRF for non-secure system, the other is SGRF for secure system.

4.2 Function Description

The function of general register file is:

IOMUX control
Control the state of GPIO in power-down mode
GPIO PAD pull down and pull up control
Used for common system control
Used to record the system state

4.3 GRF Register Description

4.3.1 Register Summary

Name	Offset	Size	Reset Value	Description
GRF_GPIO1D_IOMUX	0x000c	W	0x00000000	GPIO1D iomux control
GRF_GPIO2A_IOMUX	0x0010	W	0x00000000	GPIO2A iomux control
GRF_GPIO2B_IOMUX	0x0014	W	0x00000000	GPIO2B iomux control
GRF_GPIO2C_IOMUX	0x0018	W	0x00000000	GPIO2C iomux control
GRF_GPIO3A_IOMUX	0x0020	W	0x00000000	GPIO3A iomux control
GRF_GPIO3B_IOMUX	0x0024	W	0x00000000	GPIO3B iomux control
GRF_GPIO3C_IOMUX	0x0028	W	0x00000000	GPIO3C iomux control
GRF_GPIO3DL_IOMUX	0x002c	W	0x00000000	GPIO3D iomux control
GRF_GPIO3DH_IOMUX	0x0030	W	0x00000000	GPIO3D iomux control
GRF_GPIO4AL_IOMUX	0x0034	W	0x00000000	GPIO4A iomux control
GRF_GPIO4AH_IOMUX	0x0038	W	0x00000000	GPIO4A iomux control
GRF_GPIO4BL_IOMUX	0x003c	W	0x00000000	GPIO4B iomux control
GRF_GPIO4C_IOMUX	0x0044	W	0x00000000	GPIO4C iomux control
GRF_GPIO4D_IOMUX	0x0048	W	0x00000000	GPIO4D iomux control
GRF_GPIO5B_IOMUX	0x0050	W	0x00000000	GPIO5B iomux control
GRF_GPIO5C_IOMUX	0x0054	W	0x00000000	GPIO5C iomux control
GRF_GPIO6A_IOMUX	0x005c	W	0x00000000	GPIO6A iomux control
GRF_GPIO6B_IOMUX	0x0060	W	0x00000000	GPIO6B iomux control
GRF_GPIO6C_IOMUX	0x0064	W	0x00001555	GPIO6C iomux control
GRF_GPIO7A_IOMUX	0x006c	W	0x00000000	GPIO7A iomux control
GRF_GPIO7B_IOMUX	0x0070	W	0x00000000	GPIO7B iomux control
GRF_GPIO7CL_IOMUX	0x0074	W	0x00000000	GPIO7CL iomux control
GRF_GPIO7CH_IOMUX	0x0078	W	0x00000000	GPIO7CH iomux control
GRF_GPIO8A_IOMUX	0x0080	W	0x00000000	GPIO8A iomux control

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Name	Offset	Size	Reset Value	Description
GRF_GPIO8B_IOMUX	0x0084	W	0x00000000	GPIO8B iomux control
GRF_GPIO1H_SR	0x0104	W	0x00000f00	GPIO1C/D SR control
GRF_GPIO2L_SR	0x0108	W	0x00000000	GPIO2A/B SR control
GRF_GPIO2H_SR	0x010c	W	0x00000000	GPIO2C/D SR control
GRF_GPIO3L_SR	0x0110	W	0x000020ff	GPIO3A/B SR control
GRF_GPIO3H_SR	0x0114	W	0x0000ff04	GPIO3C/D SR control
GRF_GPIO4L_SR	0x0118	W	0x00000120	GPIO4A/B SR control
GRF_GPIO4H_SR	0x011c	W	0x00000000	GPIO4C/D SR control
GRF_GPIO5L_SR	0x0120	W	0x00000000	GPIO5A/B SR control
GRF_GPIO5H_SR	0x0124	W	0x00000000	GPIO5C/D SR control
GRF_GPIO6L_SR	0x0128	W	0x00000100	GPIO6A/B SR control
GRF_GPIO6H_SR	0x012c	W	0x00000010	GPIO6C/D SR control
GRF_GPIO7L_SR	0x0130	W	0x00000000	GPIO7A/B SR control
GRF_GPIO7H_SR	0x0134	W	0x00000000	GPIO7C/D SR control
GRF_GPIO8L_SR	0x0138	W	0x00000000	GPIO8A/B SR control
GRF_GPIO1D_P	0x014c	W	0x0000aaaa	GPIO1D PU/PD control
GRF_GPIO2A_P	0x0150	W	0x0000aaaa	GPIO2A PU/PD control
GRF_GPIO2B_P	0x0154	W	0x0000aaaa	GPIO2B PU/PD control
GRF_GPIO2C_P	0x0158	W	0x0000aaa5	GPIO2C PU/PD control
GRF_GPIO3A_P	0x0160	W	0x00005555	GPIO3A PU/PD control
GRF_GPIO3B_P	0x0164	W	0x00005699	GPIO3B PU/PD control
GRF_GPIO3C_P	0x0168	W	0x0000aaa5	GPIO3C PU/PD control
GRF_GPIO3D_P	0x016c	W	0x00005555	GPIO3D PU/PD control
GRF_GPIO4A_P	0x0170	W	0x00005555	GPIO4A PU/PD control
GRF_GPIO4B_P	0x0174	W	0x0000aaa5	GPIO4B PU/PD control
GRF_GPIO4C_P	0x0178	W	0x00005559	GPIO4C PU/PD control
GRF_GPIO4D_P	0x017c	W	0x00005a99	GPIO4D PU/PD control
GRF_GPIO5B_P	0x0184	W	0x00006559	GPIO5B PU/PD control
GRF_GPIO5C_P	0x0188	W	0x0000aaa9	GPIO5C PU/PD control
GRF_GPIO6A_P	0x0190	W	0x0000aaaa	GPIO6A PU/PD control
GRF_GPIO6B_P	0x0194	W	0x0000aa96	GPIO6B PU/PD control
GRF_GPIO6C_P	0x0198	W	0x00005655	GPIO6C PU/PD control
GRF_GPIO7A_P	0x01a0	W	0x000059aa	GPIO7A PU/PD control
GRF_GPIO7B_P	0x01a4	W	0x0000a696	GPIO7B PU/PD control
GRF_GPIO7C_P	0x01a8	W	0x00005955	GPIO7C PU/PD control
GRF_GPIO8A_P	0x01b0	W	0x00006555	GPIO8A PU/PD control
GRF_GPIO8B_P	0x01b4	W	0x0000aaaa	GPIO8B PU/PD control
GRF_GPIO1D_E	0x01cc	W	0x000055aa	GPIO1D drive strength control
GRF_GPIO2A_E	0x01d0	W	0x0000aaaa	GPIO2A drive strength control
GRF_GPIO2B_E	0x01d4	W	0x0000aaaa	GPIO2B drive strength control
GRF_GPIO2C_E	0x01d8	W	0x00005555	GPIO2C drive strength control
GRF_GPIO3A_E	0x01e0	W	0x0000aaaa	GPIO3A drive strength control
GRF_GPIO3B_E	0x01e4	W	0x00005955	GPIO3B drive strength control

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Name	Offset	Size	Reset Value	Description
GRF_GPIO3C_E	0x01e8	W	0x00005565	GPIO3C drive strength control
GRF_GPIO3D_E	0x01ec	W	0x0000aaaa	GPIO3D drive strength control
GRF_GPIO4A_E	0x01f0	W	0x00005955	GPIO4A drive strength control
GRF_GPIO4B_E	0x01f4	W	0x00005556	GPIO4B drive strength control
GRF_GPIO4C_E	0x01f8	W	0x00005555	GPIO4C drive strength control
GRF_GPIO4D_E	0x01fc	W	0x00005555	GPIO4D drive strength control
GRF_GPIO5B_E	0x0204	W	0x00005555	GPIO5B drive strength control
GRF_GPIO5C_E	0x0208	W	0x00005555	GPIO5C drive strength control
GRF_GPIO6A_E	0x0210	W	0x00005555	GPIO6A drive strength control
GRF_GPIO6B_E	0x0214	W	0x00005555	GPIO6B drive strength control
GRF_GPIO6C_E	0x0218	W	0x00005555	GPIO6C drive strength control
GRF_GPIO7A_E	0x0220	W	0x00005555	GPIO7A drive strength control
GRF_GPIO7B_E	0x0224	W	0x00005555	GPIO7B drive strength control
GRF_GPIO7C_E	0x0228	W	0x00005555	GPIO7C drive strength control
GRF_GPIO8A_E	0x0230	W	0x00005555	GPIO8A drive strength control
GRF_GPIO8B_E	0x0234	W	0x00005555	GPIO8B drive strength control
GRF_GPIO_SMT	0x0240	W	0x00000fff	GPIO smitter control register
GRF_SOC_CON0	0x0244	W	0x00001c18	SoC control register 0
GRF_SOC_CON1	0x0248	W	0x00004040	SoC control register 1
GRF_SOC_CON2	0x024c	W	0x00000002	SoC control register 2
GRF_SOC_CON3	0x0250	W	0x00000810	SoC control register 3
GRF_SOC_CON4	0x0254	W	0x00000607	SoC control register 4
GRF_SOC_CON5	0x0258	W	0x00008c87	SoC control register 5
GRF_SOC_CON6	0x025c	W	0x00008000	SoC control register 6
GRF_SOC_CON7	0x0260	W	0x00000000	SoC control register 7
GRF_SOC_CON8	0x0264	W	0x0000000e	SoC control register 8
GRF_SOC_CON9	0x0268	W	0x0000000e	SoC control register 9
GRF_SOC_CON10	0x026c	W	0x0000000f	SoC control register 10
GRF_SOC_CON11	0x0270	W	0x00000000	SoC control register 11
GRF_SOC_CON12	0x0274	W	0x00000013	SoC control register 12
GRF_SOC_CON13	0x0278	W	0x00000000	SoC control register 13
GRF_SOC_CON14	0x027c	W	0x00000000	SoC control register 14
GRF_SOC_STATUS0	0x0280	W	0x00000000	SoC status register 0
GRF_SOC_STATUS1	0x0284	W	0x00000000	SoC status register 1
GRF_SOC_STATUS2	0x0288	W	0x00000000	SoC status register 2
GRF_SOC_STATUS3	0x028c	W	0x00000000	SoC status register 3
GRF_SOC_STATUS4	0x0290	W	0x00000000	SoC status register 4
GRF_SOC_STATUS5	0x0294	W	0x00000000	SoC status register 5
GRF_SOC_STATUS6	0x0298	W	0x00000000	SoC status register 6
GRF_SOC_STATUS7	0x029c	W	0x00000000	SoC status register 7
GRF_SOC_STATUS8	0x02a0	W	0x00000000	SoC status register 8
GRF_SOC_STATUS9	0x02a4	W	0x00000000	SoC status register 9
GRF_SOC_STATUS10	0x02a8	W	0x00000000	SoC status register 10

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Name	Offset	Size	Reset Value	Description
GRF_SOC_STATUS11	0x02ac	W	0x00000000	SoC status register 11
GRF_SOC_STATUS12	0x02b0	W	0x00000000	SoC status register 12
GRF_SOC_STATUS13	0x02b4	W	0x00000000	SoC status register 13
GRF_SOC_STATUS14	0x02b8	W	0x00000000	SoC status register 14
GRF_SOC_STATUS15	0x02bc	W	0x00000000	SoC status register 15
GRF_SOC_STATUS16	0x02c0	W	0x00000000	SoC status register 16
GRF_SOC_STATUS17	0x02c4	W	0x00000000	SoC status register 17
GRF_SOC_STATUS18	0x02c8	W	0x00000000	SoC status register 18
GRF_SOC_STATUS19	0x02cc	W	0x00000000	SoC status register 19
GRF_SOC_STATUS20	0x02d0	W	0x00000000	SoC status register 20
GRF_SOC_STATUS21	0x02d4	W	0x00000000	SoC status register 21
GRF_PERIDMAC_CON0	0x02e0	W	0x000000fa	PERI DMAC control register 0
GRF_PERIDMAC_CON1	0x02e4	W	0x00000000	PERI DMAC control register 1
GRF_PERIDMAC_CON2	0x02e8	W	0x0000ffff	PERI DMAC control register 2
GRF_PERIDMAC_CON3	0x02ec	W	0x0000ffff	PERI DMAC control register 3
GRF_DDRC0_CON0	0x02f0	W	0x00000000	DDRC0 control register 0
GRF_DDRC1_CON0	0x02f4	W	0x00000000	DDRC1 control register 0
GRF_CPU_CON0	0x02f8	W	0x00008220	CPU control register 0
GRF_CPU_CON1	0x02fc	W	0x00000ff0	CPU control register 1
GRF_CPU_CON2	0x0300	W	0x00000fff	CPU control register 2
GRF_CPU_CON3	0x0304	W	0x00000000	CPU control register 3
GRF_CPU_CON4	0x0308	W	0x00002400	CPU control register 4
GRF_CPU_STATUS0	0x0318	W	0x00000000	CPU status register 0
GRF_UOC0_CON0	0x0320	W	0x00000089	UOC0 control register 0
GRF_UOC0_CON1	0x0324	W	0x00007333	UOC0 control register 1
GRF_UOC0_CON2	0x0328	W	0x00000d08	UOC0 control register 2
GRF_UOC0_CON3	0x032c	W	0x00000001	UOC0 control register 3
GRF_UOC0_CON4	0x0330	W	0x00000003	UOC0 control register 4
GRF_UOC1_CON0	0x0334	W	0x00000b89	UOC1 control register 0
GRF_UOC1_CON1	0x0338	W	0x00007333	UOC1 control register 1
GRF_UOC1_CON2	0x033c	W	0x00000d08	UOC1 control register 2
GRF_UOC1_CON3	0x0340	W	0x00001c41	UOC1 control register 3
GRF_UOC1_CON4	0x0344	W	0x0000c820	UOC1 control register 4
GRF_UOC2_CON0	0x0348	W	0x00000089	UOC2 control register 0
GRF_UOC2_CON1	0x034c	W	0x00007333	UOC2 control register 1
GRF_UOC2_CON2	0x0350	W	0x00000d08	UOC2 control register 2
GRF_UOC2_CON3	0x0354	W	0x00001c01	UOC2 control register 3
GRF_UOC3_CON0	0x0358	W	0x000030eb	UOC3 control register 0
GRF_UOC3_CON1	0x035c	W	0x00000003	UOC3 control register 1
GRF_UOC4_CON0	0x0360	W	0x00001080	UOC4 control register 0
GRF_UOC4_CON1	0x0364	W	0x00000820	UOC4 control register 1
GRF_PVTM_CON0	0x0368	W	0x00000000	PVT monitor control register 0
GRF_PVTM_CON1	0x036c	W	0x016e3600	PVT monitor control register 1

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Name	Offset	Size	Reset Value	Description
GRF_PVTM_CON2	0x0370	W	0x016e3600	PVT monitor control register 2
GRF_PVTM_STATUS0	0x0374	W	0x00000000	PVT monitor status register 0
GRF_PVTM_STATUS1	0x0378	W	0x00000000	PVT monitor status register 1
GRF_PVTM_STATUS2	0x037c	W	0x00000000	PVT monitor status register 2
GRF_IO_VSEL	0x0380	W	0x00000004	IO voltage select
GRF_SARADC_TESTBIT	0x0384	W	0x00000000	SARADC Test bit register
GRF_TSADC_TESTBIT_L	0x0388	W	0x00000000	TSADC Test bit low register
GRF_TSADC_TESTBIT_H	0x038c	W	0x00000000	TSADC Test bit high register
GRF_OS_REG0	0x0390	W	0x00000000	OS register 0
GRF_OS_REG1	0x0394	W	0x00000000	OS register 1
GRF_OS_REG2	0x0398	W	0x00000000	OS register 2
GRF_OS_REG3	0x039c	W	0x00000000	OS register 3
GRF_SOC_CON15	0x03a4	W	0x00000000	SoC control register 15
GRF_SOC_CON16	0x03a8	W	0x00000000	SoC control register 16

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

4.3.2 Detail Register Description

GRF_GPIO1D_IOMUX
Address: Operational Base + offset (0x000c)
GPIO1D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio1d3_sel GPIO1D[3] iomux select 1'b0: gpio 1'b1: lcdc0_dclk
5	RO	0x0	reserved
4	RW	0x0	gpio1d2_sel GPIO1D[2] iomux select 1'b0: gpio 1'b1: lcdc0_den
3	RO	0x0	reserved
2	RW	0x0	gpio1d1_sel GPIO1D[1] iomux select 1'b0: gpio 1'b1: lcdc0_vsync
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio1d0_sel GPIO1D[0] iomux select 1'b0: gpio 1'b1: lcdc0_hsync

GRF_GPIO2A_IOMUX
Address: Operational Base + offset (0x0010)
GPIO2A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio2a7_sel GPIO2A[7] iomux select 2'b00: gpio 2'b01: cif_data9 2'b10: host_din5 2'b11: hsadc_data7
13:12	RW	0x0	gpio2a6_sel GPIO2A[6] iomux select 2'b00: gpio 2'b01: cif_data8 2'b10: host_din4 2'b11: hsadc_data6
11:10	RW	0x0	gpio2a5_sel GPIO2A[5] iomux select 2'b00: gpio 2'b01: cif_data7 2'b10: host_ckinn 2'b11: hsadc_data5
9:8	RW	0x0	gpio2a4_sel GPIO2A[4] iomux select 2'b00: gpio 2'b01: cif_data6 2'b10: host_ckinp 2'b11: hsadc_data4
7:6	RW	0x0	gpio2a3_sel GPIO2A[3] iomux select 2'b00: gpio 2'b01: cif_data5 2'b10: host_din3 2'b11: hsadc_data3

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio2a2_sel GPIO2A[2] iomux select 2'b00: gpio 2'b01: cif_data4 2'b10: host_din2 2'b11: hsadc_data2
3:2	RW	0x0	gpio2a1_sel GPIO2A[1] iomux select 2'b00: gpio 2'b01: cif_data3 2'b10: host_din1 2'b11: hsadc_data1
1:0	RW	0x0	gpio2a0_sel GPIO2A[0] iomux select 2'b00: gpio 2'b01: cif_data2 2'b10: host_din0 2'b11: hsadc_data0

GRF_GPIO2B_IOMUX
Address: Operational Base + offset (0x0014)
GPIO2B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	gpio2b7_sel GPIO2B[7] iomux select 1'b0: gpio 1'b1: cif_data11
13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	gpio2b6_sel GPIO2B[6] iomux select 1'b0: gpio 1'b1: cif_data10
11	RO	0x0	reserved
10	RW	0x0	gpio2b5_sel GPIO2B[5] iomux select 1'b0: gpio 1'b1: cif_data1
9	RO	0x0	reserved
8	RW	0x0	gpio2b4_sel GPIO2B[4] iomux select 1'b0: gpio 1'b1: cif_data0
7:6	RW	0x0	gpio2b3_sel GPIO2B[3] iomux select 2'b00: gpio 2'b01: cif_clkout 2'b10: host_wkreq 2'b11: hsadcts_fail
5:4	RW	0x0	gpio2b2_sel GPIO2B[2] iomux select 2'b00: gpio 2'b01: cif_clkin 2'b10: host_wkack 2'b11: gps_clk (when hsadc_clkout_en==0) hsadc_clkout (when hsadc_clkout_en==1)
3:2	RW	0x0	gpio2b1_sel GPIO2B[1] iomux select 2'b00: gpio 2'b01: cif_href 2'b10: host_din7 2'b11: hsadcts_valid
1:0	RW	0x0	gpio2b0_sel GPIO2B[0] iomux select 2'b00: gpio 2'b01: cif_vsync 2'b10: host_din6 2'b11: hsadcts_sync

GRF_GPIO2C_IOMUX
Address: Operational Base + offset (0x0018)
GPIO2C iomux control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:3	RO	0x0	reserved
2	RW	0x0	gpio2c1_sel GPIO2C[1] iomux select 1'b0: gpio 1'b1: i2c3cam_sda
1	RO	0x0	reserved
0	RW	0x0	gpio2c0_sel GPIO2C[0] iomux select 1'b0: gpio 1'b1: i2c3cam_scl

GRF_GPIO3A_IOMUX
Address: Operational Base + offset (0x0020)
GPIO3A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio3a7_sel GPIO3A[7] iomux select 2'b00: gpio 2'b01: flash0_data7 2'b10: emmc_data7 2'b11: reserved
13:12	RW	0x0	gpio3a6_sel GPIO3A[6] iomux select 2'b00: gpio 2'b01: flash0_data6 2'b10: emmc_data6 2'b11: reserved
11:10	RW	0x0	gpio3a5_sel GPIO3A[5] iomux select 2'b00: gpio 2'b01: flash0_data5 2'b10: emmc_data5 2'b11: reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	gpio3a4_sel GPIO3A[4] iomux select 2'b00: gpio 2'b01: flash0_data4 2'b10: emmc_data4 2'b11: reserved
7:6	RW	0x0	gpio3a3_sel GPIO3A[3] iomux select 2'b00: gpio 2'b01: flash0_data3 2'b10: emmc_data3 2'b11: reserved
5:4	RW	0x0	gpio3a2_sel GPIO3A[2] iomux select 2'b00: gpio 2'b01: flash0_data2 2'b10: emmc_data2 2'b11: reserved
3:2	RW	0x0	gpio3a1_sel GPIO3A[1] iomux select 2'b00: gpio 2'b01: flash0_data1 2'b10: emmc_data1 2'b11: reserved
1:0	RW	0x0	gpio3a0_sel GPIO3A[0] iomux select 2'b00: gpio 2'b01: flash0_data0 2'b10: emmc_data0 2'b11: reserved

GRF_GPIO3B_IOMUX
Address: Operational Base + offset (0x0024)
GPIO3B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	gpio3b7_sel GPIO3B[7] iomux select 1'b0: gpio 1'b1: flash0_csn1
13	RO	0x0	reserved
12	RW	0x0	gpio3b6_sel GPIO3B[6] iomux select 1'b0: gpio 1'b1: flash0_csn0
11	RO	0x0	reserved
10	RW	0x0	gpio3b5_sel GPIO3B[5] iomux select 1'b0: gpio 1'b1: flash0_wrn
9	RO	0x0	reserved
8	RW	0x0	gpio3b4_sel GPIO3B[4] iomux select 1'b0: gpio 1'b1: flash0_cle
7	RO	0x0	reserved
6	RW	0x0	gpio3b3_sel GPIO3B[3] iomux select 1'b0: gpio 1'b1: flash0_ale
5	RO	0x0	reserved
4	RW	0x0	gpio3b2_sel GPIO3B[2] iomux select 1'b0: gpio 1'b1: flash0_rdn
3:2	RW	0x0	gpio3b1_sel GPIO3B[1] iomux select 2'b00: gpio 2'b01: flash0_wp 2'b10: emmc_pwren 2'b11: reserved
1	RO	0x0	reserved
0	RW	0x0	gpio3b0_sel GPIO3B[0] iomux select 1'b0: gpio 1'b1: flash0_rdy

GRF_GPIO3C_IOMUX
Address: Operational Base + offset (0x0028)
GPIO3C iomux control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5:4	RW	0x0	gpio3c2_sel GPIO3C[2] iomux select 2'b00: gpio 2'b01: flash0_dqs 2'b10: emmc_clkout 2'b11: reserved
3:2	RW	0x0	gpio3c1_sel GPIO3C[1] iomux select 2'b00: gpio 2'b01: flash0_csn3 2'b10: emmc_rstnout 2'b11: reserved
1:0	RW	0x0	gpio3c0_sel GPIO3C[0] iomux select 2'b00: gpio 2'b01: flash0_csn2 2'b10: emmc_cmd 2'b11: reserved

GRF_GPIO3DL_IOMUX
Address: Operational Base + offset (0x002c)
GPIO3D iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d3_sel GPIO3D[3] iomux select 3'b000: gpio 3'b001: flash1_data3 3'b010: host_dout3 3'b011: mac_rxd3 3'b100: sdio1_data3 other: reserved

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Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d2_sel GPIO3D[2] iomux select 3'b000: gpio 3'b001: flash1_data2 3'b010: host_dout2 3'b011: mac_rxd2 3'b100: sdio1_data2 other: reserved
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d1_sel GPIO3D[1] iomux select 3'b000: gpio 3'b001: flash1_data1 3'b010: host_dout1 3'b011: mac_txd3 3'b100: sdio1_data1 other: reserved
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d0_sel GPIO3D[0] iomux select 3'b000: gpio 3'b001: flash1_data0 3'b010: host_dout0 3'b011: mac_txd2 3'b100: sdio1_data0 other: reserved

GRF_GPIO3DH_IOMUX
Address: Operational Base + offset (0x0030)
GPIO3D iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio3d7_sel GPIO3D[7] iomux select 3'b000: gpio 3'b001: flash1_data7 3'b010: host_dout7 3'b011: mac_rxd1 3'b100: sdio1_intn other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d6_sel GPIO3D[6] iomux select 3'b000: gpio 3'b001: flash1_data6 3'b010: host_dout6 3'b011: mac_rxd0 3'b100: sdio1_bkpwr other: reserved
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d5_sel GPIO3D[5] iomux select 3'b000: gpio 3'b001: flash1_data5 3'b010: host_dout5 3'b011: mac_txd1 3'b100: sdio1_wrprt other: reserved
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d4_sel GPIO3D[4] iomux select 3'b000: gpio 3'b001: flash1_data4 3'b010: host_dout4 3'b011: mac_txd0 3'b100: sdio1_detectn other: reserved

GRF_GPIO4AL_IOMUX
Address: Operational Base + offset (0x0034)
GPIO4A iomux control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a3_sel GPIO4A[3] iomux select 3'b001: flash1_ale 3'b010: host_dout9 3'b011: mac_clk 3'b100: flash0_csn6 other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a2_sel GPIO4A[2] iomux select 3'b000: gpio 3'b001: flash1_rdn 3'b010: host_dout8 3'b011: mac_rxer 3'b100: flash0_csn5 other: reserved
7	RO	0x0	reserved
6:4	RW	0x0	gpio4a1_sel GPIO4A[1] iomux select 3'b000: gpio 3'b001: flash1_wp 3'b010: host_ckoutn 3'b011: mac_rxdv 3'b100: flash0_csn4 other: reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	gpio4a0_sel GPIO4A[0] iomux select 2'b00: gpio 2'b01: flash1_rdy 2'b10: host_ckoutp 2'b11: mac_mdc

GRF_GPIO4AH_IOMUX
Address: Operational Base + offset (0x0038)
GPIO4A iomux control

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a7_sel GPIO4A[7] iomux select 3'b000: gpio 3'b001: flash1_csn1 3'b010: host_dout13 3'b011: mac_crs 3'b100: sdio1_clkout other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a6_sel GPIO4A[6] iomux select 3'b000: gpio 3'b001: flash1_csn0 3'b010: host_dout12 3'b011: mac_rxclk 3'b100: sdio1_cmd other: reserved
7:6	RO	0x0	reserved
5:4	RW	0x0	gpio4a5_sel GPIO4A[5] iomux select 2'b00: gpio 2'b01: flash1_wrn 2'b10: host_dout11 2'b11: mac_mdio
3	RO	0x0	reserved
2:0	RW	0x0	gpio4a4_sel GPIO4A[4] iomux select 3'b000: gpio 3'b001: flash1_cle 3'b010: host_dout10 3'b011: mac_txen 3'b100: flash0_csn7 other: reserved

GRF_GPIO4BL_IOMUX
Address: Operational Base + offset (0x003c)
GPIO4B iomux control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6:4	RW	0x0	gpio4b1_sel GPIO4B[1] iomux select 3'b000: gpio 3'b001: flash1_csn2 3'b010: host_dout15 3'b011: mac_txclk 3'b100: sdio1_pwren other: reserved
3	RO	0x0	reserved
2:0	RW	0x0	gpio4b0_sel GPIO4B[0] iomux select 3'b000: gpio 3'b001: flash1_dqs 3'b010: host_dout14 3'b011: mac_col 3'b100: flash1_csn3 other: reserved

GRF_GPIO4C_IOMUX
Address: Operational Base + offset (0x0044)
GPIO4C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio4c7_sel GPIO4C[7] iomux select 1'b0: gpio 1'b1: sdio0_data3
13	RO	0x0	reserved
12	RW	0x0	gpio4c6_sel GPIO4C[6] iomux select 1'b0: gpio 1'b1: sdio0_data2

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Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10	RW	0x0	gpio4c5_sel GPIO4C[5] iomux select 1'b0: gpio 1'b1: sdio0_data1
9	RO	0x0	reserved
8	RW	0x0	gpio4c4_sel GPIO4C[4] iomux select 1'b0: gpio 1'b1: sdio0_data0
7	RO	0x0	reserved
6	RW	0x0	gpio4c3_sel GPIO4C[3] iomux select 1'b0: gpio 1'b1: uart0bt_rtsn
5	RO	0x0	reserved
4	RW	0x0	gpio4c2_sel GPIO4C[2] iomux select 1'b0: gpio 1'b1: uart0bt_ctsn
3	RO	0x0	reserved
2	RW	0x0	gpio4c1_sel GPIO4C[1] iomux select 1'b0: gpio 1'b1: uart0bt_sout
1	RO	0x0	reserved
0	RW	0x0	gpio4c0_sel GPIO4C[0] iomux select 1'b0: gpio 1'b1: uart0bt_sin

GRF_GPIO4D_IOMUX
Address: Operational Base + offset (0x0048)
GPIO4D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	gpio4d6_sel GPIO4D[6] iomux select 1'b0: gpio 1'b1: sdio0_intn
11	RO	0x0	reserved
10	RW	0x0	gpio4d5_sel GPIO4D[5] iomux select 1'b0: gpio 1'b1: sdio0_bkpwr
9	RO	0x0	reserved
8	RW	0x0	gpio4d4_sel GPIO4D[4] iomux select 1'b0: gpio 1'b1: sdio0_pwren
7	RO	0x0	reserved
6	RW	0x0	gpio4d3_sel GPIO4D[3] iomux select 1'b0: gpio 1'b1: sdio0_wrprt
5	RO	0x0	reserved
4	RW	0x0	gpio4d2_sel GPIO4D[2] iomux select 1'b0: gpio 1'b1: sdio0_detectn
3	RO	0x0	reserved
2	RW	0x0	gpio4d1_sel GPIO4D[1] iomux select 1'b0: gpio 1'b1: sdio0_clkout
1	RO	0x0	reserved
0	RW	0x0	gpio4d0_sel GPIO4D[0] iomux select 1'b0: gpio 1'b1: sdio0_cmd

GRF_GPIO5B_IOMUX
Address: Operational Base + offset (0x0050)
GPIO5B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio5b7_sel GPIO5B[7] iomux select 2'b00: gpio 2'b01: spi0_rxd 2'b10: ts0_data7 2'b11: uart4exp_sin
13:12	RW	0x0	gpio5b6_sel GPIO5B[6] iomux select 2'b00: gpio 2'b01: spi0_txd 2'b10: ts0_data6 2'b11: uart4exp_sout
11:10	RW	0x0	gpio5b5_sel GPIO5B[5] iomux select 2'b00: gpio 2'b01: spi0_csn0 2'b10: ts0_data5 2'b11: uart4exp_rtsn
9:8	RW	0x0	gpio5b4_sel GPIO5B[4] iomux select 2'b00: gpio 2'b01: spi0_clk 2'b10: ts0_data4 2'b11: uart4exp_ctsn
7:6	RW	0x0	gpio5b3_sel GPIO5B[3] iomux select 2'b00: gpio 2'b01: uart1bb_rtsn 2'b10: ts0_data3 2'b11: reserved
5:4	RW	0x0	gpio5b2_sel GPIO5B[2] iomux select 2'b00: gpio 2'b01: uart1bb_ctsn 2'b10: ts0_data2 2'b11: reserved
3:2	RW	0x0	gpio5b1_sel GPIO5B[1] iomux select 2'b00: gpio 2'b01: uart1bb_sout 2'b10: ts0_data1 2'b11: reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio5b0_sel GPIO5B[0] iomux select 2'b00: gpio 2'b01: uart1bb_sin 2'b10: ts0_data0 2'b11: reserved

GRF_GPIO5C_IOMUX
Address: Operational Base + offset (0x0054)
GPIO5C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio5c3_sel GPIO5C[3] iomux select 1'b0: gpio 1'b1: ts0_err
5	RO	0x0	reserved
4	RW	0x0	gpio5c2_sel GPIO5C[2] iomux select 1'b0: gpio 1'b1: ts0_clk
3	RO	0x0	reserved
2	RW	0x0	gpio5c1_sel GPIO5C[1] iomux select 1'b0: gpio 1'b1: ts0_valid
1:0	RW	0x0	gpio5c0_sel GPIO5C[0] iomux select 2'b00: gpio 2'b01: spi0_csn1 2'b10: ts0_sync 2'b11: reserved

GRF_GPIO6A_IOMUX
Address: Operational Base + offset (0x005c)
GPIO6A iomux control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio6a7_sel GPIO6A[7] iomux select 1'b0: gpio 1'b1: i2s_sdo3
13	RO	0x0	reserved
12	RW	0x0	gpio6a6_sel GPIO6A[6] iomux select 1'b0: gpio 1'b1: i2s_sdo2
11	RO	0x0	reserved
10	RW	0x0	gpio6a5_sel GPIO6A[5] iomux select 1'b0: gpio 1'b1: i2s_sdo1
9	RO	0x0	reserved
8	RW	0x0	gpio6a4_sel GPIO6A[4] iomux select 1'b0: gpio 1'b1: i2s_sdo0
7	RO	0x0	reserved
6	RW	0x0	gpio6a3_sel GPIO6A[3] iomux select 1'b0: gpio 1'b1: i2s_sdi
5	RO	0x0	reserved
4	RW	0x0	gpio6a2_sel GPIO6A[2] iomux select 1'b0: gpio 1'b1: i2s_lrcktx
3	RO	0x0	reserved
2	RW	0x0	gpio6a1_sel GPIO6A[1] iomux select 1'b0: gpio 1'b1: i2s_lrckrx
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio6a0_sel GPIO6A[0] iomux select 1'b0: gpio 1'b1: i2s_sclk

GRF_GPIO6B_IOMUX
Address: Operational Base + offset (0x0060)
GPIO6B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio6b3_sel GPIO6B[3] iomux select 1'b0: gpio 1'b1: spdif_tx
5	RO	0x0	reserved
4	RW	0x0	gpio6b2_sel GPIO6B[2] iomux select 1'b0: gpio 1'b1: i2c1audio_scl
3	RO	0x0	reserved
2	RW	0x0	gpio6b1_sel GPIO6B[1] iomux select 1'b0: gpio 1'b1: i2c1audio_sda
1	RO	0x0	reserved
0	RW	0x0	gpio6b0_sel GPIO6B[0] iomux select 1'b0: gpio 1'b1: i2s_clk

GRF_GPIO6C_IOMUX
Address: Operational Base + offset (0x0064)
GPIO6C iomux control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x1	gpio6c6_sel GPIO6C[6] iomux select 1'b0: gpio 1'b1: sdmmc0_dectn
11	RO	0x0	reserved
10	RW	0x1	gpio6c5_sel GPIO6C[5] iomux select 1'b0: gpio 1'b1: sdmmc0_cmd
9:8	RW	0x1	gpio6c4_sel GPIO6C[4] iomux select 2'b00: gpio 2'b01: sdmmc0_clkout 2'b10: jtag_tdo 2'b11: reserved
7:6	RW	0x1	gpio6c3_sel GPIO6C[3] iomux select 2'b00: gpio 2'b01: sdmmc0_data3 2'b10: jtag_tck 2'b11: reserved
5:4	RW	0x1	gpio6c2_sel GPIO6C[2] iomux select 2'b00: gpio 2'b01: sdmmc0_data2 2'b10: jtag_tdi 2'b11: reserved
3:2	RW	0x1	gpio6c1_sel GPIO6C[1] iomux select 2'b00: gpio 2'b01: sdmmc0_data1 2'b10: jtag_trstn 2'b11: reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio6c0_sel GPIO6C[0] iomux select 2'b00: gpio 2'b01: sdmmc0_data0 2'b10: jtag_tms 2'b11: reserved

GRF_GPIO7A_IOMUX
Address: Operational Base + offset (0x006c)
GPIO7A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio7a7_sel GPIO7A[7] iomux select 2'b00: gpio 2'b01: uart3gps_sin 2'b10: gps_mag 2'b11: hsadct1_data0
13:3	RO	0x0	reserved
2	RW	0x0	gpio7a1_sel GPIO7A[1] iomux select 1'b0: gpio 1'b1: pwm_1
1:0	RW	0x0	gpio7a0_sel GPIO7A[0] iomux select 2'b00: gpio 2'b01: pwm_0 2'b10: vop0_pwm 2'b11: vop1_pwm

GRF_GPIO7B_IOMUX
Address: Operational Base + offset (0x0070)
GPIO7B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio7b7_sel GPIO7B[7] iomux select 2'b00: gpio 2'b01: isp_shuttertrig 2'b10: spi1_txd 2'b11: reserved
13:12	RW	0x0	gpio7b6_sel GPIO7B[6] iomux select 2'b00: gpio 2'b01: isp_prelighttrig 2'b10: spi1_rxd 2'b11: reserved
11:10	RW	0x0	gpio7b5_sel GPIO7B[5] iomux select 2'b00: gpio 2'b01: isp_flashtrigout 2'b10: spi1_csn0 2'b11: reserved
9:8	RW	0x0	gpio7b4_sel GPIO7B[4] iomux select 2'b00: gpio 2'b01: isp_shutteren 2'b10: spi1_clk 2'b11: reserved
7:6	RW	0x0	gpio7b3_sel GPIO7B[3] iomux select 2'b00: gpio 2'b01: usb_drvvbus1 2'b10: edp_hotplug 2'b11: reserved
5:4	RW	0x0	gpio7b2_sel GPIO7B[2] iomux select 2'b00: gpio 2'b01: uart3gps_rtsn 2'b10: usb_drvvbus0 2'b11: reserved
3:2	RW	0x0	gpio7b1_sel GPIO7B[1] iomux select 2'b00: gpio 2'b01: uart3gps_ctsn 2'b10: gps_rfclk 2'b11: gpst1_clk

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio7b0_sel GPIO7B[0] iomux select 2'b00: gpio 2'b01: uart3gps_sout 2'b10: gps_sig 2'b11: hsadct1_data1

GRF_GPIO7CL_IOMUX
Address: Operational Base + offset (0x0074)
GPIO7CL iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:12	RW	0x0	gpio7c3_sel GPIO7C[3] iomux select 2'b00: gpio 2'b01: i2c5hdmi_sda 2'b10: edphdmii2c_sda 2'b11: reserved
11:9	RO	0x0	reserved
8	RW	0x0	gpio7c2_sel GPIO7C[2] iomux select 1'b0: gpio 1'b1: i2c4tp_scl
7:5	RO	0x0	reserved
4	RW	0x0	gpio7c1_sel GPIO7C[1] iomux select 1'b0: gpio 1'b1: i2c4tp_sda
3:2	RO	0x0	reserved
1:0	RW	0x0	gpio7c0_sel GPIO7C[0] iomux select 2'b00: gpio 2'b01: isp_flashtrigin 2'b10: edphdmi_cecinoutt1 2'b11: reserved

GRF_GPIO7CH_IOMUX
Address: Operational Base + offset (0x0078)
GPIO7CH iomux control

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio7c7_sel GPIO7C[7] iomux select 3'b000: gpio 3'b001: uart2dbg_sout 3'b010: uart2dbg_sirout 3'b011: pwm_3 3'b100: edphdmi_cecinout other: reserved
11:10	RO	0x0	reserved
9:8	RW	0x0	gpio7c6_sel GPIO7C[6] iomux select 2'b00: gpio 2'b01: uart2dbg_sin 2'b10: uart2dbg_sirin 2'b11: pwm_2
7:2	RO	0x0	reserved
1:0	RW	0x0	gpio7c4_sel GPIO7C[4] iomux select 2'b00: gpio 2'b01: i2c5hdmi_scl 2'b10: edphdmii2c_scl 2'b11: reserved

GRF_GPIO8A_IOMUX
Address: Operational Base + offset (0x0080)
GPIO8A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio8a7_sel GPIO8A[7] iomux select 2'b00: gpio 2'b01: spi2_csn0 2'b10: sc_detect 2'b11: reserve
13:12	RW	0x0	gpio8a6_sel GPIO8A[6] iomux select 2'b00: gpio 2'b01: spi2_clk 2'b10: sc_io 2'b11: reserve
11:10	RW	0x0	gpio8a5_sel GPIO8A[5] iomux select 2'b00: gpio 2'b01: i2c2sensor_scl 2'b10: sc_clk 2'b11: reserved
9:8	RW	0x0	gpio8a4_sel GPIO8A[4] iomux select 2'b00: gpio 2'b01: i2c2sensor_sda 2'b10: sc_rst 2'b11: reserved
7:6	RW	0x0	gpio8a3_sel GPIO8A[3] iomux select 2'b00: gpio 2'b01: spi2_csn1 2'b10: sc_iot1 2'b11: reserved
5	RO	0x0	reserved
4	RW	0x0	gpio8a2_sel GPIO8A[2] iomux select 1'b0: gpio 1'b1: sc_detectt1
3:2	RW	0x0	gpio8a1_sel GPIO8A[1] iomux select 2'b00: gpio 2'b01: ps2_data 2'b10: sc_vcc33v 2'b11: reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio8a0_sel GPIO8A[0] iomux select 2'b00: gpio 2'b01: ps2_clk 2'b10: sc_vcc18v 2'b11: reserved

GRF_GPIO8B_IOMUX
Address: Operational Base + offset (0x0084)
GPIO8B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:4	RO	0x0	reserved
3:2	RW	0x0	gpio8b1_sel GPIO8B[1] iomux select 2'b00: gpio 2'b01: spi2_txd 2'b10: sc_clk 2'b11: reserve
1:0	RW	0x0	gpio8b0_sel GPIO8B[0] iomux select 2'b00: gpio 2'b01: spi2_rxd 2'b10: sc_rst 2'b11: reserve

GRF_GPIO1H_SR
Address: Operational Base + offset (0x0104)
GPIO1C/D SR control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x0f	gpio1d_sr GPIO1D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RO	0x0	reserved

GRF_GPIO2L_SR
Address: Operational Base + offset (0x0108)
GPIO2A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio2b_sr GPIO2B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio2a_sr GPIO2A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO2H_SR
Address: Operational Base + offset (0x010c)
GPIO2C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio2c_sr GPIO2C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO3L_SR
Address: Operational Base + offset (0x0110)
GPIO3A/B SR control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x20	gpio3b_sr GPIO3B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0xff	gpio3a_sr GPIO3A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO3H_SR
Address: Operational Base + offset (0x0114)
GPIO3C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:8	RW	0xff	gpio3d_sr GPIO3D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x04	gpio3c_sr GPIO3C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO4L_SR
Address: Operational Base + offset (0x0118)
GPIO4A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x01	gpio4b_sr GPIO4B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x20	gpio4a_sr GPIO4A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO4H_SR
Address: Operational Base + offset (0x011c)
GPIO4C/D SR control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio4d_sr GPIO4D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio4c_sr GPIO4C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO5L_SR
Address: Operational Base + offset (0x0120)
GPIO5A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bits 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	gpio5b_sr GPIO5B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RO	0x0	reserved

GRF_GPIO5H_SR
Address: Operational Base + offset (0x0124)
GPIO5C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio5c_sr GPIO5C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO6L_SR
Address: Operational Base + offset (0x0128)
GPIO6A/B SR control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x01	gpio6b_sr GPIO6B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio6a_sr GPIO6A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO6H_SR
Address: Operational Base + offset (0x012c)
GPIO6C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x10	gpio6c_sr GPIO6C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO7L_SR
Address: Operational Base + offset (0x0130)
GPIO7A/B SR control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio7b_sr GPIO7B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio7a_sr GPIO7A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO7H_SR
Address: Operational Base + offset (0x0134)
GPIO7C/D SR control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio7c_sr GPIO7C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO8L_SR
Address: Operational Base + offset (0x0138)
GPIO8A/B SR control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio8b_sr GPIO8B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio8a_sr GPIO8A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO1D_P
Address: Operational Base + offset (0x014c)
GPIO1D PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio1d_p GPIO1D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2A_P
Address: Operational Base + offset (0x0150)
GPIO2A PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio2a_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2B_P
Address: Operational Base + offset (0x0154)
GPIO2B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio2b_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2C_P
Address: Operational Base + offset (0x0158)
GPIO2C PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa5	gpio2c_p GPIO2C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3A_P
Address: Operational Base + offset (0x0160)
GPIO3A PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio3a_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3B_P
Address: Operational Base + offset (0x0164)
GPIO3B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5699	gpio3b_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3C_P
Address: Operational Base + offset (0x0168)
GPIO3C PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa5	gpio3c_p GPIO3C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3D_P
Address: Operational Base + offset (0x016c)
GPIO3D PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio3d_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4A_P
Address: Operational Base + offset (0x0170)
GPIO4A PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio4a_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4B_P
Address: Operational Base + offset (0x0174)
GPIO4B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa5	gpio4b_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4C_P
Address: Operational Base + offset (0x0178)
GPIO4C PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5559	gpio4c_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4D_P
Address: Operational Base + offset (0x017c)
GPIO4D PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5a99	gpio4d_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO5B_P
Address: Operational Base + offset (0x0184)
GPIO5B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x6559	gpio5b_p GPIO5B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO5C_P
Address: Operational Base + offset (0x0188)
GPIO5C PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa9	gpio5c_p GPIO5C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO6A_P
Address: Operational Base + offset (0x0190)
GPIO6A PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio6a_p GPIO6A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO6B_P
Address: Operational Base + offset (0x0194)
GPIO6B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaa96	gpio6b_p GPIO6B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO6C_P
Address: Operational Base + offset (0x0198)
GPIO6C PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5655	gpio6c_p GPIO6C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO7A_P
Address: Operational Base + offset (0x01a0)
GPIO7A PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x59aa	gpio7a_p GPIO7A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO7B_P
Address: Operational Base + offset (0x01a4)
GPIO7B PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xa696	gpio7b_p GPIO7B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO7C_P
Address: Operational Base + offset (0x01a8)
GPIO7C PU/PD control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5955	gpio7c_p GPIO7C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO8A_P
Address: Operational Base + offset (0x01b0)
GPIO8A PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x6555	gpio8a_p GPIO8A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO8B_P
Address: Operational Base + offset (0x01b4)
GPIO8B PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio8b_p GPIO8B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO1D_E
Address: Operational Base + offset (0x01cc)
GPIO1D drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x55aa	gpio1d_e GPIO1D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO2A_E
Address: Operational Base + offset (0x01d0)
GPIO2A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio2a_e GPIO2A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO2B_E
Address: Operational Base + offset (0x01d4)
GPIO2B drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio2b_e GPIO2B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO2C_E
Address: Operational Base + offset (0x01d8)
GPIO2C drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio2c_e GPIO2C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3A_E
Address: Operational Base + offset (0x01e0)
GPIO3A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio3a_e GPIO3A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3B_E
Address: Operational Base + offset (0x01e4)
GPIO3B drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5955	gpio3b_e GPIO3B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3C_E
Address: Operational Base + offset (0x01e8)
GPIO3C drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5565	gpio3c_e GPIO3C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3D_E
Address: Operational Base + offset (0x01ec)
GPIO3D drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio3d_e GPIO3D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4A_E
Address: Operational Base + offset (0x01f0)
GPIO4A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5955	gpio4a_e GPIO4A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4B_E
Address: Operational Base + offset (0x01f4)
GPIO4B drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5556	gpio4b_e GPIO4B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4C_E
Address: Operational Base + offset (0x01f8)
GPIO4C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio4c_e GPIO4C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4D_E
Address: Operational Base + offset (0x01fc)
GPIO4D drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio4d_e GPIO4D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO5B_E
Address: Operational Base + offset (0x0204)
GPIO5B drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio5b_e GPIO5B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO5C_E
Address: Operational Base + offset (0x0208)
GPIO5C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio5c_e GPIO5C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO6A_E
Address: Operational Base + offset (0x0210)
GPIO6A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio6a_e GPIO6A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO6B_E
Address: Operational Base + offset (0x0214)
GPIO6B drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio6b_e GPIO6B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO6C_E
Address: Operational Base + offset (0x0218)
GPIO6C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio6c_e GPIO6C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO7A_E
Address: Operational Base + offset (0x0220)
GPIO7A drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio7a_e GPIO7A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO7B_E
Address: Operational Base + offset (0x0224)
GPIO7B drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio7b_e GPIO7B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO7C_E
Address: Operational Base + offset (0x0228)
GPIO7C drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio7c_e GPIO7C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO8A_E
Address: Operational Base + offset (0x0230)
GPIO8A drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio8a_e GPIO8A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO8B_E
Address: Operational Base + offset (0x0234)
GPIO8B drive strength control

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio8b_e GPIO8B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO_SMT
Address: Operational Base + offset (0x0240)
GPIO smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x1	gpio8a1_smt GPIO8A_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
10	RW	0x1	gpio8a0_smt GPIO8A_0 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
9	RW	0x1	gpio7c4_smt GPIO7C_4 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
8	RW	0x1	gpio7c3_smt GPIO7C_3 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
7	RW	0x1	gpio7c2_smt GPIO7C_2 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
6	RW	0x1	gpio7c1_smt GPIO7C_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
5	RW	0x1	gpio2c1_smt GPIO2C_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
4	RW	0x1	gpio2c0_smt GPIO2C_0 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
3	RW	0x1	gpio6b2_smt GPIO6B_2 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
2	RW	0x1	gpio6b1_smt GPIO6B_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
1	RW	0x1	gpio8a5_smt GPIO8A_5 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio8a4_smt GPIO8A_4 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

GRF_SOC_CON0
Address: Operational Base + offset (0x0244)
SoC control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	pause_mmc_peri PERI MMC AHB bus arbiter pause control
14	RW	0x0	pause_emem_peri PERI EMEM AHB bus arbiter pause control
13	RW	0x0	pause_usb_peri PERI USB AHB bus arbiter pause control
12	RW	0x1	grf_force_jtag Force select jtag function from sdmmc0 IO
11	RW	0x1	grf_core_idle_req_mode_sel1 core idle request mode selection 1
10	RW	0x1	grf_core_idle_req_mode_sel0 core idle request mode selection 0
9	RW	0x0	ddr1_16bit_en DDR Channel 1 interface 16bit enable
8	RW	0x0	ddr0_16bit_en DDR Channel 0 interface 16bit enable
7	RW	0x0	vcodec_sel vdpu vepu clock select 1'b0: select vepu aclk as vcodec main clock 1'b1: select vdpu aclk as vcodec main clock

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Bit	Attr	Reset Value	Description
6	RW	0x0	upctl1_c_active_in Channel 1 DDR clock active in External signal from system that flags if a hardware low power request can be accepted or should always be denied. 1'b0: may be accepted 1'b1: will be denied
5	RW	0x0	upctl0_c_active_in Channel 0 DDR clock active in External signal from system that flags if a hardware low power request can be accepted or should always be denied. 1'b0: may be accepted 1'b1: will be denied
4	RW	0x1	msch1_mainddr3 Channel 1 DDR3 mode control 1'b1: DDR3 mode
3	RW	0x1	msch0_mainddr3 Channel 0 DDR3 mode control 1'b1: DDR3 mode
2	RW	0x0	msch1_mainpartialpop msch1_mainpartialpop bit control
1	RW	0x0	msch0_mainpartialpop msch0_mainpartialpop bit control
0	RO	0x0	reserved

GRF_SOC_CON1
Address: Operational Base + offset (0x0248)
SoC control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x1	rmii_mode RMII mode selection 1'b1: RMII mode
13:12	RW	0x0	gmac_clk_sel RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
11	RW	0x0	rmii_clk_sel RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz
10	RW	0x0	gmac_speed MAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
9	RW	0x0	gmac_flowctrl GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
8:6	RW	0x1	gmac_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
5	RW	0x0	host_remap Host interface remap control
4:0	RO	0x0	reserved

GRF_SOC_CON2

Address: Operational Base + offset (0x024c)

SoC control register 2

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13	RW	0x0	upctl1_lpddr3_odt_en Channel 1 DDR odt enable in LPDDR3 mode 1'b1: ODT enable 1'b0: ODT disable
12	RW	0x0	upctl1_bst_diable Channel 1 DDR controller burst termination disable control 1'b1: disable 1'b0: enable
11	RW	0x0	lpddr3_en1 Channel 1 LPDDR3 mode control 1'b1: LPDDR3 mode
10	RW	0x0	upctl0_lpddr3_odt_en Channel 0 DDR odt enable in LPDDR3 mode 1'b1: ODT enable 1'b0: ODT disable
9	RW	0x0	upctl0_bst_diable Channel 0 DDR controller burst termination disable control 1'b1: disable 1'b0: enable
8	RW	0x0	lpddr3_en0 Channel 0 LPDDR3 mode control 1'b1: LPDDR3 mode

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Bit	Attr	Reset Value	Description
7	RW	0x0	grf_poc_flash0_ctrl Flash0 IO domain 1.8V selection source 1'b0: GPIO3C_3 to decide the flash0 IO domain voltage, when GPIO3C_3 high, the voltage is 1.8V 1'b1: grf_io_vsel[2] to decide the flash0 IO domain voltage, when grf_io_vsel[2] high, the voltage is 1.8V
6	RW	0x0	simcard_mux_sel sim card iomux solution selection 1'b1: use GPIO8A[5:2] 1'b0: use GPIO8A[7:6] and GPIO8B[1:0]
5:2	RO	0x0	reserved
1	RW	0x1	grf_spdif_2ch_en SPDIF solution selection 1'b0: 8CH SPDIF 1'b1: 2CH SPDIF
0	RW	0x0	pwm_sel PWM solution selection 1'b1: RK PWM 1'b0: PWM(old)

GRF_SOC_CON3
Address: Operational Base + offset (0x0250)
SoC control register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	rxclk_dly_ena_gmac RGMII RX clock delayline enable 1'b1: enable 1'b0: disable

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Bit	Attr	Reset Value	Description
14	RW	0x0	txclk_dly_ena_gmac RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
13:7	RW	0x10	clk_rx_dl_cfg_gmac RGMII RX clock delayline value
6:0	RW	0x10	clk_tx_dl_cfg_gmac RGMII TX clock delayline value

GRF_SOC_CON4
Address: Operational Base + offset (0x0254)
SoC control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	dfi_eff_stat_en1 Channel 1 DFI monitor efficiency statistics enable
14	RW	0x0	dfi_eff_stat_en0 Channel 0 DFI monitor efficiency statistics enable
13	RW	0x0	mobile_ddr_sel Mobile DDR selection in DFI monitor 1'b1: mobile DDR(LPDDR2/LPDDR3) 1'b0: DDR3
12:10	RW	0x1	host_l3_ocp_sconnect_grf Host interface l3_ocp_sconnect signal control
9:8	RW	0x2	host_txport_rst_val_grf Host interface txport_rst_val signal control
7:6	RW	0x0	host_rxport_rst_val_grf Host interface rxport_rst_val signal control

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Bit	Attr	Reset Value	Description
5	RW	0x0	host_wakereq_grf Host interface wakereq signal control
4:3	RW	0x0	host_eoi_in_grf Host interface eoi_in signal control
2	RW	0x1	host_mstandy_in_grf Host interface mstandy_in signal control
1	RW	0x1	host_mwait_grf Host interface mwait signal control
0	RW	0x1	host_sidle_req_grf Host interface sidle_req signal control

GRF_SOC_CON5
Address: Operational Base + offset (0x0258)
SoC control register 5

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	host_mux_sel Host interface mux selection 1'b1: 8bits input, 16bits output 1'b0: 8bits output, 16bits input
14	RW	0x0	tsp0_inout_sel TSP0 input/output selection 1'b1: output 1'b0: input
13	RW	0x0	hsadc_clkout_en hsadc clkout enable 1'b1: hsadc_clkout 1'b0: gps_clk
12:3	RW	0x190	host_fclk_freq_rst_val_grf Host interface fclk_freq_rst_val signal control

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Bit	Attr	Reset Value	Description
2:1	RW	0x3	host_l3_iocp_mconnect_grf Host interface l3_iocp_mconnect signal control
0	RW	0x1	host_l3_ocp_mdiscbehave_grf Host interface l3_ocp_mdiscbehave signal control

GRF_SOC_CON6
Address: Operational Base + offset (0x025c)
SoC control register 6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	grf_hdmi_edp_sel HDMI source selection 1'b1: from HDMI controller 1'b0: from eDP controller
14	RW	0x0	dsi_csi_testbus_sel MIPI PHY TX1RX1 test bus source selection 1'b1: CSI host 1'b0: DSI host1
13	RW	0x0	hsadc_extclk_mux_sel HSADC external clock source selection 1'b1: GPIO7B[1] 1'b0: GPIO2B[2]
12	RW	0x0	clk_27m_mux_sel 27M clock input source selection 1'b1: GPIO0C[1] 1'b0: GPIO0B[5]
11	RW	0x0	grf_con_dsi1_dpicolorm DSI host1 dpicolorm bit control

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Bit	Attr	Reset Value	Description
10	RW	0x0	grf_con_dsi1_dpishutdn DSI host1 dpishutdn bit control
9	RW	0x0	grf_con_dsi1_lcdc_sel DSI host1 data from VOP selection 1'b1: VOP LIT output to DSI host1 1'b0: VOP BIG output to DSI host1
8	RW	0x0	grf_con_dsi0_dpicolorm DSI host0 dpicolorm bit control
7	RW	0x0	grf_con_dsi0_dpishutdn DSI host0 dpishutdn bit control
6	RW	0x0	grf_con_dsi0_lcdc_sel DSI host0 data from VOP selection 1'b1: VOP LIT output to DSI host0 1'b0: VOP BIG output to DSI host0
5	RW	0x0	grf_con_edp_lcdc_sel eDP data from VOP selection 1'b1: VOP LIT output to eDP 1'b0: VOP BIG output to eDP
4	RW	0x0	grf_con_hdmi_lcdc_sel HDMI data from VOP selection 1'b1: VOP LIT output to HDMI 1'b0: VOP BIG output to HDMI
3	RW	0x0	grf_con_lvds_lcdc_sel LVDS data from VOP selection 1'b1: VOP LIT output to LVDS 1'b0: VOP BIG output to LVDS
2	RW	0x0	grf_con_iep_vop_sel IEP connect to VOP selection 1'b1: IEP connect to VOP LIT 1'b0: IEP connect to VOP BIG
1	RW	0x0	grf_con_isp_dphy_sel ISP connect to MIPI PHY selection 1'b1: MIPI PHY TX1RX1 1'b0: MIPI PHY RX0
0	RW	0x0	grf_con_disable_isp Disable ISP control

GRF_SOC_CON7
Address: Operational Base + offset (0x0260)
SoC control register 7

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_lvds_pwrdwn LVDS PHY power down control 1'b1: power down 1'b0: power up
14	RO	0x0	reserved
13	RW	0x0	grf_lvds_lcdc_trace_sel LVDS IO used as trace bus enable 1'b1: used as trace bus 1'b0: used as LVDS IO or LCDC RGB output port
12	RW	0x0	grf_lvds_con_enable_2 LVDS controller enable_2 signal control
11	RW	0x0	grf_lvds_con_enable_1 LVDS controller enable_1 signal control
10	RW	0x0	grf_lvds_con_den_polarity LVDS controller den_polarity signal control
9	RW	0x0	grf_lvds_con_hs_polarity LVDS controller hs_polarity signal control
8	RW	0x0	grf_lvds_con_clkinv LVDS controller clkinv signal control
7	RW	0x0	grf_lvds_con_startphase LVDS controller startphase signal control
6	RW	0x0	grf_lvds_con_ttl_en LVDS controller ttl_en signal control
5	RW	0x0	grf_lvds_con_startsel LVDS controller startsel signal control
4	RW	0x0	grf_lvds_con_chasel LVDS controller chasel signal control
3	RW	0x0	grf_lvds_con_msbsel LVDS controller msbsel signal control

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	grf_lvds_con_select LVDS controller select signal control

GRF_SOC_CON8
Address: Operational Base + offset (0x0264)
SoC control register 8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_edp_hdcp_protect eDP HDCP function protection 1'b1: protect 1'b0: not protect
14	RW	0x0	grf_edp_bist_en eDP PHY BIST function enabled 1'b1: enable 1'b0: disable
13	RW	0x0	grf_edp_mem_ctrl_sel eDP memory control selection 1'b1: controlled by eDP controller internal logic 1'b0: controlled by APB BUS
12	RW	0x0	grf_hdmi_cec_mux_sel HDMI cec source selection 1'b1: from GPIO7C[0] 1'b0: from GPIO7C[7]
11:8	RW	0x0	grf_dphy_tx0_forcetxstopmode MIPI DPHY TX0 force lane into transmit mode and generate stop sate. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	grf_dphy_tx0_forcerxmode MIPI DPHY TX0 force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
3:0	RW	0xe	grf_dphy_tx0_turndisable MIPI DPHY TX0 disable turn around control Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON9
Address: Operational Base + offset (0x0268)
SoC control register 9

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	grf_dphy_tx1rx1_enable MIPI DPHY TX1RX1 enable lane N module(N=0~3). Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
11:8	RW	0x0	grf_dphy_tx1rx1_forcetxstopmode MIPI DPHY TX1RX1 force lane into transmit mode and generate stop sate. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
7:4	RW	0x0	grf_dphy_tx1rx1_forcerxmode MIPI DPHY TX1RX1 force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

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Bit	Attr	Reset Value	Description
3:0	RW	0xe	grf_dphy_tx1rx1_turndisable MIPI DPHY TX1RX1 disable turn around control Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON10
Address: Operational Base + offset (0x026c)
SoC control register 10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	grf_dphy_rx0_enable MIPI DPHY RX0 enable lane N module(N=0~3). Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
11:8	RW	0x0	grf_dphy_rx0_forcetxstopmode MIPI DPHY RX0 force lane into transmit mode and generate stop sate. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
7:4	RW	0x0	grf_dphy_rx0_forcerxmode MIPI DPHY RX0 force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
3:0	RW	0xf	grf_dphy_rx0_turndisable MIPI DPHY RX0 disable turn around control Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

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GRF_SOC_CON11
Address: Operational Base + offset (0x0270)
SoC control register 11

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gpio8_a2_fall_edge_irq_pd GIIO8A[2] fall edge interrupt pending status 1'b1: enable 1'b0: disable
14	RW	0x0	gpio8_a2_fall_edge_irq_en GIIO8A[2] fall edge interrupt enable 1'b1: enable 1'b0: disable
13	RW	0x0	gpio8_a2_rise_edge_irq_pd GIIO8A[2] rise edge interrupt pending status 1'b1: enable 1'b0: disable
12	RW	0x0	gpio8_a2_rise_edge_irq_en GIIO8A[2] rise edge interrupt enable 1'b1: enable 1'b0: disable
11	RW	0x0	gpio7_c6_fall_edge_irq_pd GIIO7C[6] fall edge interrupt pending status 1'b1: enable 1'b0: disable
10	RW	0x0	gpio7_c6_fall_edge_irq_en GIIO7C[6] fall edge interrupt enable 1'b1: enable 1'b0: disable

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Bit	Attr	Reset Value	Description
9	RW	0x0	gpio7_c6_rise_edge_irq_pd GIIO7C[6] rise edge interrupt pending status 1'b1: enable 1'b0: disable
8	RW	0x0	gpio7_c6_rise_edge_irq_en GIIO7C[6] rise edge interrupt enable 1'b1: enable 1'b0: disable
7	RW	0x0	gpio7_b3_fall_edge_irq_pd GIIO7B[3] fall edge interrupt pending status 1'b1: enable 1'b0: disable
6	RW	0x0	gpio7_b3_fall_edge_irq_en GIIO7B[3] fall edge interrupt enable 1'b1: enable 1'b0: disable
5	RW	0x0	gpio7_b3_rise_edge_irq_pd GIIO7B[3] rise edge interrupt pending status 1'b1: enable 1'b0: disable
4	RW	0x0	gpio7_b3_rise_edge_irq_en GIIO7B[3] rise edge interrupt enable 1'b1: enable 1'b0: disable
3	RW	0x0	sd_detectn_fall_edge_irq_pd sdmmc detect_n fall edge interrupt pending status 1'b1: enable 1'b0: disable
2	RW	0x0	sd_detectn_fall_edge_irq_en sdmmc0 detect_n signal fall edge interrupt enable 1'b1: enable 1'b0: disable
1	RW	0x0	sd_detectn_rise_edge_irq_pd sdmmc detect_n rise edge interrupt pending status 1'b1: enable 1'b0: disable
0	RW	0x0	sd_detectn_rise_edge_irq_en sdmmc0 detect_n signal rise edge interrupt enable 1'b1: enable 1'b0: disable

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GRF_SOC_CON12
Address: Operational Base + offset (0x0274)
SoC control register 12

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RW	0x000	grf_edp_frq_vid_ck_in eDP PHY frequency information of vid_ck_in frq_vid_ck_in<8:0>/8 = freq(vid_ck_in)/10
6	RW	0x0	grf_edp_vid_lock eDP PHY input video PLL stable indicator 1'b1: stable 1'b0: unstable
5	RW	0x0	grf_edp_iddq_en eDP PHY IDDQ enable 1'b0: disable 1'b1: enable, all circuits are power down, all IO are high-z
4	RW	0x1	grf_edp_ref_clk_sel eDP PHY reference clock source selection 1'b0: from PAD(IO_EDP_OSC_CLK_24M) 1'b1: from internal 24MHz or 27MHz clock
3	RW	0x0	grf_edp_dc_tp_i eDP PHY analog DC test point input
2	RO	0x0	reserved
1:0	RW	0x3	grf_filter_cnt_sel the counter select for sd card detect filter 2'b00: 5ms 2'b01: 15ms 2'b10: 35ms 2'b11: 50ms

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GRF_SOC_CON13
Address: Operational Base + offset (0x0278)
SoC control register 13

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	grf_edp_tx_bscan_data eDP TX boundary data bit0: boundary data to ch0 bit1: boundary data to ch1 bit2: boundary data to ch2 bit3: boundary data to ch3
11	RW	0x0	grf_edp_tx_bscan_en eDP TX boundary enable 1'b0: disable 1'b1: enable
10	RO	0x0	reserved
9:5	RW	0x00	grf_uart_rts_sel UART polarity selection for rts port Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT. 1'b1: high asserted 1'b0: low asserted
4:0	RW	0x00	grf_uart_cts_sel UART polarity selection for cts port Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT. 1'b1: high asserted 1'b0: low asserted

GRF_SOC_CON14

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Address: Operational Base + offset (0x027c)
SoC control register 14

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_dphy_tx1rx1_basedir MIPI DPHY TX1RX1 base direction control
14	RW	0x0	grf_dphy_tx1rx1_masterslavez MIPI DPHY TX1RX1 master/slave control
13	RW	0x0	dphy_rx1_src_sel MIPI DPHY RX1 source selection 1'b1: isp 1'b0: csi host
12	RW	0x0	dphy_tx1rx1_enableclk MIPI DPHY TX1RX1 enable clock Lane module
11	RO	0x0	reserved
10:3	RW	0x00	dphy_rx0_testdin MIPI DPHY RX0 test bus input data
2	RW	0x0	dphy_rx0_testen MIPI DPHY RX0 test bus enable
1	RW	0x0	dphy_rx0_testclk MIPI DPHY RX0 test bus clock
0	RW	0x0	dphy_rx0_testclr MIPI DPHY RX0 test bus clear control

GRF_SOC_STATUS0
Address: Operational Base + offset (0x0280)
SoC status register 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ddrupctl1_bbflags DDR channel 1 NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes. Bit0 indication Bank0 busy, bit1 indication Bank1 busy, and so on.
15:0	RW	0x0000	ddrupctl0_bbflags DDR channel 0 NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes. Bit0 indication Bank0 busy, bit1 indication Bank1 busy, and so on.

GRF_SOC_STATUS1
Address: Operational Base + offset (0x0284)
SoC status register 1

Bit	Attr	Reset Value	Description
31	RW	0x0	gmac_portselect MAC Port Select A high indicates an MII interface, and a low a GMII interface.
30:26	RO	0x0	reserved
25:22	RW	0x0	reserved
21:16	RW	0x00	reserved
15:13	RW	0x0	ddrupctl1_stat 3'b000: Init_mem 3'b001: Config 3'b010: Config_req 3'b011: Access 3'b100: Access_req 3'b101: Low_power 3'b110: Low_power_entry_req 3'b111: Low_power_exit_req

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Bit	Attr	Reset Value	Description
12:10	RW	0x0	ddrupctl0_stat 3'b000: Init_mem 3'b001: Config 3'b010: Config_req 3'b011: Access 3'b100: Access_req 3'b101: Low_power 3'b110: Low_power_entry_req 3'b111: Low_power_exit_req
9	RW	0x0	newpll_lock NEW PLL lock status
8	RW	0x0	generalpll_lock GENERAL PLL lock status
7	RW	0x0	codecpll_lock CODEC PLL lock status
6	RW	0x0	armpll_lock ARM PLL lock status
5	RW	0x0	ddrpll_lock DDR PLL lock status
4	RW	0x0	newpll_clk NEW PLL clock output
3	RW	0x0	generalpll_clk GENERAL PLL clock output
2	RW	0x0	codecpll_clk CODEC PLL clock output
1	RW	0x0	armpll_clk ARM PLL clock output
0	RW	0x0	ddrpll_clk DDR PLL clock output

GRF_SOC_STATUS2
Address: Operational Base + offset (0x0288)
SoC status register 2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	usbhost0_stat_ohci_bufacc USB HOST0 ohci_bufacc signal status
29	RW	0x0	usbhost0_stat_ohci_rmtwkp USB HOST0 ohci_rmtwkp signal status
28:27	RW	0x0	usbhost0_utmi_linestate USB HOST0 utmi_linestate signal status
26	RW	0x0	usbhost0_stat_ohci_drwe USB HOST0 ohci_drwe signal status

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Bit	Attr	Reset Value	Description
25	RW	0x0	usbhost0_stat_ohci_rwe USB HOST0 ohci_rwe signal status
24	RW	0x0	usbhost0_stat_ohci_ccs USB HOST0 ohci_ccs signal status
23	RW	0x0	usbhost1_utmiotg_iddig USB HOST1 utmiotg_iddig signal status
22:21	RW	0x0	usbhost1_utmi_linestate USB HOST1 utmi_linestate signal status
20	RW	0x0	usbhost1_utmisrp_bvalid USB HOST1 utmisrp_bvalid signal status
19	RW	0x0	usbhost1_utmiotg_vbusvalid USB HOST1 utmiotg_vbusvalid signal status
18	RW	0x0	usbhost1_chirp_on USB HOST1 chirp_on signal status
17	RW	0x0	usbotg_utmiotg_iddiq USB OTG utmiotg_iddig signal status
16:15	RW	0x0	usbotg_utmi_linestate USB OTG utmi_linestate signal status
14	RW	0x0	usbotg_utmisrp_bvalid USB OTG utmisrp_bvalid
13	RW	0x0	usbotg_utmiotg_vbusvalid USB OTG utmiotg_vbusvalid signal status
12	RO	0x0	reserved
11	RW	0x0	reserved
10:0	RW	0x000	reserved

GRF_SOC_STATUS3
Address: Operational Base + offset (0x028c)
SoC status register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo0 DDR channel0 NIF interface FIFO0 status

GRF_SOC_STATUS4
Address: Operational Base + offset (0x0290)
SoC status register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo1 DDR channel0 NIF interface FIFO1 status

GRF_SOC_STATUS5
Address: Operational Base + offset (0x0294)
SoC status register 5

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo2 DDR channel0 NIF interface FIFO2 status

GRF_SOC_STATUS6
Address: Operational Base + offset (0x0298)
SoC status register 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo3 DDR channel0 NIF interface FIFO3 status

GRF_SOC_STATUS7
Address: Operational Base + offset (0x029c)
SoC status register 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo0 DDR channel1 NIF interface FIFO0 status

GRF_SOC_STATUS8
Address: Operational Base + offset (0x02a0)
SoC status register 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo1 DDR channel1 NIF interface FIFO1 status

GRF_SOC_STATUS9
Address: Operational Base + offset (0x02a4)
SoC status register 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo2 DDR channel1 NIF interface FIFO2 status

GRF_SOC_STATUS10
Address: Operational Base + offset (0x02a8)
SoC status register 10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo3 DDR channel1 NIF interface FIFO3 status

GRF_SOC_STATUS11
Address: Operational Base + offset (0x02ac)
SoC status register 11

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_eff_wr_num DDR channel0 DFI interface write command number

GRF_SOC_STATUS12
Address: Operational Base + offset (0x02b0)
SoC status register 12

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_eff_rd_num DDR channel0 DFI interface read command number

GRF_SOC_STATUS13
Address: Operational Base + offset (0x02b4)
SoC status register 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_eff_act_num DDR channel0 DFI interface active command number

GRF_SOC_STATUS14
Address: Operational Base + offset (0x02b8)
SoC status register 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_timer_val DDR channel0 DFI interface statistics timer value

GRF_SOC_STATUS15
Address: Operational Base + offset (0x02bc)
SoC status register 15

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_eff_wr_num DDR channel1 DFI interface write command number

GRF_SOC_STATUS16
Address: Operational Base + offset (0x02c0)
SoC status register 16

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_eff_rd_num DDR channel1 DFI interface read command number

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GRF_SOC_STATUS17
Address: Operational Base + offset (0x02c4)
SoC status register 17

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_eff_act_num DDR channel1 DFI interface active command number

GRF_SOC_STATUS18
Address: Operational Base + offset (0x02c8)
SoC status register 18

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_timer_val DDR channel1 DFI interface statistics timer value

GRF_SOC_STATUS19
Address: Operational Base + offset (0x02cc)
SoC status register 19

Bit	Attr	Reset Value	Description
31	RW	0x0	usbhost1_fsvminus USB HOST1 PHY fsvminus bit status
30	RW	0x0	usbhost1_fsvplus USB HOST1 PHY fsvplus bit status
29	RW	0x0	usbhost1_chgdet USB HOST1 PHY charge detect status
28	RW	0x0	usbhost0_fsvminus USB HOST0 PHY fsvminus bit status
27	RW	0x0	usbhost0_fsvplus USB HOST0 PHY fsvplus bit status
26	RW	0x0	usbhost0_chgdet USB HOST0 PHY charge detect status
25	RW	0x0	usbotg_fsvminus USB OTG PHY fsvminus bit status
24	RW	0x0	usbotg_fsvplus USB OTG PHY fsvplus bit status
23	RW	0x0	usbotg_chgdet USB OTG PHY charge detect status
22:14	RO	0x0	reserved
13:11	RW	0x0	host_l3_ocp_sconnect Host interface L3 OCP sconnect status
10	RW	0x0	host_l3_ocp_tactive Host interface L3 OCP tactive status
9:8	RW	0x0	host_l3_ocp_mconnect Host interface L3 OCP mconnect status

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Bit	Attr	Reset Value	Description
7	RW	0x0	host_wakeack Host interface wakeack status
6:5	RW	0x0	host_eoi_out Host interface eoi_out status
4	RW	0x0	host_mwait_out Host interface mwait_out status
3	RW	0x0	host_mwakeup Host interface mwakeup status
2	RW	0x0	host_mstandby Host interface mstandby status
1:0	RW	0x0	host_sidle_ack Host interface sidle ack

GRF_SOC_STATUS20
Address: Operational Base + offset (0x02d0)
SoC status register 20

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	host_geno Host interface geno bit stauts The GENI GENO is a mechanism that allows the 2 chip to exchange flags (interupts), up to 32 independent flags are available.

GRF_SOC_STATUS21
Address: Operational Base + offset (0x02d4)
SoC status register 21

Bit	Attr	Reset Value	Description
31:26	RW	0x00	usbhost0_stat_ehci_usbsts USB host0 ehci_usbsts bit status
25:15	RW	0x000	usbhost0_stat_ehci_xfer_cnt USB host0 ehci_xfer counter status
14	RW	0x0	usbhost0_stat_ehci_xfer_prdc USB host0 ehci_xfer_prdc bit status
13:10	RW	0x0	usbhost0_stat_ehci_lpsmc_state USB host0 ehci_lpsmc_state bit status
9	RW	0x0	usbhost0_stat_ehci_bufacc USB host0 ehci_bufacc bit status
8	RW	0x0	usbhost0_stat_ohci_globalsuspend USB host0 ohci_globalsuspend bit status
7:0	RW	0x00	dphy_rx0_testdout MIPI DPHY RX0 test bus data output

GRF_PERIDMAC_CON0
Address: Operational Base + offset (0x02e0)

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PERI DMAC control register 0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	peridmac_boot_addr peridmac_boot_addr[19:12] PERI DMAC boot_addr[19:12] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
7:4	RW	0xf	peridmac_boot_periph_ns peridmac_boot_periph_ns[19:16] PERI DMAC boot_peri_ns input control Controls the security state of a peripheral request interface, when the PERI DMAC exits from reset. Note: PERI DMAC don't support secure feature, these bits don't need to be configured
3	RW	0x1	peridmac_boot_manager_ns PERI DMAC boot_manager_ns input control When the DMAC exits from reset , this signal controls the security state of the DMA manager thread: 1'b0: assigns DMA manager to the secure state 1'b1: assigns DMA manager to the Non-secure state

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Bit	Attr	Reset Value	Description
2:1	RW	0x1	grf_drtype_peridmac PERI DMAC type of acknowledgement or request for peripheral signals: 2'b00: single level request 2'b01: burst level request 2'b10: acknowledging a flush request 2'b11: reserved
0	RW	0x0	peridmac_boot_from_pc PERI DMAC boot_from_pc input control Controls the location in which the DMAC0 executes its initial instruction, after it exits from reset : 1'b0: DMAC waits for an instruction from APB interface 1'b1: DMAC manager thread executes the instruction that is located at the address that boot_addr[31:0] provided.

GRF_PERIDMAC_CON1
Address: Operational Base + offset (0x02e4)
PERI DMAC control register 1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:0	RW	0x000	peridmac_boot_addr peridmac_boot_addr[31:20] PERI DMAC boot_addr[31:20] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.

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GRF_PERIDMAC_CON2
Address: Operational Base + offset (0x02e8)
PERI DMAC control register 2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xffff	peridmac_boot_irq_ns PERI DMAC boot_irq_ns input control Controls the security state of an event-interrupt resource , when the PERI DMAC exits from reset. Note : PERI DMAC don't support secure feature, these bits don't need to be configured.

GRF_PERIDMAC_CON3
Address: Operational Base + offset (0x02ec)
PERI DMAC control register 3

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xffff	peridmac_boot_periph_ns PERI DMAC boot_peri_ns input control Controls the security state of a peripheral request interface, when the DMAC exits from reset. Note: PERI DMAC don't support secure feature, these bits don't need to be configured.

GRF_DDRC0_CON0
Address: Operational Base + offset (0x02f0)
DDRC0 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:11	RW	0x0	ddr0_dto_lb DDR0 DTO I/O internal loopback enable
10:9	RW	0x0	ddr0_dto_te DDR0 DTO I/O on-die termination enable
8:7	RW	0x0	ddr0_dto_pdr DDR0 DTO I/O receiver power down
6:5	RW	0x0	ddr0_dto_pdd DDR0 DTO I/O driver power down
4:3	RW	0x0	ddr0_dto_iom DDR0 DTO I/O mode select
2:1	RW	0x0	ddr0_dto_oe DDR0 DTO I/O output enable
0	RW	0x0	ddr0_ato_ae Enables, if set, the analog test output I/O. Connects to the AE pin of the analog test output I/O

GRF_DDRC1_CON0
Address: Operational Base + offset (0x02f4)
DDRC1 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:11	RW	0x0	ddr1_dto_lb DDR1 DTO I/O internal loopback enable
10:9	RW	0x0	ddr1_dto_te DDR1 DTO I/O on-die termination enable
8:7	RW	0x0	ddr1_dto_pdr DDR1 DTO I/O receiver power down
6:5	RW	0x0	ddr1_dto_pdd DDR1 DTO I/O driver power down

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	ddr1_dto_iom DDR1 DTO I/O mode select
2:1	RW	0x0	ddr1_dto_oe DDR1 DTO I/O output enable
0	RW	0x0	ddr1_ato_ae Enables, if set, the analog test output I/O. Connects to the AE pin of the analog test output I/O

GRF_CPU_CON0
Address: Operational Base + offset (0x02f8)
CPU control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	cfgaddrfilt_en_grf A17 cfgaddrfilt_en bit control
14	RO	0x0	reserved
13:10	RW	0x0	cfgend_a17 A17 cfgend bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
9	RW	0x1	tpiu_ctl_grf tpiu_ctl bit control
8:5	RW	0x1	cs_instid_grf Coresight cs_instid bit control
4	RW	0x0	l2rstdisable_grf A17 l2rstdisable bit control
3:0	RW	0x0	l1rstdisable_grf A17 l1rstdisable bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.

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GRF_CPU_CON1
Address: Operational Base + offset (0x02fc)
CPU control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0ff0	cfgaddrfilt_start_grf A17 non secure filter start address[15:0]

GRF_CPU_CON2
Address: Operational Base + offset (0x0300)
CPU control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0fff	cfgaddrfilt_end_grf A17 non secure filter end address[15:0]

GRF_CPU_CON3

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Address: Operational Base + offset (0x0304)
CPU control register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:8	RW	0x0	cfgnmfi_a17 A17 cfgnmfi bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
7:4	RW	0x0	cfgaddrfilt_end_grf A17 non secure filter end address[19:16]
3:0	RW	0x0	cfgaddrfilt_start_grf A17 non secure filter start address[19:16]

GRF_CPU_CON4
Address: Operational Base + offset (0x0308)
CPU control register 4

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RW	0x1	l2_mem_ema_grf L2 memory EMA control
12:10	RW	0x1	owl_mem_ema_grf A17 memory EMA control
9	RW	0x0	evento_clear A17 evento clear bit control
8	RW	0x0	eventi_a17 A17 eventi bit control
7:4	RO	0x0	reserved
3:0	RW	0x0	teinit_a17 A17 teinit bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.

GRF_CPU_STATUS0
Address: Operational Base + offset (0x0318)
CPU status register 0

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	evento_rising_edge evento signal rising edge
13:10	RW	0x0	owl_pmupl1_grf A17 PMU Privilege level 1 event Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
9:6	RW	0x0	owl_pmupl2_grf A17 PMU Privilege level 2 event Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	owl_pmusecure_grf A17 pmu secure event Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
1	RW	0x0	jtagnsw_st_grf JTAG nsw status
0	RW	0x0	jtagtop_st_grf JTAG top status

GRF_UOC0_CON0
Address: Operational Base + offset (0x0320)
UOC0 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbotg_linestate_irq_pd USB OTG linestate interrupt pending bit
14	RW	0x0	usbotg_linestate_irq_en USB OTG line state interrupt enable
13	RW	0x0	usbotg_siddq USB OTG IDDQ test enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.

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Bit	Attr	Reset Value	Description
12	RW	0x0	usbotg_port_reset USB OTG per-port reset When asserted, this customer-specific signal resets the corresponding port transmit and receive logic without disabling the clocks within the PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK cycles.
11:10	RO	0x0	reserved
9:8	RW	0x0	usbotg_scaledown_mode USB OTG scale down mode control
7:5	RW	0x4	usbotg_tune USB OTG VBUS valid threshold adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +9% 3'b110: +6% 3'b101: +3% 3'b100: Design default 3'b011: -3% 3'b010: -6% 3'b001: -9% 3'b000: -12%
4	RW	0x0	usbotg_disable USB OTG block disable 1'b1: the USB OTG block is power down 1'b0: the USB OTG block is power up
3:1	RW	0x4	usbotg_compdistune Disconnect Threshold Adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +4.5% 3'b110: +3% 3'b101: +1.5% 3'b100: Design default 3'b011: -1.5% 3'b010: -3% 3'b001: -4.5% 3'b000: -6%

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Bit	Attr	Reset Value	Description
0	RW	0x1	usbotg_common_on_n USB OTG common block power-down control This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend or Sleep mode. 1'b1: In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered.

GRF_UOC0_CON1
Address: Operational Base + offset (0x0324)
UOC0 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	usbotg_txrisetune USB OTG HS transmitter rise/fall time adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -20% 2'b10: -15% 2'b01: design default 2'b00: +10%

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Bit	Attr	Reset Value	Description
13:12	RW	0x3	usbotg_txhsxvtune USB OTG transmitter high-speed crossover adjustment This bus adjusts the voltage at which the DP and DM signals cross while transmitting in HS mode. 2'b11: Default setting 2'b10: +15 mV 2'b01: -15 mV 2'b00: Reserved
11:8	RW	0x3	usbotg_txvreftune USB OTG HS DC voltage level adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +8.75% 4'b1110: +7.5% 4'b1101: +6.25% 4'b1100: +5% 4'b1011: +3.75% 4'b1010: +2.5% 4'b1001: +1.25% 4'b1000: Design default 4'b0111: -1.25% 4'b0110: -2.5% 4'b0101: -3.75% 4'b0100: -5% 4'b0011: -6.25% 4'b0010: -7.5% 4'b0001: -8.75% 4'b0000: -10%
7:4	RW	0x3	usbotg_txfslstune USB OTG FS/LS source impedance adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -5% 4'b0111: -2.5% 4'b0011: Design default 4'b0001: +2.5% 4'b0000: +5%

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Bit	Attr	Reset Value	Description
3	RW	0x0	usbotg_txpreemppulsetune USB OTG HS transmitter pre-emphasis duration control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. transition in HS mode. 1'b1: 1X, short pre-emphasis current duration 1'b0: (desian default) 2X, long pre-emphasis currrent duration
2:0	RW	0x3	usbotg_sqrxtune USB OTG squelch threshold adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -20% 3'b110: -15% 3'b101: -10% 3'b100: -5% 3'b011: Design default 3'b010: +5% 3'b001: +10% 3'b000: +15%

GRF_UOC0_CON2
Address: Operational Base + offset (0x0328)
UOC0 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

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Bit	Attr	Reset Value	Description
15	RW	0x0	usbotg_acaenb USB OTG ACA ID_OTG pin resistance detection enable 1'b1: enable detection on resistance on the ID_OTG pin of an ACA 1'b0: disable detection on resistance on the ID_OTG pin of an ACA
14	RW	0x0	usbotg_dcdenb USB OTG data contact detection enable 1'b1: IDP_SRC current is sourced onto DP, pull-down resistance on DMA is enabled 1'b0: IDP_SRC current is disable, pull-down resistance on DM is disabled
13	RO	0x0	reserved
12:11	RW	0x1	usbotg_txrestune USB OTG source impedance adjustment 2'b11: source impedance is desreased by 4ohm 2'b10: source impedance is desreased by 2ohm 2'b01: design default 2'b00: source impedance is desreased by 1.5ohm
10	RW	0x1	usbotg_sleepm USB OTG sleep mode enable Asserting this signal place the USB PHY in sleep mode. 1'b0: sleep mode enable 1'b1: normal mode
9	RO	0x0	reserved
8	RW	0x1	usbotg_retenable_n USB OTG retention mode enable 0: retention mode enable 1: retention mode disable
7	RW	0x0	usbotg_vdatsrcenb USB OTG battery charging sourcing select 1'b1: data source voltage is enable 1'b0: data source voltage is disable
6	RW	0x0	usbotg_vdatdetenb USB OTG battery charging attach/connect detection enable 1'b1: enable 1'b0: disable

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Bit	Attr	Reset Value	Description
5	RW	0x0	usbotg_chrgsel USB OTG battery charging source select 1'b1: data source voltage is sourced onto DM and sunk from DP 1'b0: data source voltage is sourced onto DP and sunk from DM
4:3	RW	0x1	usbotg_txpreempamptune 2'b11: 3X pre-emphasis current 2'b10: 2X pre-emphasis current 2'b01: 1X pre-emphasis current 2'b00: HS Transmitter Pre-Emphasis is disabled
2	RW	0x0	usbotg_soft_con_sel 1'b0: software control usb otg disable 1'b1: software control usb otg enable
1	RW	0x0	usbotg_vbusvldextsel USB OTG external VBUS valid select This signal selects the VBUSVLDEXT input or the internal Session Valid comparator to indicate when the VBUS signal on the USB cable is valid. 1'b1: The VBUSVLDEXT input is used. 1'b0: The internal Session Valid comparator is used.
0	RW	0x0	usbotg_vbusvldext USB OTG external VBUS valid indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL signal is set to 1. VBUSVLDEXT indicates whether the VBUS signal on the USB cable is valid. In addition, BUSVLDEXT enables the pullup resistor on the D+ line. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.

GRF_UOC0_CON3
Address: Operational Base + offset (0x032c)
UOC0 control register 3

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbotg_dbnce_fltr_bypass USB OTG debounce filter bypass enable
14	RO	0x0	reserved
13	RW	0x0	usbotg_iddiq_sel USB OTG iddig soft control enable 1'b1: software control 1'b0: hardware control
12	RW	0x0	usbotg_iddiq USB OTG iddig software control bit
11:8	RO	0x0	reserved
7	RW	0x0	usbotg_bypasssel transmitter digital bypass select 1'b1: transmitter digital bypass mode is enabled 1'b0: transmitte digital bypass mode is disabled
6	RW	0x0	usbotg_bypassdmen DM0 transmitter digital bypass enable 1'b1: DM0 FS/LS driver is enabled and driven with the BYPASSDPDATA0 signals 1'b0: DM0 FS/LS driver is disabled in transmitter digital byapss mode
5	RW	0x0	usbotg_utmi_termselect USB OTG utmi termination select 1'b1: full speed terminations are enabled 1'b0: high speed terminations are enabled

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	usbotg_utmi_xcvrselect USB OTG utmi transceiver select 2'b11: sends an LS packet on an FS bus or receives an LS packet 2'b10: LS transceiver 2'b01: FS transceiver 2'b00: HS transceiver
2:1	RW	0x0	usbotg_utmi_opmode USB OTG utmi operation mode This controller bus selects the UTMI+ operation mode 2'b11: normal operation without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encoding 2'b01: no-driving 2'b00: normal
0	RW	0x1	usbotg_utmi_suspend_n USB OTG suspend mode enable 1'b1: normal operation mode 1'b0: suspend mode

GRF_UOC0_CON4
Address: Operational Base + offset (0x0330)
UOC0 control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7	RW	0x0	usbotg_id_fall_edge_irq_pd USB OTG id fall edge interrupt pending bit, write 1 to this bit , it will be cleared.

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Bit	Attr	Reset Value	Description
6	RW	0x0	usbotg_id_fall_edge_irq_en USB OTG id fall edge interrupt enable
5	RW	0x0	usbotg_id_rise_edge_irq_pd USB OTG id rise edge interrupt pending bit, write 1 to this bit , it will be cleared.
4	RW	0x0	usbotg_id_rise_edge_irq_en USB OTG id rise edge interrupt enable
3	RW	0x0	usbotg_bvalid_irq_pd USB OTG bvalid interrupt pending bit, write 1 to this bit, it will be cleared.
2	RW	0x0	usbotg_bvalid_irq_en USB OTG bvalid interrupt enable
1:0	RW	0x3	linestate_cnt_sel linestate signal filter time select 2'b00: 100us 2'b01: 500us 2'b10: 2.5ms 2'b11: 15ms

GRF_UOC1_CON0
Address: Operational Base + offset (0x0334)
UOC1 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_linestate_irq_pd USB HOST0 linestate interrupt pending bit
14	RW	0x0	usbhost0_linestate_irq_en USB HOST0 line state interrupt enable

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Bit	Attr	Reset Value	Description
13	RW	0x0	usbhost0_siddq USB HOST0 IDDQ test enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.
12	RW	0x0	usbhost0_port_reset USB HOST0 per-port reset When asserted, this customer-specific signal resets the corresponding port transmit and receive logic without disabling the clocks within the PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK cycles.
11	RW	0x1	usbhost0_word_if USB HOST0 word_if bit control
10	RW	0x0	usbhost0_sim_mode USB HOST0 sim_mode bit control
9	RW	0x1	usbhost0_incrx_en USB HOST0 incrx_en bit control
8	RW	0x1	usbhost0_incr8_en USB HOST0 incr8_en bit control
7:5	RW	0x4	usbhost0_tune USB HOST0 VBUS valid threshold adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +9% 3'b110: +6% 3'b101: +3% 3'b100: Design default 3'b011: -3% 3'b010: -6% 3'b001: -9% 3'b000: -12%
4	RW	0x0	usbhost0_disable USB HOST0 block disable 1'b1: the USB HOST0 block is power down 1'b0: the USB HOST0 block is power up

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Bit	Attr	Reset Value	Description
3:1	RW	0x4	usbhost0_compdistune USB HOST0 disconnect threshold adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +4.5% 3'b110: +3% 3'b101: +1.5% 3'b100: Design default 3'b011: -1.5% 3'b010: -3% 3'b001: -4.5% 3'b000: -6%
0	RW	0x1	usbhost0_common_on_n USB HOST0 common block power-down control This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend or Sleep mode. 1'b1: In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered.

GRF_UOC1_CON1
Address: Operational Base + offset (0x0338)
UOC1 control register 1

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	usbhost0_txrisetune USB HOST0 HS transmitter rise/fall time adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -20% 2'b10: -15% 2'b01: design default 2'b00: +10%
13:12	RW	0x3	usbhost0_txhsxvtune USB HOST0 transmitter high-speed crossover adjustment This bus adjusts the voltage at which the DP and DM signals cross while transmitting in HS mode. 2'b11: Default setting 2'b10: +15 mV 2'b01: -15 mV 2'b00: Reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x3	usbhost0_txvreftune USB HOST0 HS DC voltage level adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +8.75% 4'b1110: +7.5% 4'b1101: +6.25% 4'b1100: +5% 4'b1011: +3.75% 4'b1010: +2.5% 4'b1001: +1.25% 4'b1000: Design default 4'b0111: -1.25% 4'b0110: -2.5% 4'b0101: -3.75% 4'b0100: -5% 4'b0011: -6.25% 4'b0010: -7.5% 4'b0001: -8.75% 4'b0000: -10%
7:4	RW	0x3	usbhost0_txfslstune USB HOST0 FS/LS source impedance adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -5% 4'b0111: -2.5% 4'b0011: Design default 4'b0001: +2.5% 4'b0000: +5%
3	RW	0x0	usbhost0_txpreemppulsetune USB HOST0 HS transmitter pre-emphasis duration control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. transition in HS mode. 1'b1: 1X, short pre-emphasis current duration 1'b0: (desian default) 2X, long pre-emphasis currrent duration

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Bit	Attr	Reset Value	Description
2:0	RW	0x3	usbhost0_sqrxtune USB HOST0 squelch threshold adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -20% 3'b110: -15% 3'b101: -10% 3'b100: -5% 3'b011: Design default 3'b010: +5% 3'b001: +10% 3'b000: +15%

GRF_UOC1_CON2
Address: Operational Base + offset (0x033c)
UOC1 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_acaenb USB HOST0 ACA ID_OTG pin resistance detection enable 1'b1: enable detection on resistance on the ID_OTG pin of an ACA 1'b0: disable detection on resistance on the ID_OTG pin of an ACA

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Bit	Attr	Reset Value	Description
14	RW	0x0	usbhost0_dcdenb USB HOST0 data contact detection enable 1'b1: IDP_SRC current is sourced onto DP, pull-down resistance on DMA is enabled 1'b0: IDP_SRC current is disable, pull-down resistance on DM is disabled
13	RW	0x0	usbhost0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
12:11	RW	0x1	usbhost0_txrestune USB HOST0 source impedance adjustment 2'b11: source impedance is desreased by 4ohm 2'b10: source impedance is desreased by 2ohm 2'b01: design default 2'b00: source impedance is desreased by 1.5ohm
10	RW	0x1	usbhost0_sleepm USB HOST0 sleep mode enable Asserting this signal place the USB PHY in sleep mode. 1'b0: sleep mode enable 1'b1: normal mode
9	RW	0x0	usbhost0_autoppd_on_overcur USB HOST0 autoppd_on_overcur bit control
8	RW	0x1	usbhost0_retenable_n USB HOST0 retention mode enable 0: retention mode enable 1: retention mode disable
7	RW	0x0	usbhost0_vdatsrcenb USB HOST0 battery charging sourcing select 1'b1: data source voltage is enable 1'b0: data source voltage is disable
6	RW	0x0	usbhost0_vdatdetenb USB HOST0 battery charging attach/connect detection enable 1'b1: enable 1'b0: disable
5	RW	0x0	usbhost0_chrgsel USB HOST0 battery charging source select 1'b1: data source voltage is sourced onto DM and sunk from DP 1'b0: data source voltage is sourced onto DP and sunk from DM

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Bit	Attr	Reset Value	Description
4:3	RW	0x1	usbhost0_txpreempamptune 2'b11: 3X pre-emphasis current 2'b10: 2X pre-emphasis current 2'b01: 1X pre-emphasis current 2'b00: HS Transmitter Pre-Emphasis is disabled
2	RW	0x0	usbhost0_soft_con_sel 1'b0: software control usb host0 disable 1'b1: software control usb host0 enable
1	RW	0x0	usbhost0_vbusvldextsel USB HOST0 external VBUS valid select This signal selects the VBUSVLDEXT input or the internal Session Valid comparator to indicate when the VBUS signal on the USB cable is valid. 1'b1: The VBUSVLDEXT input is used. 1'b0: The internal Session Valid comparator is used.
0	RW	0x0	usbhost0_vbusvldext USB HOST0 external VBUS valid indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL signal is set to 1. VBUSVLDEXT indicates whether the VBUS signal on the USB cable is valid. In addition, BUSVLDEXT enables the pullup resistor on the D+ line. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.

GRF_UOC1_CON3
Address: Operational Base + offset (0x0340)
UOC1 control register 3

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
14	RW	0x0	usbhost0_ohci_cntsel USB HOST0 ohci_cntsel bit control
13	RW	0x0	usbhost0_utmiotg_idpullup USB HOST0 idpullup bit control
12	RW	0x1	usbhost0_utmiotg_dppulldown USB HOST0 dppulldown bit control
11	RW	0x1	usbhost0_utmiotg_dmpulldown USB HOST0 dmpulldown bit control
10	RW	0x1	usbhost0_utmiotg_drvvbus USB HOST0 drvvbus bit contrl
9:7	RO	0x0	reserved
6	RW	0x1	usbhost0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit conrol
5	RW	0x0	usbhost0_utmi_termselect USB HOST0 utmi termination select 1'b1: full speed terminations are enabled 1'b0: high speed terminations are enabled
4:3	RW	0x0	usbhost0_utmi_xcvrselect USB HOST0 utmi transceiver select 2'b11: sends an LS packet on an FS bus or receives an LS packet 2'b10: LS transceiver 2'b01: FS transceiver 2'b00: HS transceiver

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	usbhost0_utmi_opmode USB HOST0 utmi operation mode This controller bus selects the UTMI+ operation mode 2'b11: normal operation without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encoding 2'b01: no-driving 2'b00: normal
0	RW	0x1	usbhost0_utmi_suspend_n USB HOST0 suspend mode enable 1'b1: normal operation mode 1'b0: suspend mode

GRF_UOC1_CON4
Address: Operational Base + offset (0x0344)
UOC1 control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	usbhost0_incr4_en USB HOST0 incr4_en bit control
14	RW	0x1	usbhost0_incr16_en USB HOST0 incr16_en bit control
13	RW	0x0	usbhost0_hubsetup_min USB HOST0 hubsetup_min bit control
12	RW	0x0	usbhost0_app_start_clk USB HOST0 app_start_clk bit control
11:6	RW	0x20	usbhost0_fladj_val_common USB HOST0 fladj_val_common bit control
5:0	RW	0x20	usbhost0_fladj USB HOST0 fladj bit control

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GRF_UOC2_CON0
Address: Operational Base + offset (0x0348)
UOC2 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost1_linestate_irq_pd USB HOST1 linestate interrupt pending bit
14	RW	0x0	usbhost1_linestate_irq_en USB HOST1 line state interrupt enable
13	RW	0x0	usbhost1_siddq USB HOST1 IDDQ test enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.
12	RW	0x0	usbhost1_port_reset USB HOST1 per-port reset When asserted, this customer-specific signal resets the corresponding port transmit and receive logic without disabling the clocks within the PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK cycles.
11:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x4	usbhost1_tune USB HOST1 VBUS valid threshold adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +9% 3'b110: +6% 3'b101: +3% 3'b100: Design default 3'b011: -3% 3'b010: -6% 3'b001: -9% 3'b000: -12%
4	RW	0x0	usbhost1_disable USB HOST1 block disable 1'b1: the USB HOST1 block is power down 1'b0: the USB HOST1 block is power up
3:1	RW	0x4	usbhost1_compdistune USB HOST1 disconnect threshold adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +4.5% 3'b110: +3% 3'b101: +1.5% 3'b100: Design default 3'b011: -1.5% 3'b010: -3% 3'b001: -4.5% 3'b000: -6%
0	RW	0x1	usbhost1_common_on_n USB HOST1 common block power-down control This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend or Sleep mode. 1'b1: In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered.

GRF_UOC2_CON1
Address: Operational Base + offset (0x034c)

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UOC2 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	usbhost1_txrisetune USB HOST1 HS transmitter rise/fall time adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -20% 2'b10: -15% 2'b01: design default 2'b00: +10%
13:12	RW	0x3	usbhost1_txhsxvtune USB HOST1 transmitter high-speed crossover adjustment This bus adjusts the voltage at which the DP and DM signals cross while transmitting in HS mode. 2'b11: Default setting 2'b10: +15 mV 2'b01: -15 mV 2'b00: Reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x3	usbhost1_txvreftune USB HOST1 HS DC voltage level adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +8.75% 4'b1110: +7.5% 4'b1101: +6.25% 4'b1100: +5% 4'b1011: +3.75% 4'b1010: +2.5% 4'b1001: +1.25% 4'b1000: Design default 4'b0111: -1.25% 4'b0110: -2.5% 4'b0101: -3.75% 4'b0100: -5% 4'b0011: -6.25% 4'b0010: -7.5% 4'b0001: -8.75% 4'b0000: -10%
7:4	RW	0x3	usbhost1_txfslstune USB HOST1 FS/LS source impedance adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -5% 4'b0111: -2.5% 4'b0011: Design default 4'b0001: +2.5% 4'b0000: +5%
3	RW	0x0	usbhost1_txpreemppulsetune USB HOST1 HS transmitter pre-emphasis duration control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. transition in HS mode. 1'b1: 1X, short pre-emphasis current duration 1'b0: (desian default) 2X, long pre-emphasis currrent duration

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Bit	Attr	Reset Value	Description
2:0	RW	0x3	usbhost1_sqrxtune USB HOST1 squelch threshold adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -20% 3'b110: -15% 3'b101: -10% 3'b100: -5% 3'b011: Design default 3'b010: +5% 3'b001: +10% 3'b000: +15%

GRF_UOC2_CON2
Address: Operational Base + offset (0x0350)
UOC2 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost1_acaenb USB HOST1 ACA ID_OTG pin resistance detection enable 1'b1: enable detection on resistance on the ID_OTG pin of an ACA 1'b0: disable detection on resistance on the ID_OTG pin of an ACA

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Bit	Attr	Reset Value	Description
14	RW	0x0	usbhost1_dcdenb USB HOST1 data contact detection enable 1'b1: IDP_SRC current is sourced onto DP, pull-down resistance on DMA is enabled 1'b0: IDP_SRC current is disable, pull-down resistance on DM is disabled
13	RO	0x0	reserved
12:11	RW	0x1	usbhost1_txrestune USB HOST1 source impedance adjustment 2'b11: source impedance is desreased by 4ohm 2'b10: source impedance is desreased by 2ohm 2'b01: design default 2'b00: source impedance is desreased by 1.5ohm
10	RW	0x1	usbhost1_sleepm USB HOST1 sleep mode enable Asserting this signal place the USB PHY in sleep mode. 1'b0: sleep mode enable 1'b1: normal mode
9	RO	0x0	reserved
8	RW	0x1	usbhost1_retenable_n USB HOST1 retention mode enable 0: retention mode enable 1: retention mode disable
7	RW	0x0	usbhost1_vdatsrcenb USB HOST1 battery charging sourcing select 1'b1: data source voltage is enable 1'b0: data source voltage is disable
6	RW	0x0	usbhost1_vdatdetenb USB HOST1 battery charging attach/connect detection enable 1'b1: enable 1'b0: disable
5	RW	0x0	usbhost1_chrgsel USB HOST1 battery charging source select 1'b1: data source voltage is sourced onto DM and sunk from DP 1'b0: data source voltage is sourced onto DP and sunk from DM

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Bit	Attr	Reset Value	Description
4:3	RW	0x1	usbhost1_txpreempamptune 2'b11: 3X pre-emphasis current 2'b10: 2X pre-emphasis current 2'b01: 1X pre-emphasis current 2'b00: HS Transmitter Pre-Emphasis is disabled
2	RW	0x0	usbhost1_soft_con_sel 1'b0: software control usb host1 disable 1'b1: software control usb host1 enable
1	RW	0x0	usbhost1_vbusvldextsel USB HOST1 external VBUS valid select This signal selects the VBUSVLDEXT input or the internal Session Valid comparator to indicate when the VBUS signal on the USB cable is valid. 1'b1: The VBUSVLDEXT input is used. 1'b0: The internal Session Valid comparator is used.
0	RW	0x0	usbhost1_vbusvldext USB HOST1 external VBUS valid indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL signal is set to 1. VBUSVLDEXT indicates whether the VBUS signal on the USB cable is valid. In addition, BUSVLDEXT enables the pullup resistor on the D+ line. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.

GRF_UOC2_CON3
Address: Operational Base + offset (0x0354)
UOC2 control register 3

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	usbhost1_scaledown_mode USB HOST1 scale down mode control
13	RW	0x0	usbhost1_utmiotg_idpullup USB HOST1 idpullup bit control
12	RW	0x1	usbhost1_utmiotg_dppulldown USB HOST1 dppulldown bit control
11	RW	0x1	usbhost1_utmiotg_dmpulldown USB HOST1 dmpulldown bit control
10	RW	0x1	usbhost1_utmiotg_drvvbus USB HOST1 drvvbus bit contrl
9:6	RO	0x0	reserved
5	RW	0x0	usbhost1_utmi_termselect USB HOST1 utmi termination select 1'b1: full speed terminations are enabled 1'b0: high speed terminations are enabled
4:3	RW	0x0	usbhost1_utmi_xcvrselect USB HOST1 utmi transceiver select 2'b11: sends an LS packet on an FS bus or receives an LS packet 2'b10: LS transceiver 2'b01: FS transceiver 2'b00: HS transceiver

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	usbhost1_utmi_opmode USB HOST1 utmi operation mode This controller bus selects the UTMI+ operation mode 2'b11: normal operation without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encoding 2'b01: no-driving 2'b00: normal
0	RW	0x1	usbhost1_utmi_suspend_n USB HOST1 suspend mode enable 1'b1: normal operation mode 1'b0: suspend mode

GRF_UOC3_CON0
Address: Operational Base + offset (0x0358)
UOC3 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14:0	RW	0x0	reserved

GRF_UOC3_CON1
Address: Operational Base + offset (0x035c)
UOC3 control register 1

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RO	0x0	reserved

GRF_UOC4_CON0
Address: Operational Base + offset (0x0360)
UOC4 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	drvvbus_out_sel0 USB PHY drv vbus output select 0 2'b00: USB OTG drv vbus 2'b01: USB HOST0 drv vbus 2'b1x: USB HOST1 drv vbus

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	drvvbus_out_sel1 USB PHY drv vbus output select 1 2'b00: USB OTG drv vbus 2'b01: USB HOST0 drv vbus 2'b1x: USB HOST1 drv vbus
11: 0	RO	0x0	reserved

GRF_UOC4_CON1
Address: Operational Base + offset (0x0364)
UOC4 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RO	0x0	reserved

GRF_PVTM_CON0
Address: Operational Base + offset (0x0368)
PVT monitor control register 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x0	pvtm_gpu_osc_en pd_gpu PVT monitor oscilator enable 1'b1: enable 1'b0: disable
8	RW	0x0	pvtm_gpu_start pd_gpu PVT monitor start control
7:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_osc_en pd_core PVT monitor oscilator enable 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_start pd_core PVT monitor start control

GRF_PVTM_CON1
Address: Operational Base + offset (0x036c)
PVT monitor control register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_core_cal_cnt pd_core pvtm calculator counter

GRF_PVTM_CON2
Address: Operational Base + offset (0x0370)
PVT monitor control register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_gpu_cal_cnt pd_gpu pvtm calculator counter

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GRF_PVTM_STATUS0
Address: Operational Base + offset (0x0374)
PVT monitor status register 0

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_freq_done pd_core pvtm frequency calculate done stutus
0	RW	0x0	pvtm_gpu_freq_done pd_gpu pvtm frequency calculate done stutus

GRF_PVTM_STATUS1
Address: Operational Base + offset (0x0378)
PVT monitor status register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_freq_cnt pd_core pvtm frequency count

GRF_PVTM_STATUS2
Address: Operational Base + offset (0x037c)
PVT monitor status register 2

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pvtm_gpu_freq_cnt pd_gpu pvtm frequency count

GRF_IO_VSEL
Address: Operational Base + offset (0x0380)
IO voltage select

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	gpio1830_v18sel GPIO1830 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
8	RW	0x0	gpio30_v18sel GPIO30 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
7	RW	0x0	sdcard_v18sel SDCARD IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
6	RW	0x0	audio_v18sel AUDIO IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
5	RW	0x0	bb_v18sel BB IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
4	RW	0x0	wifi_v18sel WIFI IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
3	RW	0x0	flash1_v18sel FLASH1 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
2	RW	0x1	flash0_v18sel FLASH0 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
1	RW	0x0	dvp_v18sel DVP IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
0	RW	0x0	lcdc_v18sel LCDC IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V

GRF_SARADC_TESTBIT
Address: Operational Base + offset (0x0384)
SARADC Test bit register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	saradc_testbit SARADC test bit

GRF_TSADC_TESTBIT_L
Address: Operational Base + offset (0x0388)
TSADC Test bit low register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	tsadc_testbit_l Low 16bits of TSADC test bit

GRF_TSADC_TESTBIT_H
Address: Operational Base + offset (0x038c)
TSADC Test bit high register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	tsadc_testbit_h High 16bits of TSADC test bit

GRF_OS_REG0
Address: Operational Base + offset (0x0390)
OS register 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg0 OS register 0

GRF_OS_REG1
Address: Operational Base + offset (0x0394)
OS register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg1 OS register 1

GRF_OS_REG2
Address: Operational Base + offset (0x0398)
OS register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg2 OS register 2

GRF_OS_REG3
Address: Operational Base + offset (0x039c)
OS register 3

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg3 OS register 3

GRF_SOC_CON15
Address: Operational Base + offset (0x03a4)
SoC control register 15

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_dclk1_lvds_inv_sel Invertion of VOP_LIT dclk for LVDS selection 1'b1: invert 1'b0: not invert
14	RW	0x0	grf_dclk1_lvds_div2_sel 2 divide frequency of VOP_LIT dclk for LVDS selection 1'b1: 2 divide frequency 1'b0: no divide frequency
13	RW	0x0	grf_dclk0_lvds_inv_sel Invertion of VOP_BIG dclk for LVDS selection 1'b1: invert 1'b0: not invert
12	RW	0x0	grf_dclk0_lvds_div2_sel 2 divide frequency of VOP_BIG dclk for LVDS selection 1'b1: 2 divide frequency 1'b0: no divide frequency
11	RO	0x0	reserved
10:8	RW	0x0	dphy_tx0_turnrequest MIPI DPHY TX0 turn around request Every bit for one lane, bit2 is for lane3, bit2 is for lane2, bit0 is for lane1.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	dphy_tx1rx1_turnrequest MIPI DPHY TX1RX1 turn around request Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
3:0	RW	0x0	dphy_rx0_turnrequest MIPI DPHY RX0 turn around request Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON16
Address: Operational Base + offset (0x03a8)
SoC control register 16

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RO	0x0	reserved
1	RW	0x0	grf_con_dsi1_dpiupdatecfg DSI host1 dpiupdatecfg bit control
0	RW	0x0	grf_con_dsi0_dpiupdatecfg DSI host0 dpiupdatecfg bit control

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Chapter 5 Core System

5.1 Overview

The Core system of the device is based on the symmetric multiprocessor (SMP) architecture, contain quad Cortex-A17.The Cortex-A17 implements 32KB L1 instruction cache, 32KB L1 data cache, 1MB L2 cache.It delivers higher performance and optimal power management, debug and emulation capabilities.

The core system also contain a bus interconnect, which connect the A17's peripheral port and the generic interrupt controller (GIC400).

The core system contain the ARM's coresight cell , which helps to do debug and trace .

The interrupt controller is also included in this system, for detail description , please reference to chapter 12.

The Core system supports following features:

ARM Coretex-A17 based quad MPU subsystem with SMP architecture
Cortex-A17 core revision r0p1
Full implements the ARMv7-A architecture profile that includes SIMDv2 and VFPv4-D32 extensions
32KB L1 I-cache and 32KB L1 D-cache with 64-byte line size and 4-way set associative per CPU
A 32-entry,fully associative, instruction micro TLB.
A 32-entry,fully associative, data micro TLB.
A 1024-entry, 4-way, unified main TLB with hit-under-miss capabilities.
Memory management unit (MMU)
Automatic cache coherency between L1 data caches within the cluster.
Interrupt controller with 128 hardware interrupt inputs.
1MB L2 cache with 64-byte line size, and 16-way set associative.
standard CoreSight™ components to support SMP debug and emulation
Program trace macrocell (PTM)
Emulation logic (cross-triggers)
TPIU for trace.

5.2 Block Diagram

The Core system comprises with:

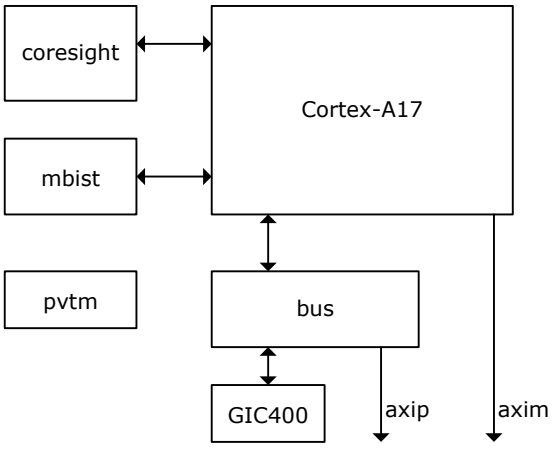

Fig. 5-1 Block Diagram

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Chapter 6 Interconnect

6.1 Overview

The chip-level interconnect consists of main interconnect and peri interconnects. It enables communication among the modules and subsystems in the device.

The main interconnect supports the following features:

Cross-bar exchange network
A special internal slave for accessing the configuration register
Little-endian platform
Embedded memory scheduler for ddr transaction generation
QoS management for optimizing the transaction flow
Transaction statistics for analyzing the transaction flow
Security protection mechanism to compatible with the TrustZone technology
The peri interconnect belong to peripheral system which is responsible for peripheral devices control such as usb device, flash device, uart, spi etc.

6.2 Block Diagram

The interconnect comprises with:

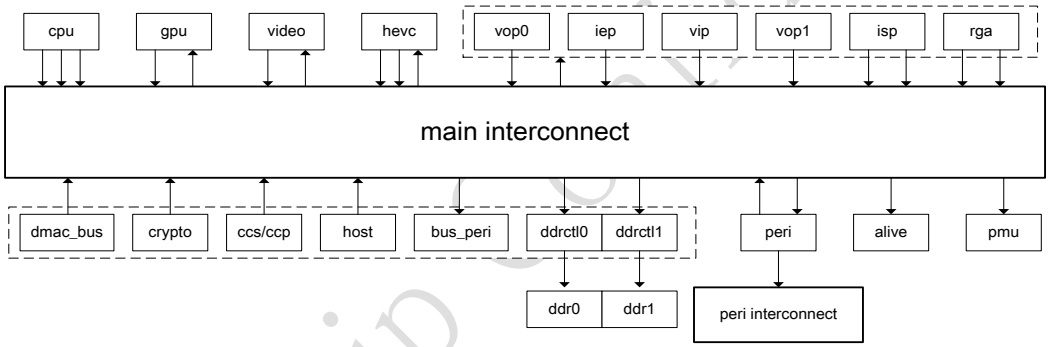

Fig. 6-1 Block Diagram

6.3 Function Description(main interconnect)

6.3.1 Master & Slave

The main interconnect is connected with all the related IPs of the system, the interface between the IP and the interconnect is called as NIU(native interface unit). All the connected NIU are list as bellowing:

Table 6-1 Master NIU

Master NIU	Description
cpup	Cortex-A17 AXI P port, access to any peripheral device
cpum	Cortex-A17 AXI M port , access to main memory
dbg	Jtag Debug master , access to any peripheral
bus_dmac	DMAC in pd_bus power domain
crypto	Crypto , used in trustzone technolgy

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ccs	CCS, used in trustzone technolgy
ccp	CCP, used in trustzone technolgy
gpu	Mali-T760 of pd_gpu power domain
hevc	HEVC of pd_hevc power domain
video	Video codec of pd_video power domain
vop_big	Lcdc full function of pd_vio power domain
iep	IEP of pd_vio power domain
vip	VIP of pd_vio power domain
vop_lit	Lcdc lite of pd_vio power domain
isp	ISP of pd_vio power domain
rga	RGA of pd_vio power domain
peri	Peri-bus of pd_peri power domain

Table 6-2 slave NIU

Slave NIU	**Description**
msch0	Memory scheduler channel-0 in pd_bus power domain
msch1	Memory scheduler channel-1 in pd_bus power domain
bus_ahb	Ahb slave in pd_bus power domain
imem	Internal memory in pd_bus power domain
bus_apb	Apb slave in pd_bus power domain
pmu_apb	Pmu apb slave in pd_pmu power domain
alive_apb	Alive apb slave in pd_alive power domain
vio_ahb	Vio ahb slave in pd_vio power domain
gevc_ahb	Hevc ahb slave in pd_hevc power domain
video_ahb	Video ahb slave in pd_video power domain
gpu_axi	Gpu axi slave in pd_gpu power domain
service_bus	Service module inside the interconnect in pd_bus power domain, used as register configuration
service_core	Service module in pd_core power domain
service_dmac	Service module in pd_bus power domain
service_gpu	Service module in pd_gpu power domain
service_hevc	Service module in pd_hevc power domain

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service_peri	Service module in pd_peri power domain
service_vio	Service module in pd_vio power domain
service_video	Service module in pd_video power domain

6.3.2 Clock & Power domain

The interconnect is divided to several clock domain and power domain. Each domain contain different IPs.
The clock/power domain and IP combination is list as bellowing:

Table 6-3 Clock and Power domain

Clock domain	Clock	Power domain	IP
alive_clk_dm	alive_pclk	alive_pwr	CRU/PLL/GRF/GPIO/TIMER/WDT
bus_clk_dm	bus_aclk	bus_pwr	IMEM
	bus_hclk		I2S/SPDIF/CRYPTO
	bus_pclk		TIMER/PWM/I2C/UART/DMAC/PCTL
core_clk_dm	cpum_aclk/ cpup_aclk	core_pwr	Cortex-A17
gpu_clk_dm	gpu_aclk	gpu_pwr	Mali-T760
hevc_aclk_dm	hevc_aclk	hevc_pwr	HEVC
hevc_hclk_dm	hevc_hclk		
msch0_clk_dm	msch0_clk	bus_pwr	Memory scheduler 0
msch1_clk_dm	msch1_clk		Memory scheduler 1
peri_clk_dm	peri_aclk	peri_pwr	Peri-BUS
pmu_clk_dm	pmu_pclk	pmu_pwr	PMU/PMU_IMEM/SGRF/GPIO
video_aclk_dm	video_aclk	video_pwr	VCODEC
video_hclk_dm	video_hclk		
vio0_clk_dm	vio0_aclk	vio_pwr	VOP_BIG/IEP/VIP
vio01_clk_dm	vio1_aclk		ISP/VOP_LIT
vio2_clk_dm	vio2_aclk		RGA
vio_hclk_dm	vio_hclk		

6.3.3 QoS management

The interconnect offers 4 modes of qos management:

- None: QoSGenerator is disabled, and priority information are stuck at 0.
- Fixed: QoSGenerator drives applies a fixed urgency to read transactions, and a (possibly different) urgency to write transactions.
- Limiter: QoSGenerator behaves as in fixed mode, but limits the traffic bandwidth coming from that socket, possibly stalling requests if the initiator attempts to exceed its budget.

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- Regulator: QoSGenerator promotes are demotes hurry, depending the bandwidth obtained by the initiator is below or beyond a bandwidth budget. As transactions exceeding the bandwidth limit are sent (even though demoted), the regulator mode may be considered as a softer version of the limiter mode.

Limiter Behavior

When configured in bandwidth limiter, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

• Adds the number of byte rounded up to 16 (1 -> 16) and then multiplied by 256 to the current value, each time a request is sent.
• Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
• If the Counter value is greater than the Saturation register value multiplied by 16*256, any incoming request is stalled until this condition disappears. Note that the Counter cannot wrap-around because the maximum value it can reach is: SaturationMax*16*256 + BurstMax*256 = 1023*4K+4K*256 = 5116K or 223 = 8192K.

The following example will show the Counter behavior: 32 byte bursts, F=400MHz, BW=200MB/s, T=0.32us. The Bandwidth register will be set to 256*200/400 = 128, and the Saturation register to 128*0.32*400/4096 = 4 (which corresponds to 64 bytes).

Regulator Behavior

When configured in bandwidth regulator, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

• Adds the number of byte rounded up to 16 and then multiplied by 256 to the current value, each time a response is received. If the result is greater than the Saturation register value multiplied by 16*256, saturation to this value is applied.
• Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
• If the Counter value is less than or equal to the Saturation register value multiplied by 16*256/2, the SocketMst Hurry signal will be set to the HurryHigh register, and HurryLow otherwise. Note that Urgency and Press will be also set to the same value.

The following example will show the Counter behavior: 1Kbyte bursts, F=500MHz, BW=2GB/s,T=2.048us. The Bandwidth register will be set to 256*2000/500 = 1024, and the Saturation register to 1024*2.048*500/4096 = 256 (which corresponds to 4 Kbytes).

QoS Generator Programming

Bandwidth: This log2(socket.wData/8)+8 bits registerdefines the bandwidth in 1/256th byte per cycle unit. Thisallows a 2 MByte/s resolution at 500MHz. When thebandwidth is given in MByte/s, the value of this register will
be equal to 256*BWMB/s / FMHz.

Saturation: This 10 bits register defines the number of byteused for bandwidth measurement. It is expressed in 16bytes unit (up to 16 Kbyte). Usually the integration windowis given in us or in cycle: the value of this register will beequal to Bandwidh*Tus*FMHz/(256*16)or Bandwidh*Ncycle/(256*16).

6.3.4 Memory Scheduler

Memory scheduler is a special NIU of the interconnect, it mainly deal with the transaction inside the interconnect and convert it to the transaction which the ddr protocol controller can

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recognize.
There are two memory schedulers in the interconnect, each is in different clock domain. These two memory schedulers are totally equal in function .
Following table shows the software configurable setting for the memory scheduler when the system connected to different size of ddr device.
The DDRCONF[3:0] is a configurable register inside the interconnect.
R: indicates Row bits
B: indicates Bank bits
C: indicates Column bits
D: indicates Chip selects bits

Table 6-4 DDR configuration

DDR CONF[3:0]	
0	R DBBB RRRR RRRR RRRR RRRC CCCC CCCC C---
1	C RRRD RRRR RRRR RRRR RBBB CCCC CCCC C---
2	C RRDR RRRR RRRR RRRR RBBB CCCC CCCC C---
3	C RDRR RRRR RRRR RRRR RBBB CCCC CCCC C---
4	C DRRR RRRR RRRR RRRR RBBB CCCC CCCC C---
5	R RRDR RRRR RRRR RRRR BBBC CCCC CCCC C---
6	R RDRR RRRR RRRR RRRR BBBC CCCC CCCC C---
7	R DRRR RRRR RRRR RRRR BBBC CCCC CCCC C---
8	C CRRR DRRR RRRR RRRR RRBB BCCC CCCC C---
9	C CRRD RRRR RRRR RRRR RRBB BCCC CCCC C---
10	C CRDR RRRR RRRR RRRR RRBB BCCC CCCC C---
11	C CBRR DRRR RRRR RRRR RRRB BCCC CCCC C---
12	C RBRR DRRR RRRR RRRR RRBB CCCC CCCC C---
13	B RRRR DRRR RRRR RRRR RBBC CCCC CCCC C---
14	C DRBB BRRR RRRR RRRR RRRR CCCC CCCC C---
15	D RRRR RRRR RRRR RRRR BBBC CCCC CCCC C---

When access to the two memory schedulers, the interconnect supports different stride between the two memory schedulers. Because of this function, the transaction can be interleaved send to the two channel ddr devices.
The stride can be 0Bytes,128Bytes,256Bytes,512Bytes,4kBytes.
It support the following configuration:

Table 6-5 DDR Stride

DDR STRIDE[4:0]	Channel 0 Address range	Channel 1 Address range	Stride size	Total size
5'b0_0000	0x0--0x0fff_ffff	0x1000_0000--0x1fff_ffff	256MB	512MB
5'b0_0001	0x0--0x1fff_ffff	0x2000_0000--0x3fff_ffff	512MB	1GB
5'b0_0010	0x0--0x3fff_ffff	0x4000_0000--0x7fff_ffff	1GB	2GB
5'b0_0011	0x0--0x7fff_ffff	0x8000_0000--0xffff_ffff	2GB	4GB
5'b0_0100	0x0--0x3fff_ffff	0x0--0x3fff_ffff	128B	1GB
5'b0_0101	0x0--0x3fff_ffff	0x0--0x3fff_ffff	256B	1GB
5'b0_0110	0x0--0x3fff_ffff	0x0--0x3fff_ffff	512B	1GB
5'b0_0111	0x0--0x3fff_ffff	0x0--0x3fff_ffff	4KB	1GB

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DDR STRIDE[4:0]	Channel 0 Address range	Channel 1 Address range	Stride size	Total size
5'b0_1000	0x0--0x7fff_ffff	0x0--0x7fff_ffff	128B	2GB
5'b0_1001	0x0--0x7fff_ffff	0x0--0x7fff_ffff	256B	2GB
5'b0_1010	0x0--0x7fff_ffff	0x0--0x7fff_ffff	512B	2GB
5'b0_1011	0x0--0x7fff_ffff	0x0--0x7fff_ffff	4KB	2GB
5'b0_1100	0x0--0xffff_ffff	0x0--0xffff_ffff	128B	4GB
5'b0_1101	0x0--0xffff_ffff	0x0--0xffff_ffff	256B	4GB
5'b0_1110	0x0--0xffff_ffff	0x0--0xffff_ffff	512B	4GB
5'b0_1111	0x0--0xffff_ffff	0x0--0xffff_ffff	4KB	4GB
5'b1_0000	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	128B	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	128B	
5'b1_0001	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	256B	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	256B	
5'b1_0010	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	512B	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	512B	
5'b1_0011	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	4KB	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	4KB	
5'b1_0100	0x0-- 0x0fff_ffff	0x1000_0000-- 0x1fff_ffff	256MB	1GB
	0x2000_0000-- 0x3fff_ffff	0x2000_0000-- 0x3fff_ffff	128B	
5'b1_0101	0x0-- 0x1fff_ffff	0x2000_0000-- 0x3fff_ffff	512MB	2GB
	0x4000_0000-- 0x7fff_ffff	0x4000_0000-- 0x7fff_ffff	128B	
5'b1_0110	0x0--0xffff_ffff		4GB	4GB
5'b1_0111		0x0000_0000--0xffff_ffff	4GB	4GB
5'b1_1010	0x0-0xffff_ffff	0x1_0000_0000—0x1_ffff_ffff	4GB	8GB
5'b1_1011	0x0-0x1_ffff_ffff	0x0-0x1_ffff_ffff	128B	8GB

The following picture shows the address mapping from soc system to ddr device space, when configure the ddrstride=5'b01000 ,interleaved size as 128Bytes.

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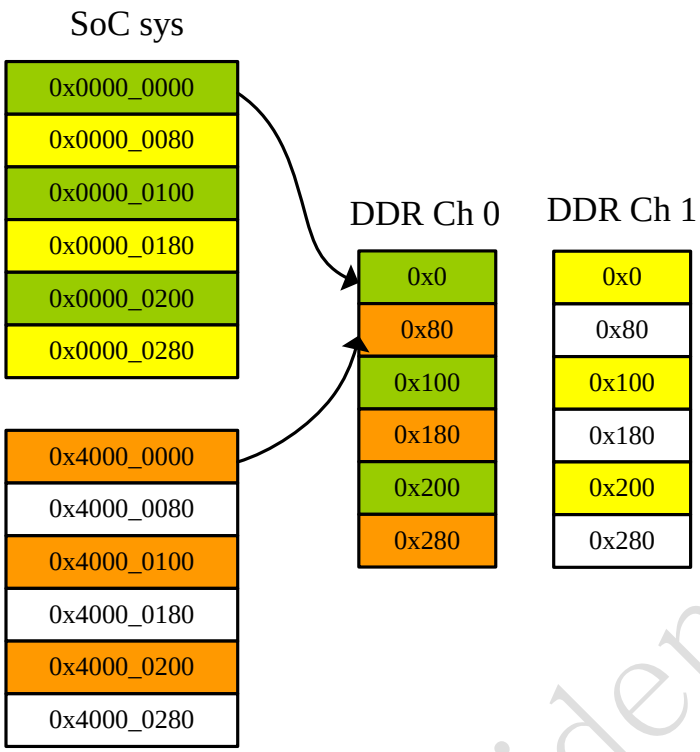

Fig. 6-2 DDR interleaved example

6.4 Register Description(main interconnect)

6.4.1 Internal Address Mapping

Table 6-6 Service module

Service Module	Base address
service_bus	0xffac_0000
service_core	0xffa8_0000
service_dmac	0xffa9_0000
service_gpu	0xffaa_0000
service_hevc	0xffaf_0000
service_peri	0xffab_0000
service_vio	0xffad_0000
service_video	0xffae_0000

Table 6-7 Service_bus block

Register block inside service_bus	Internal offset
msch0	0x0
msch0_cpum_probe	0x400
msch0_gpu_probe	0x800
msch0_obsrv	0x180
msch0_peri_probe	0xc00
msch0_video_probe	0x1000
msch0_vio0_probe	0x1400
msch0_vio1_probe	0x1800
msch0_vio2_probe	0x1c00
msch1	0x80
msch1_cpum_probe	0x2000
msch1_gpu_probe	0x2400
msch1_obsrv	0x200
msch1_peri_probe	0x2800
msch1_video_probe	0x2c00

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Register block inside service_bus	Internal offset
msch1_vio0_probe	0x3000
msch1_vio1_probe	0x3400
msch1_vio2_probe	0x3800

Table 6-8 Service_core block

Register block inside service_core	Internal offset
cpum_r_qos	0x80
cpum_w_qos	0x100
cpup_qos	0x0

Table 6-9 Service_dmac block

Register block inside service_dmac	Internal offset
bus_dmac_qos	0x0
ccp_qos	0x180
crypto_qos	0x100
ccs_qos	0x200
host_qos	0x80

Table 6-10 Service_gpu block

Register block inside service_gpu	Internal offset
gpu_r_qos	0x0
gpu_w_qos	0x80

Table 6-11 Service_hevc block

Register block inside service_hevc	Internal offset
hevc_r_qos	0x0
hevc_w_qos	0x100

Table 6-12 Service_peri block

Register block inside service_peri	Internal offset
peri_qos	0x0

Table 6-13 Service_vio block

Register block inside service_vio	Internal offset
vio0_iep_qos	0x500
vio0_vip_qos	0x480
vio0_vop_qos	0x400
vio1_isp_r_qos	0x900
vio1_isp_w0_qos	0x100
vio1_isp_w1_qos	0x180
vio1_vop_qos	0x0
vio2_rga_r_qos	0x800
vio2_rga_w_qos	0x880

6.4.2 Registers Summary

service_bus: memory scheduler channel-0 register summary

Name	Offset	Size	Reset Value	Description
coreid	0x0000	W	0x21501602	core id of memory scheduler 0
revisionid	0x0004	W	0x0126f200	revisionid
ddrconf	0x0008	W	0x00000000	ddr configuration register
ddrtiming	0x000c	W	0x2475931c	ddr timing register
ddrmode	0x0010	W	0x00000000	ddr mode register

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Name	Offset	Size	Reset Value	Description
readlatency	0x0014	W	0x00000032	read latency register
activate	0x0038	W	0x00000400	activate register
devtodev	0x003c	W	0x00000000	devtodev register

service_core: cpup_qos register summary

Name	Offset	Size	Reset Value	Description
priority	0x0008	W	0x00000101	priority register
mode	0x000c	W	0x00000003	qos mode register
bandwidth	0x0010	W	0x00000005	qos bandwidth register
saturation	0x0014	W	0x00000040	qos saturation register
extcontrol	0x0018	W	0x00000000	qos extcontrol register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

service_bus:msch1's register is same with msch0

other master's qos register is same with service_core:cpup_qos

6.4.3 Detail Register Description

service_bus: memory scheduler channel-0 coreid
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x21501602	msch0' core id

service_bus: memory scheduler channel-0 revisionid
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x0126f200	msch0' revision id

service_bus: memory scheduler channel-0 ddrconf
Address: Operational Base + offset (0x0008)
Memory scheduler configuration register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	DdrConf select the ddr rank,row,bank,col sequence

service_bus: memory scheduler channel-0 ddrtiming
Address: Operational Base + offset (0x000c)
Memory scheduler timing register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31	RW	0x0	BwRatio Bandwidth determines , in conjunction with field BwRatioExtended of register ddrmode, the number of DRAM data bus cycles required to process a acheduler data bus word. When BwRatio and BwRatioExtended are set to 0, the bandwidth ratio is 1:1, that is one DRAM cycles per scheduler word. When BwRatio is set to 1, and BwRatioExtended is set to 0, the bandwidth ratio is 2:1, that is ,two DRAM cycles per scheduler word.
30:26	RW	0x00	WrToRd Minimum time between the last DRAM Write command and a Read command.
25:21	RW	0x00	RdToWr Minimum time between the last DRAM Read command and a Write command.
20:18	RW	0x0	BurstLen DRAM burst duration on the DRAM data bus. Also equal to minimum time between two DRAM commands.
17:12	RW	0x00	WrToMiss Minimum time between the last DRAM Write command and a new Read or Write command in another page of the same bank.
11:6	RW	0x00	RdToMiss Minimum time between the last DRAM Read command and a new Read or Write command in another page of the same bank.
5:0	RW	0x00	ActToAct Minimum time between two consecutive DRAM Activate commands on the same bank.

service_bus: memory scheduler channel-0 ddrmode
Address: Operational Base + offset (0x0010)
Memory scheduler mode register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	BwRatioExtended When 0, bandwidth ratio is determined by BwRatio. When 1, the bandwidth ratio is 4:1, that is four DRAM cycles per scheduler word, and BwRatio must be set to 0.

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Bit	Attr	Reset Value	Description
0	RW	0x0	AutoPrecharge When set to 1, pages are automatically closed after each access(no page hit). When set to 0, pages are left open until an access in a different page occurs.

service_bus: memory scheduler channel-0 readlatency
Address: Operational Base + offset (0x0014)
Memory scheduler read latency register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
7:0	RW	0x32	ReadLatency Stores a user-defined read response latency ceiling, expressed in scheduler clock cycles. When the scheduler determines that the latency of a read transaction to the controller exceeded this value, the scheduler stalls further transactions to reduce the number of commands in the memory controller queue.

service_bus: memory scheduler channel-0 activate
Address: Operational Base + offset (0x0038)
Memory scheduler activate register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x01	Fawbank Indicates the number of banks of a given device involved in the FAW period during which four banks can be activate.
9:4	RW	0x00	Faw The length of the FAW period, in cycles.
3:0	RW	0x00	Rrd The minimum number of scheduler clock cycles between two consecutive DRAM activate commands on different banks on the same device.

service_bus: memory scheduler channel-0 devtodev
Address: Operational Base + offset (0x003c)
Memory scheduler devtodev register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x00	Buswrtord The time delay, expressed in cycles, between a write and a read operation on different devices.

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Bit	Attr	Reset Value	Description
3:2	RW	0x00	Busrdtowr The time delay, expressed in cycles, between a read and a write operation on different devices.
1:0	RW	0x00	Busrdtord The time delay, expressed in cycles, between a read and a read operation on different devices.

Following is cpup port's QoS register detail description. Other ports have the same register. The only different is the base address's offset. The offset information is descripted in Table1-6 ~~ Table1-13.

service_core: cpup_qos Priority

Address: Operational Base + offset (0x0008)

CPU master0 priority register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x2	P1 sets the high hurry level (i.e. when the measured bandwidth does not exceed the setting) when in Regulator mode, or read urgency level when in fixed or limiter mode.
1:0	RW	0x0	P0 sets the low hurry level, that is, when the measured bandwidth exceeds the setting, when in regulator mode, or write urgency level when in fixed or limiter mode.

service_core: cpup_qos Mode

Address: Operational Base + offset (0x000c)

CPU master0 QoS mode register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x3	Mode determines which of the following modes the QoSGenerator will adopt at reset: 0 : None 1 : Fixed 2 : Limiter 3 : Regulator

service_core: cpup_qos Bandwidth

Address: Operational Base + offset (0x0010)

CPU master0 QoS bandwidth register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x007	Bandwidth Parameter bandwidth determines the bandwidth triggering of the limiter or the regulator. It is expressed in bytes per second. This parameter becomes available when limiter or regulator hardware is implemented.

service_core: cpup_qos Saturation
Address: Operational Base + offset (0x0014)
CPU master0 QoS saturation register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	Saturation Parameter saturation determines the excursion of the payload counter, used to estimate the bandwidth, expressed in bytes. This parameter becomes available when limiter or regulator hardware is implemented.

service_core: cpup_qos ExtControl
Address: Operational Base + offset (0x0014)
CPU master0 QoS saturation register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
2	RW	0x0	Replace the External reference by the local clock.
1	RW	0x0	ExtThr input controls Low/High priority instead of bandwidth threshold.
0	W	0x0	Combines the Socket QoS with Regulator QoS

6.5 Function Description(peri interconnect)

The peri interconnect contain the following master:
peri,gps,dmac,usb,nandc,mac,tsp,sdmmc.
A Global Programmers View (GPV) module exists to configure some properties of the interconnect. The arbitration scheme of this interconnect is configurable through GPV.
The priority from high to low is as follow:

peri/gps
dmac
usb
nandc/mac

Customers can configure the Qos value through the GPV to change this priority. If you config them to same priority, then the interconnect uses a Least Recently Used (LRU) algorithm

6.6 Register Description(peri interconnect)

6.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PERI_RQos_M0	0x42100	4bits	0x0003	peri AXI Port Read channel QoS value.

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Name	Offset	Size	Reset Value	Description
PERI_WQos_M0	0x42104	4bits	0x0003	peri AXI Port Write channel quality value.
PERI_RQos_M1	0x43100	4bits	0x0002	dmac Port Read channel QoS value.
PERI_WQos_M1	0x43104	4bits	0x0002	dmac Port Write channel quality value.
PERI_RQos_M2	0x44100	4bits	0x0001	nandc Port Read channel QoS value.
PERI_WQos_M2	0x44104	4bits	0x0001	nandc Port Write channel quality value.
PERI_RQos_M3	0x45100	4bits	0x0000	usb Port Read channel QoS value.
PERI_WQos_M3	0x45104	4bits	0x0000	usb Port Write channel quality value.
PERI_RQos_M4	0x46100	4bits	0x0000	gps Port Read channel QoS value.
PERI_WQos_M4	0x46104	4bits	0x0000	gps Port Write channel quality value.

*Notes: Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access*

6.6.2 Detail Register Description

PERI_RQos_M0
Address:Operational Base+0x42100
PERI_AXI Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x1	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M0
Address:Operational Base+0x42104
PERI_AXI Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x1	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M1
Address:Operational Base+0x43100
DMAC Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M1
Address:Operational Base+0x43104
DMAC Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M2
Address:Operational Base+0x44100
NANDC Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates

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			higher priority.

PERI_WQos_M2
Address:Operational Base+0x44104
NANDC Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M3
Address: Operational Base+0x45100
USB Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M3
Address: Operational Base+0x45104
USB Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M4
Address: Operational Base+0x46100
GPS Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M4
Address: Operational Base+0x46104
GPS Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

6.7 Application Notes

6.7.1 QoS setting

The cpum read channel, vop read channel , gpu write channel have the external QoS control. After reset each master port both have priority setting as 1. It's recommended that field 0 of qos.ExtControl set to 1 to enable the external qos control. And prioirty setting of each master kept at 1.

6.7.2 Idle request

The main interconnect supports flushing the ongoing transaction when the software needed to do so.
If the GPU power domain need to disconnect from the main interconnect, Idle request has to be sent to GPU NIU, the NIU will respond a ack, and when it's ready to be disconnect, one Idle signal will be send out . Then, if GPU still have transaction to be sent to the memory scheduler, it will be stalled by the NIU.
If the GPU system power domain is disconnected as the above flow, then CPU want to access to the GPU system, it will response error to CPU.
The sequence is like following figure shows:

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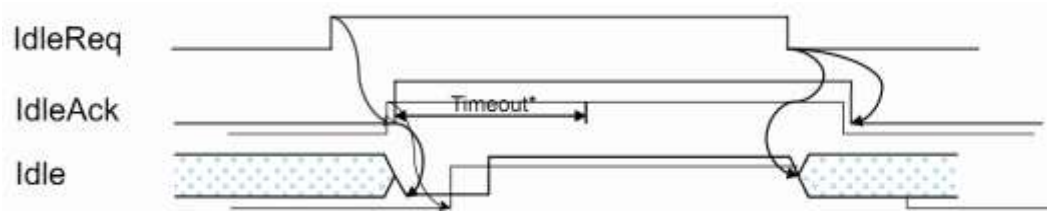

Fig. 6-3 Idle request

The idle request is set by PMU register.

6.7.3 DDR timing examples

The following picture provides examples of DDR timing values, in clock cycles for register values, and nanoseconds for parameter values.

DDR type	DDR2-3E		DDR2-25E		DDR3-187E		DDR3-125E	
DDR frequency	333 MHz		400 MHz		533 MHz		800 MHz	
Scheduler frequency	333 MHz		400 MHz		533 MHz		400 MHz	
Burst length	4		8		8		8	
Register field	cycles	ns	cycles	ns	cycles	ns	cycles	ns
ActToAct	18	54	22	55	27	50.6	19	47.5
RdToMiss	9	27	9	22.5	15	28.1	11	27.5
WrToMiss	16	48	20	50	29	54.3	20	50
BurstLen	2	6	4	10	4	7.5	2	5
RdToWr	2	6	2	5	3	5.6	2	5
WrToRd	2	6	7	17.5	10	18.7	7	17.5
Rrd	4	12	4	10	6	11.2	3	7.5
Faw	17	51	18	45	27	50.6	16	24
BusRdToRd	1	3	1	2.5	1	1.8	1	2.5
BusRdToWr	2	6	2	5	2	3.7	2	5
BusWrToRd	2	6	2	5	2	3.7	2	5

Fig. 6-4 DDR timing example

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Chapter 7 Dynamic Memory Interface (DMC)

7.1 Overview

The DMC includes two section: dynamic ram protocol controller(PCTL) and phy controller (PHYCTL).

The PCTL SoC application bus interface supports a lowest-latency native application interface (NIF). To maximize data transfer efficiency, NIF commands transfer data without flow control. To simplify command processing, the NIF accepts addresses in rank, bank, row, column format.

The PHYCTL provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, and programmable configuration controls. The PHYCTL has built-in self test features to provide support for production testing of the compatible PHY. It also provides a DFI 2.1 interface to the PHY.

The DMC supports the following features:

Complete, integrated, single-vendor DDR3, DDR3L, LPDDR2, LPDDR3 solution
DFI 2.1 interface compatibility
Up to 1066 Mbps in 1:1 frequency ratio, using a 533MHz controller clock and 533MHz memory clock
Dual channel, each channel up to 32 bits, totally support 64 bits data width
Support for x8, x16, and x32 memories
Each channel has separately controller and PHY
Up to 2 memory ranks for each channel; devices within a rank tie to a common chip select
Up to 8 open memory banks, maximum of eight per rank
Per-NIF transaction controllable bank management policies: open-page, close-page
Low area, low power architecture with minimal buffering on the data, avoiding duplication of storage resources within the system
PCTL NIF slave interface facilitates easy integration with an external scheduler or standard on-chip buses
Efficient DDR protocol implementation with in-order column (Read and Write) commands and out- of-order Activate and Precharge commands
Three clock cycles best case command latency (best case is when a command is to an open page and the shift array in the PCTL is empty).
1T or 2T memory command timing
Automatic clock stop, power-down and self-refresh entry and exit.
Clock stop is LPDDR2/LPDDR3 only
Software and hardware driven self-refresh entry and exit
Programmable memory initialization
Partial population of memories, where not all DDR byte lanes are populated with memory chips
Programmable per rank memory ODT(On-Die Termination) support for reads and writes
APB interface for controller software-accessible registers
Programmable data training interface
Assists in training of the data eye of the memory channel
Provides a method for testing large sections of memory
Support for industry standard UDIMMs (Unbuffered DIMMs) and RDIMMs (Registered DIMMs)
Automatic DQS gate training and drift compensation
At-speed built-in-self-test(BIST) loopback testing on both the address and data channels for DDR PHYs
PHY control and configuration registers
Support 2G memory wrap function

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7.2 Block Diagram

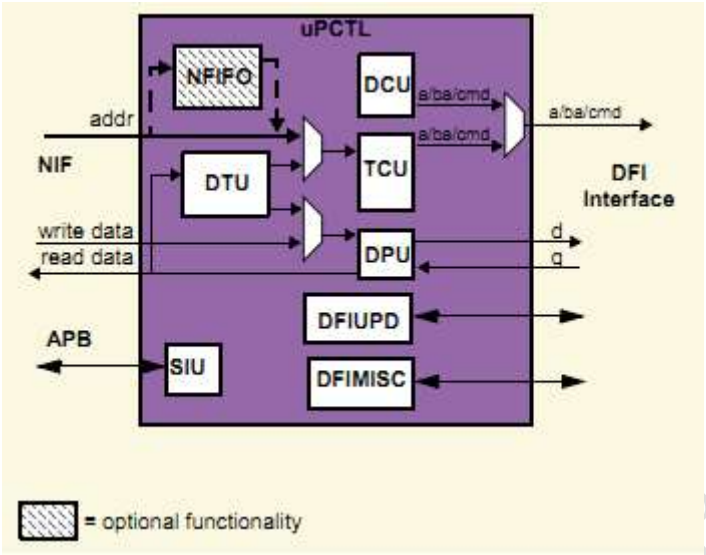

Fig. 7-1 Protocol controller architecture

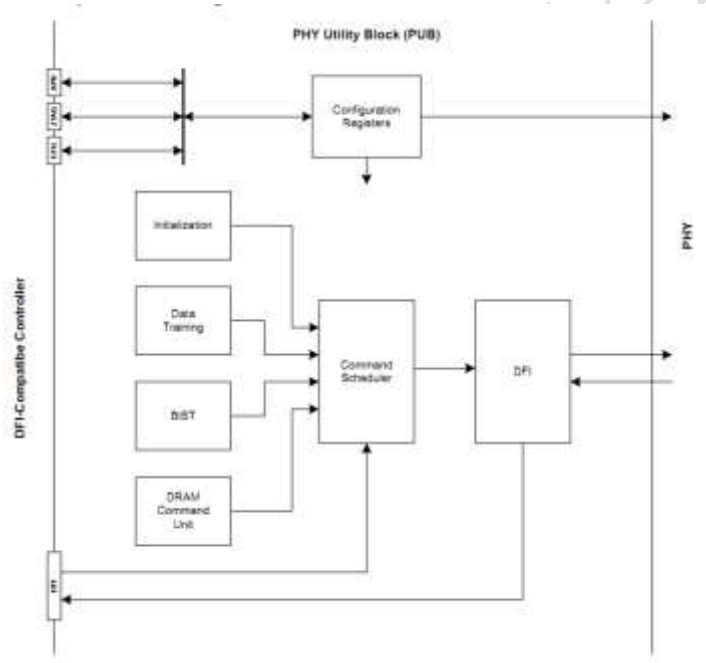

Fig. 7-2 PHY controller architecture

7.3 Function description

PCTL operations are defined in terms of the current state of the Operational State Machine. Software can move PCTL in any of the operational states by issuing commands via the SCTL register. Transitions from one operational state to the other occur pass through a "transitional" state. Transitional states are exited automatically by the PCTL after all the necessary actions required to change operational state have been completed. The current operational state of PCTL is reported by the STAT register and is also available from the p_ctl_stat output.

PCTL supports the following operational states:

Init_mem - This state is the default state entered after reset. All writable registers can be programmed. While in this state software can program PCTL and initialize the PHY and the memories. The memories are not refreshed and data that has previously been written to the memories may be lost as a result. The Init_mem state is also used when it is desirable to stop any automatic PCTL function that directly affects the memories, like Power Down and Refresh, or when software reset of the memory subsystem has to be executed.

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Config - This state is used to suspend temporarily the normal NIF traffic and allow software to reprogram PCTL and memories if necessary, while still keeping active the periodic generation of Refresh cycles to the memories. Power Down entry and exit sequences are possible while in Config state.

Access - This is the operational state where NIF transactions are accepted by the PCTL and converted into memory read and writes. None of the registers can be programmed except SCFG, SCTL, ECCCLR and DTU* registers.

Low_power - Memories are in self refresh mode. The PCTL does not generate refresh cycles while in this state.

Access and Low_power states can also be entered and exited by the hardware low power signals (c_*). In case of conflicting software and hardware low-power commands, the resulting operational state taken by the controller can be either one of the two conflicting requests. Figure 13-3 illustrates the operational and transitional states.

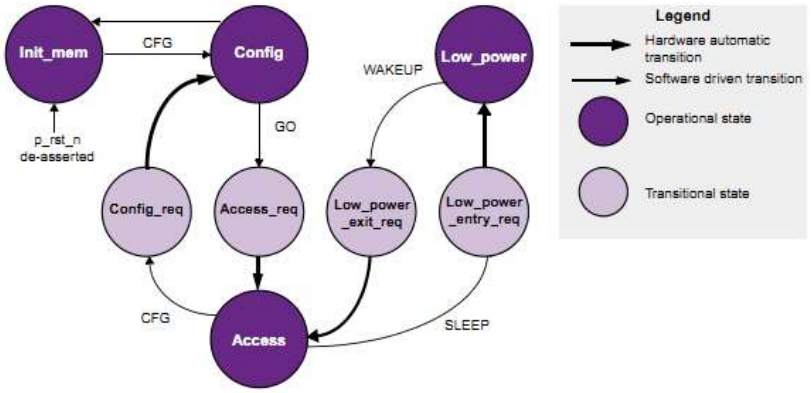

Fig. 7-3 Protocol controller architecture

The PHYCTL provides control features to ease the customer implementation of digitally controlled PHY features such as read DQS training, data eye training, output impedance calibration, and so on. The PHTCTL has built-in self test features to provide support for production testing of PHY. It also provides a DFI 2.1 interface to the PHY. The PHYCTL performs, in sequence, various tasks required by the PHY before it can commence normal DDR operations. SDRAM memory read/write access through the DDR PHY is primarily through a DFI 2.1 interface on the PHYCTL. Therefore, the memory controller used with the PHY must be DFI 2.1 compatible.

Access to the PHYCTL internal control features and registers is through a dedicated configuration port, which can be either APB or CFG (generic configuration interface). An optional JTAG interface can also be compiled in as an additional second configuration port to co-exist with either the APB or CFG main configuration ports. The PHYCTL is driven off two clocks, the controller clock (ctl_clk) and the configuration clock pclk for an APB interface. The controller clock is the same clock driving the memory controller and will be the same frequency as the SDRAM clock (ck). The configuration clock can run at a frequency equal to or less than the controller clock. The configuration clock drives all non-DDR timing logic, such as configuration registers, PHY initialization, output impedance, and so on.

7.4 DDR PHY

7.4.1 DDR PHY Overview

In order to facilitate robust system timing and ease of use, DMC interface and control architecture utilizes a mixture of soft-IP and hard-IP design elements. The main control logic (Memory Controller) is supplied as soft-IP. The PHY is comprised of hard-IP components that include double-data rate Interface Timing Modules(ITM), input and output path DLLs, and application-specific SSTL I/Os.

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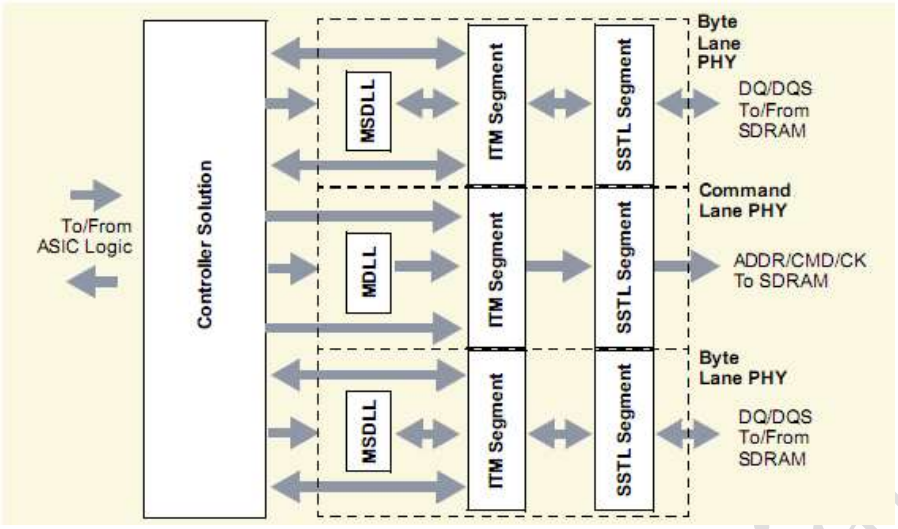

Fig. 7-4 DDR PHY architecture

In order to maximize system timing margins on the command/write path, inputs to the SDRAM are provided with the clock or data strobe centered in the associated data eye. The ITM components perform timing translation for the various signal groups of the interface. The hardened ITM approach ensures minimal pin to pin skew while allowing optimal circuit design for drive and capture circuitry. A DLL is utilized to facilitate the clock centering. In the Command Lane, a master DLL (MDLL) is utilized. In the Byte Lane, the master portion of a master/slave DLL macrocell (MSDLL) is utilized.

On the read path, read data from the SDRAM is arriving from the SDRAM edge aligned with the data strobes. In order to maintain maximum system timing margins on the input path, the data strobes are translated to the center of the data eye. The MSDLL macrocell associated with each Byte Lane contains a master DLL and 2 slave DLLs (mirror delay lines). The slave DLL portion of the MSDLL is utilized to facilitate the clock centering. DQS and DQS_b strobe inputs each utilize one of these slave DLL functions. The captured double data rate inputs are then converted to single data rate and passed onto the DDR Controller RTL logic. The ITM facilitates both data capture and DDR to SDR conversion.

The physical interface between the DDR controller and DDR SDRAMs uses DDR-specific SSTL I/O buffers with programmable on-die termination (ODT). These I/Os operate at either 1.8V for LPDDR/DDR2 interfacing (SSTL_18).

DMC interface and control architecture follows a common signal grouping philosophy. A Byte Lane is a complete eight-bit data unit consisting of the associated DQ, DM, and DQS/DQS_b signals. A 32-bit system would consist of four Byte Lanes. A Command Lane is a complete command and address unit including also clock signals. There would normally be only one Command Lane in a particular DDR SDRAM interface. All clock and data signals relative to a Lane, either Byte or Command, are isolated to within that Lane only. Timing critical clock and data signals do not traverse between Lanes. Implementation of a memory interface involves placing the Command Lane components, placing the Byte Lane components, and standard synthesis/place and route to complete the design.

Each SSTL cell communicating with the SDRAM has an associated ITM component. The ITM library consists of individual components designed specifically for signal groups of address and command, data & data mask, and data strobes. In order to ensure low pin to pin skews and facilitate ease of implementation, the ITM components are tileable. DLL output clock distribution is embedded within the ITM components.

7.4.2 Lane-Based Architecture

Byte Lane PHY

The data bus interface to the external memory is organized into self-contained units referred to herein as Byte Lanes. The external memory components are designed to support Byte Lanes for optimal system timing. The partitioning of the data word into discrete Byte Lanes allows pin to pin skew to be managed across a much smaller group of signals than would typically be required.

All components of the Byte Lane PHY are designed to permit connectivity by abutment. The ITM

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connects by abutment to the SSTL I/O, and the DLL connects by abutment to the ITM.
The SDRAM contains data strobes associated with each 8 bits of data and there is a timing skew allowance between the main clock signal to the SDRAM and its data strobe inputs during a Write command (tDQSS). 8bit memory components provide a single DQS.
A Byte Lane consists of the following I/O slots:

8 data bits (DQ)
data strobe bits (DQS / DQS_b)
1 data mask bit (DM)
I/O power and ground cells
Core power and ground cells

Each functional I/O slot has an associated ITM module, including DQ, DM, and DQS/DQS_b. The ITMs provide a mechanism for monitoring read timing drift, which can be used to adjust timing to maintain optimum system margins. Drift analysis and compensation is performed by the controller on a per Byte Lane basis. The ITM components contain the functions to monitor DQS drift and permit timing adjustment, the controller provides the analysis and control for these functions. These functions operate dynamically for each data bit of every user-issued Read command. There are no overhead penalties in channel bandwidth or utilization incurred by the use of these functions.
The memory interface (PHY) architecture is based on the concept of independent, but related, signal groups to provide the highest level of system timing performance. In order to maintain robust system timing, all clock and data signals relevant to a Byte Lane remain within that Byte Lane. These signals are not shared between other Byte Lanes or between a Byte Lane and a Command Lane. Alternate approaches require clock distribution networks that span the full length of the interface including all address, command, and data signals. These large clock distribution networks are difficult for the user to design and implement, and add an additional component of pin to pin skew to the critical timing budget.
A DLL macrocell (MSDLL) consisting of a master DLL and 2 slave DLLs (mirror delay lines) is utilized at each Byte Lane to facilitate optimal PHY timing for drive and capture of DDR data streams, and allows the Lanes to be independent. The master DLL section provides outputs for DDR data stream creation to the SDRAMs and acts as a reference for the slave delay line sections. The slave delay line sections translate the incoming DQS/DQS_b into the center of the read data eye to maximize read system timing margins.
The user is permitted to fine tune the relationship of the DQS and DQ signals to maximize read system timing margin. The DLL includes adjustability of the slave delay lines for the DQS and DQS_b signals, which provide byte-wide timing adjustments. The ITMs include adjustability of the read DQS/DQS_b strobe timing, which provides byte-wide timing adjustments. The ITMs include adjustability of the read DQ signal timing, which provides per-bit timing adjustability. To permit Lane-independent timing adjustments, DLL adjustment bits are provided by the controller per Byte Lane and ITM adjustment bits are provided per bit.
DMC interface and control solution allows memory systems with a word width narrower than the design. Our system is designed with a 32 bit data width and it can then be utilized with either 16 bit or 32 bit memory systems. The controller contains register settings to allow the desired operational mode to be set in the final device.
The DDR-specific SSTL I/Os include programmable ODT and output impendence selection. The ODT and output impedances can be be dynamically calibrated to compensate for variations in voltage and temperature. The ODT feature can be disabled by the controller. When ODT is enabled by the controller, the SSTL I/O automatically enables its internal ODT circuitry when in input mode and disable this circuitry when in output mode, as determined by the output enable signal. The initial programming and subsequent calibration of the of the ODT and output impedance is achieved through the use of an impedance control loop that can be triggered to calibrate the ODT and output impedance values at the I/Os based on the desired impedance value when compared to an precision external resistor. All the necessary pieces of the impedance control loop are included in the SSTL I/O library.
There are four Byte Lanes in our chip of 32 bit memory system.

Command Lane PHY

The control and address interface to the external memory is organized into a self-contained unit referred to herein as a Command Lane. DMC interface contains a single Command Lane

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and four Byte Lanes.
All components of the Command Lane PHY are designed to permit connectivity by abutment. The ITM connects by abutment to the SSTL I/O, and the DLL connects by abutment to the ITM. A typical Command Lane consists of the following I/O slots:

Memory clocks (CK/CK_b)
Command signals (RAS_b, CAS_b, WE_b)
1 or more clock enable (CKE)
1 or more on-die termination (ODT)
chip select (CS_b)
bank address (BA)
16 row/column address (A)
I/O power and ground cells
Core power and ground cells

The system clock input is used to provide the source clock for the memory interface. Memory controller supports 2 SDRAM ranks. There is one CKE, ODT, and CS_b signal provided for each rank.
Each functional I/O slot has an associated ITM module, with exception of the system clock input.
A master DLL (MDLL) is utilized with the Command Lane to facilitate optimal PHY timing for drive of DDR data streams, and allows the Lane to be independent. The DLL macrocells provide two 0 degree phase outputs, one which can be used to drive the controller logic. The Command Lane MDLL is used for this purpose.
To permit Lane-independent timing adjustments, DLL and ITM adjustment bits are provided by the controller separately for Command and Byte Lanes.

7.4.3 Master DLL(MDLL)

Master DLL for DDR2, and LPDDR applications is a Delay Locked Loop that takes an input reference clock (clk_in) and generates four clock outputs, each delayed in quarter clock cycle (90º) increments. These four clock phases (clk_0, clk_90, clk_180, clk_270) can be generated with very high accuracy and low jitter across a wide range of frequencies.

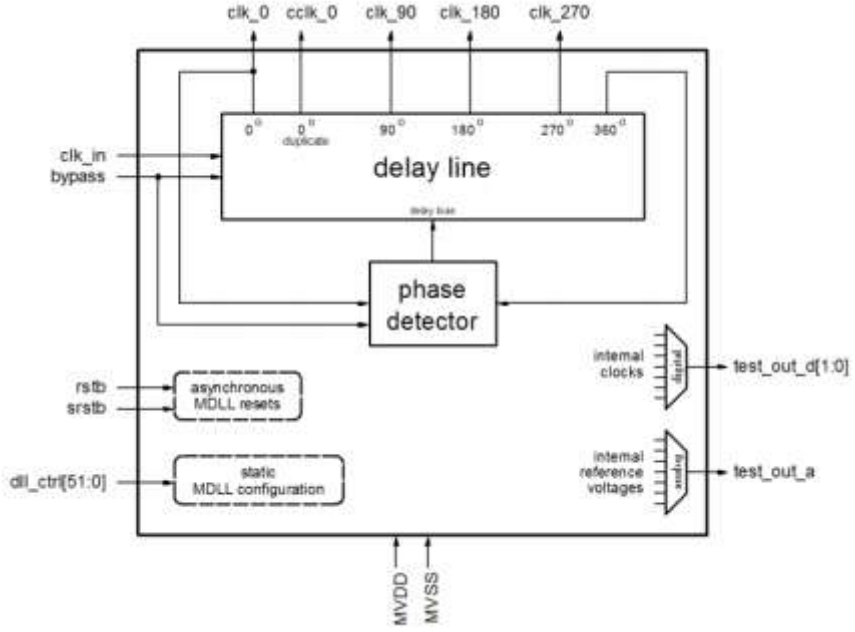

Fig. 7-5 DDR PHY master DLL architecture diagram

A number of test modes and configuration settings are included:

A bypass mode shuts down all analog circuitry, and directly buffers the input clock and strobes with appropriate delays and inversions to the output clocks and strobes. This mode can be used for low speed functional or IDDQ testing.
A digital test output (test_out_d) provides direct observability of several internal reference clock and timing nodes.
An analog test output (test_out_a) provides direct observability of several internal reference voltages.

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Master DLL Control for Trim and Test

The performance and testing of the MDLL can be accessed through the dll_ctrl bus.

Table 7-1 DDR PHYtrim and test MDLL control

Static Input		Field	Description
dll_ctrl	[1:0]		Reserved
	[4:2]	ipump_trm[2:0]	Charge pump current trim
	[5]	test_ctrl_en	Test control enable for analog and digital test outputs
	[8:6]	test_ctrl_d[2:0]	Digital test control. Selects the digital signal to be viewed at the digital test output
	[10:9]	test_ctrl_a[1:0]	Analog test control. Selects the analog signal to be viewed at the analog test output
	[11]		Reserved
	[14:12]	bias_trm[2:0]	Bias generator frequency trim
	[19,15]	fdtrm[1:0]	Bypass mode fixed delay trim
	[22:20]	bias_trm[6:4]	Bias generator control voltage trim
	[23]	bps200	Bypass frequency select
	[28:24]		Reserved
	[29]		Reserved
	[37:30]		Reserved
	[43:38]	fb_trm[5:0]	Feedback delay adjust
	[49:44]		Reserved
	[50]	test_hizb_a	Analog test output tri-stated control
	[51]		Reserved

Charge Pump Current Trim:

Table 7-2 charge pump current trim in dll_ctrl

Field	Setting	Function	Suggested Default
ipump_trm[2:0]	000	Maximum current	000
	111	Minimum current	

Digital Test Control:

Table 7-3 DLL digital test control in dll_ctrl

test_ctrl_en	test_ctrl_d[2:0]	Function	Suggested Default
0	xxx	digital test outputs disabled (drive '0')	0,000
1	000	0° output clock (clk_0)	
1	001	90° output clock (clk_90)	
1	010	180° output clock (clk_180)	
1	011	270° output clock (clk_270)	
1	100	360° internal clock (clk_360_int)	
1	101	Speed-up pulse (spdup)	
1	110	Slow-down pulse (slwdn)	
1	111	Asic output clock (cclk_0)	

Analog Test Control:

Table 7-4 DLL analog test control in dll_ctrl

test_hizb_a	test_ctrl_en	test_ctrl_a[1:0]	Function	Suggested Default

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test_hizb_a	test_ctrl_en	test_ctrl_a[1:0]	Function	Suggested Default
0	x	xx	Tri-state	0,0,00
1	0	xx	MVSS	
1	1	00	Filter output (Vc)	
1	1	01	Replica bias output for NMOS (Vbn)	
1	1	10	Replica bias output for PMOS (Vbp)	
1	1	11	MVDD	

Bias Generator Trim:

The bias generator trim capability can be used to adjust the behavior of the bias voltages being supplied to the delay line. Characteristics of the DLL that may warrant an adjustment of this trim value include the inability to lock due to a slow clock (suggest decreasing Vc adjust), inability to lock due to fast clock (suggest increasing Vc adjust) and increase noise margin on bias voltages (suggest decreasing Fmax adjust).The bit fields described in the following table can be set to any value between 000(binary) and 111(binary).

Table 7-5 bias generator trim in dll_ctrl

Field	Setting	Function	Suggested Default
bias_trm[2:0]	000	Fmax trim: minimum adjust	111
	111	Fmax trim: maximum adjust	
bias_trm[6:4]	000	Vc level trim: minimum adjust	011
	111	Vc level trim: maximum adjust	

Feedback Trim:

The feedback trim capability can be used in the event that an adjustment is desired in the phase detector feedback of the DLL. Characteristics of the DLL that may warrant an adjustment of this trim value include non-optimal phase alignment. The lower 3 bits (2:0) are used for feed-back delay trimming and the upper 3 bits (5:3) are used for feed-forward delay trimming. The feed-back trimming is used to decrease total delay, decreasing the amount of delay between phase outputs. The feed-forward trimming is used to increase total delay, increasing the amount of delay between phase outputs. For each 3-bit field, the inputs can be set to any value between 000(binary) and 111(binary).

Table 7-6 MDLL feedback trim in dll_ctrl

Field	Setting	Function	Suggested Default
fb_trm[5:3] (feed-forward path)	000	Minimum additional delay	000
	111	Maximum additional delay	
fb_trm[2:0] (feed-back path)	000	Minimum additional delay	000
	111	Maximum additional delay	

Bypass Mode

The DLL has a bypass mode which allows phased clocks to be generated with analog locking circuitry disabled. This mode may be used for low-speed functional testing and for IDDq testing. Bypass mode can also be used when operating with LPDDR SDRAMs. When bypass mode is enabled, all analog circuitry is disabled, and all static current paths are shut down.

Bypass mode has two settings for the clk_90 delay to optimize it for two different frequency ranges.

Table 7-7 MDLL bypass mode frequency range in dll_ctrl

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Field	Setting	Function	Suggested Default
bps200	0	0 to 100MHz	0
	1	0 to 200MHz	

It is also possible to trim the 90-degree delay using the fdtrm control bits.

Table 7-8 fdtrm control bits in dll_ctrl

Field	Setting	Function	Suggested Default
fdtrm[1:0]	00	nominal delay	00
	01	nominal delay – 10%	
	10	nominal delay + 10%	
	11	nominal delay + 20%	

7.4.4 Master-Slave DLL(MSDLL)

Master-Slave DLL for DDR2, and LPDDR applications is an integrated Delay Locked Loop and a pair of slave delays.The Delay Locked Loop (DLL) takes an input reference clock (clk_in), and generates four clock outputs, each delayed in quarter clock cycle (90º) increments. These four clock phases (clk_0, clk_90, clk_180, clk_270) can be generated with very high accuracy and low jitter across a wide range of frequencies.

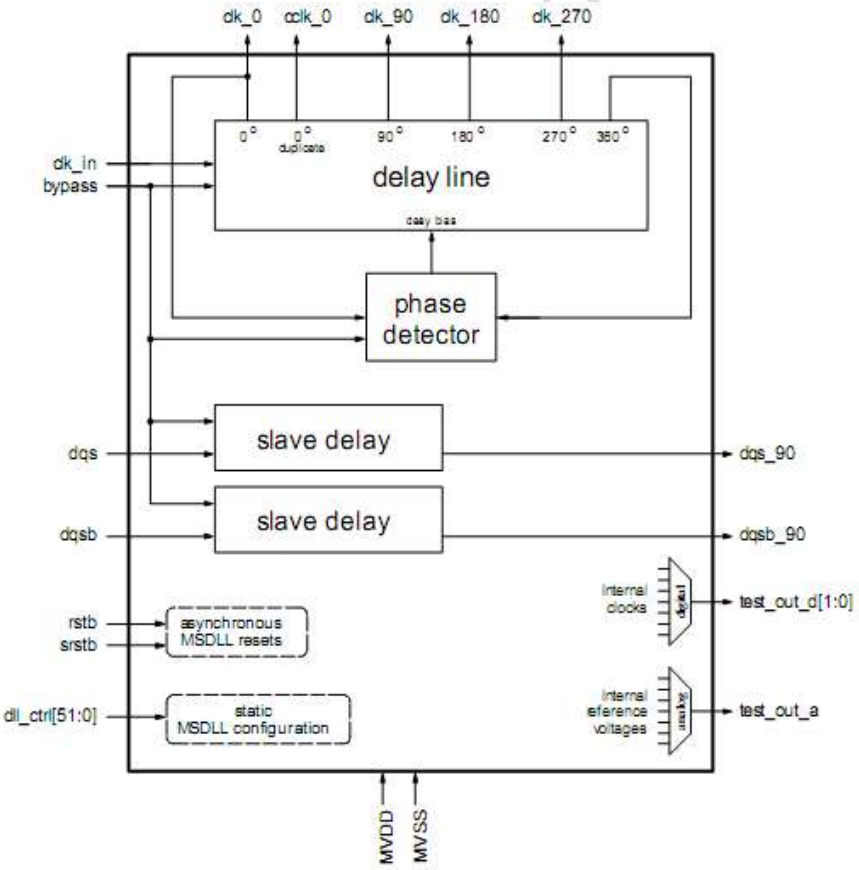

Fig. 7-6 DDR PHY master-slave DLL architecture diagram

The slave delay pair uses timing reference from the delay line to provide a highly accurate 90º delay to dqs and dqsb inputs (generating dqs_90 and dqsb_90 respectively).
A number of test modes and configuration settings are included:

A bypass mode shuts down all analog circuitry, and directly buffers the input clock and strobes with appropriate delays and inversions to the output clocks and strobes. This mode can be used for low speed functional or IDDQ testing.

A digital test output (test_out_d) provides direct observability of several internal reference clock and timing nodes.

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An analog test output (test_out_a) provides direct observability of several internal reference voltages.

The primary application for MSDLL is a DDR2 Byte Lane PHY with Interface Timing Modules (ITMs).

MSDLL Control for Trim and Test

The performance and testing of the MSDLL can be accessed through the dll_ctrl bus. Many of these controls are the same as the MDLL, therefore, this section only describes the settings that are different.

Table 7-9 DDR PHYMSDLL control for trim and test

Static Input		Field	Description
dll_ctrl	[1:0]		Reserved
	[4:2]	ipump_trm[2:0]	Charge pump current trim
	[5]	test_ctrl_en	Test control enable for analog and digital test outputs
	[8:6]	test_ctrl_d[2:0]	Digital test control. Selects the digital signal to be viewed at the digital test output
	[10:9]	test_ctrl_a[1:0]	Analog test control. Selects the analog signal to be viewed at the analog test output
	[11]	test_ctrl_switch	Test control switch. Selects the analog and digital test signals of master or slave
	[14:12]	bias_trm[2:0]	Master bias generator frequency trim
	[19,15]	fdtrm[1:0]	Master bypass fixed delay trim
	[18:16]	bias_trm[6:4]	Master bias generator control voltage trim
	[22:20]	sl_bias_trm[2:0]	Slavebias generator control voltage trim
	[23]	bps200	Bypass frequency select
	[26:24]	sl_bias_trm[6:4]	Slave bias generator control voltage trim
	[28:27]	fdtrm_sl[1:0]	Slave bypass fixed delay trim
	[29]	lock_det_en	Lock detector enable
	[31:30]		Reserved
	[37:32]	sl_fb_trm[5:0]	Slave feedback delay adjust
	[43:38]	fb_trm[5:0]	Master feedback delay adjust
	[45:44]	sl_bypass_start_up[1:0]	Slave auto-startup bypass
	[49:46]	sl_phase_trm[3:0]	Slave phase lock trim
	[50]	test_hizb_a	Analog test output tri-stated control
	[51]		Reserved

MSDLL Digital Test Control:

Table 7-10 MSDLL digital test control in dll_ctrl

test_ctrl_en	test_ctrl_switch	test_ctrl_d[2:0]	Function	Suggested Default
0	x	xx	digital test outputs disabled (drive '0')	0,0,000
1	0	000	0°output clock (clk_0)	
1		001	90°output clock (clk_90)	
1		010	180° output clock	

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test_ctrl_en	test_ctrl_switch	test_ctrl_d[2:0]	Function	Suggested Default
			(clk_180)	
1		011	270° output clock (clk_270)	
1		100	360° internal clock (clk_360_int)	
1		101	Master speed-up pulse (spdup)	
1		110	Master slow-down pulse (slwdn)	
1		111	Output clock (cclk_0)	
1	1	000	Input signal dqs	
1		001	Slave input clock reference (clk_90_in)	
1		010	Slave internal feedback clock (clk_0_out)	
1		011	Output signal dqsb_90	
1		100	Output signal dqs_90	
1		101	Slave speed-up pulse (spdup)	
1		110	Slave slow-down pulse (slwdn)	
1		111	Auto-lock enable signal	

MSDLL Analog Test Control:

Table 7-11 MSDLL analog test control in dll_ctrl

test_hizb_a	test_ctrl_en	test_ctrl_switch	test_ctrl_a[1:0]	Function	Suggested Default
0	x	x	xx	Tri-state	0,0,0,00
1	0	x	xx	MVSS	
1	1	0	00	Master Filter output (Vc)	
1	1		01	Master Replica bias output for NMOS (Vbn)	
1	1		10	Master Replica bias output for PMOS (Vbp)	
1	1		11	MVDD	
1	1	1	00	Slave Filter output (Vc)	
1	1		01	Slave Replica bias output	

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test_hizb_a	test_ctrl_en	test_ctrl_switch	test_ctrl_a[1:0]	Function	Suggested Default
				for NMOS (Vbn)	
1	1		10	Slave Replica bias output for PMOS (Vbp)	
1	1		11	MVDD	

MSDLL Lock Detector Enable:

This setting enables start of the slave DLL section after the master DLL section has reached lock. Characteristics of the DLL that may warrant an adjustment of this trim value include the slave DLL delay remaining in it's reset state (minimum delay, much less than 90 degrees) after the DLL lock time.

Table 7-12 MSDLL lock detector enable in dll_ctrl

Field	Setting	Function	Suggested Default
lock_det_en	0	Disable lock detector	0
	1	Enable lock detector	

Slave Auto-Startup Bypass:

By default, the slave DLL automatically starts to lock during the time the master is locking, after the master has begun to approach lock. This setting permits the user to manually start-up the slave DLL. To bypass the automatic startup, this setting should be set to '10'. Once the specified number of clocks has passed for the master DLL to achieve lock, the user sets this field to '11' to permit the slave DLL to startup. The user then waits for the specified number of clocks for the slave DLL to lock before proceeding. Characteristics of the slave DLL that might warrant a manual startup of the slave DLL include the inability for the slave DLL to produce a consistent and/or correct phase difference between the input signal and the output signal.

Table 7-13 slave auto_startup bypass in dll_ctrl

sl_bypass_start_up[1:0]	Function	Suggested Default
0X	Slave DLL automatically starts up	00
10	Slave DLL's automatic startup is disabled; the phase detector is disabled	
11	Slave DLL's automatic startup is disabled; the phase detector is enabled	

Slave DLL Phase Trim:

Selects the phase difference between the input signal and the corresponding output signal of the slave DLL. This setting applies to the dqs to dqs_90 and dqsb to dqsb_90 paths. The nominal phase difference is 90 degrees. Users may select to modify this value to account for factors external to the DLL, which require the DLL to produce a delay of greater than or less than the nominal 90 degrees. When modifying the value of these bits, the user does not need to issue a reset to the DLL but should wait the equivalent of the DLL lock time before the slave DLL circuitry is used (such as, receiving Read data from an SDRAM) to ensure the DLL has adequate time to stabilize with the new settings.

Table 7-14 slave DLL phase trim in dll_ctrl

sl_phase_trm[3:0]	Phase Difference (degrees)	Suggested Default
0000	90	0000
0001	72	

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sl_phase_trm[3:0]	Phase Difference (degrees)	Suggested Default
0010	54	
0011	36	
0100	108	
0101	90	
0110	72	
0111	54	
1000	126	
1001	108	
1010	90	
1011	72	
1100	144	
1101	126	
1110	108	
1111	90	

MSDLL Bypass Mode

The DLL bypass mode, when enabled, shuts down all analog delay paths and phase detection circuitry and generates output clocks as directly buffered and inverted versions of clk_in. Bypass mode can be used for low-speed functional testing or for IDDQ testing. Bypass mode can also be used when operating with LPDDR SDRAMs. When bypass mode is enabled, all analog circuitry is disabled, and all static current paths are shut down. Phased outputs are generated during bypass with inverters and standard delays:

clk_0 = buffered clk_in
clk_90 = delayed version of clk_0
clk_180 = inverted clk_0
clk_270 = inverted clk_90
cclk_0 = buffered clk_in
dqs_90 = delayed version of dqs
dqsb_90 = delayed version of dqsb

Bypass mode has two settings for the clk_90 delay to optimize it for two different frequency ranges same as MDLL.

It is also possible to trim the MDLL 90 degree delay using the fdtrm control bits same as MDLL. And it is also possible to trim the MSDLL 90 degree delay using the fdtrm_sl control bits same as fdtrm.

7.4.5 DQS Gating

DDR2 systems use a bidirectional data strobe which is driven by the host during memory writes, and by the SDRAM during memory reads. During active read commands, the ITMS basically acts as a buffer for the incoming DQS/DQS_b. A turn-around time exists between operations when neither device is driving the bus, and the strobe traces are held by termination circuitry at a mid-rail voltage.

While the DQS lines are held at mid-rail during inactive periods, an unknown value X is being received by the SSTL inputs. To prevent X from causing false transitions and other negative effects within the read path, the input read dqs strobe path is disabled when there is no active read data. The ITMS provides the functions to enable/disable this path, while the control of these functions is provided by the memory controller logic. A basic view of the enable/disable requirements is shown in following figure.

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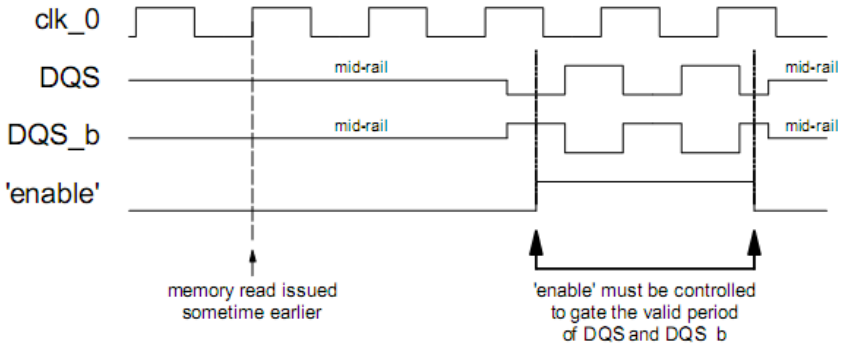

Fig. 7-7 Strobe Gating Requirements During Read Operations

After a read is issued, the SDRAM drives DQS and DQS_b for a number of clock cycles equal to the read burst length. Differing SDRAM CAS latencies, clock cycle times, board trace lengths, and other analog factors between controller and SDRAM result in a variable latency between when the read was issued, and when the returning DQS/DQS_b strobes reach the ITMS. The goal of DQS gating is to control a window, which enables and disables the input read dqs path only when the DQS lines are active, not when they are at mid-rail. There is a pre-amble and post-amble surrounding the active DQS edges that is used as the point to perform the enabling and disabling of this window.

There are two windowing schemes supported by the ITMS - passive windowing and active windowing - which are selected by input dqs_config.

Passive Windowing

In the passive windowing mode (dqs_config = 1), the controller asserts dqs_en at the start of the window and de-asserts dqs_en at the end of the window. This provides the course (clock-cycle) position of the enable and disable edges. Fine tuning (1/4 clock cycle) of the window placement is selected by phase_sel[1:0].

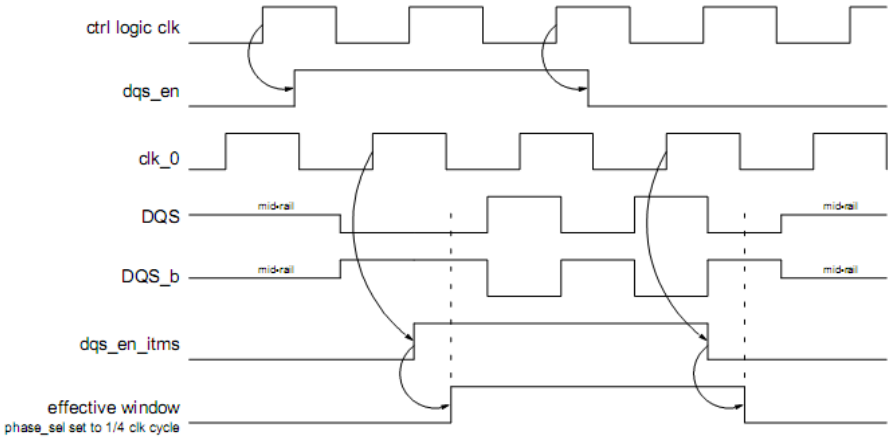

Fig. 7-8 DQS gating – passive windowing mode

The phase_sel[1:0] settings are provided.

Table 7-15 phase selection for dqs gating

phase_sel[1:0] Phase Selection		
Setting	**Selected Phase**	**Offset**
00	clk_90 (90 deg)	1/4 clock cycle
01	clk_180 (180 deg)	1/2 clock cycle
10	clk_270 (270 deg)	3/4 clock cycle
11	clk_0 (360 deg)	1 clock cycle

Active Windowing

The active windowing mode addresses the fact that the postamble is shorter than the preamble. The optimal window position for the preamble and postamble are not necessarily the same. In the active windowing mode (dqs_config = 0), the controller asserts dqs_en for one clock cycle at the start of the window and asserts dqs_dis for one clock cycle at the end of the window. Internal to ITMS, the assertion of dqs_dis is shifted by a further 180 degrees to account for the

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fact that DQS_b occurs 180 degrees later than DQS. This provides the course (clock-cycle) position of the enable and disable edges.
Fine tuning (1/4 clock cycle) of the window placement is selected by phase_sel[1:0]. The effective window is opened in the same manner as in the passive windowing mode, such as dqs_en assertion plus the phase_sel offset. To close the window, the controller asserts dqs_dis to inform the ITMS to expect the last DQS_b rising edge of the burst. The phase_sel setting is applied to this to set the effective time at which to expect the last DQS_b rising edge. The last DQS_b rising edge of the burst is also the last data of the burst. This last DQS_b rising edge is used to close the window. Thus, the window is self-closing.

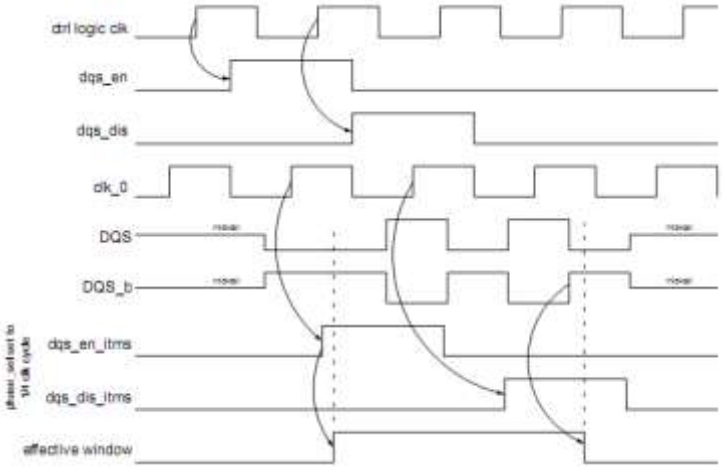

Fig. 7-9 DQS gating – active windowing mode

7.4.6 Dynamic Strobe Drift Detection

DDR2 systems can have a long round-trip path from the controller clock output (CK), to the SDRAM, and back to the controller data strobe input (DQS). The sum of potential variations in this path can exceed 25% of a clock cycle at high frequencies (>300MHz), so some compensation should be made if the path delay increases or decreases slowly, but significantly, during normal operation.

The ITMS component has a two-bit strobe drift indicator (dqs_drift), which changes value in grey code if the returning strobe drifts across internal 90° timing reference boundaries. The absolute value of this indicator is not important, but the change in value over time is.

Table 7-16 dynamic strobe drift indicators

dqs_drift[1:0]		DQS Drift Direction	Required Changes
Old Value	New Value		
00	01	forward	increase read data latency by 90 degrees
	10	backward	decrease read data latency by 90 degrees
01	11	forward	increase read data latency by 90 degrees
	00	backward	decrease read data latency by 90 degrees
10	00	forward	increase read data latency by 90 degrees
	11	backward	decrease read data latency by 90 degrees
11	10	forward	increase read data latency by 90 degrees
	01	backward	decrease read data latency by 90 degrees

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7.5 Register description

7.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR_PCTL_SCFG	0x0000	W	0x00000300	State Configuration Register
DDR_PCTL_SCTL	0x0004	W	0x00000000	Operational State Control Register
DDR_PCTL_STAT	0x0008	W	0x00000000	Operational State Status Register
DDR_PCTL_INTRSTAT	0x000c	W	0x00000000	Interrupt Status Register
DDR_PCTL_MCMD	0x0040	W	0x00100000	Memory Command Register
DDR_PCTL_POWCTL	0x0044	W	0x00000000	Power Up Control Register
DDR_PCTL_POWSTAT	0x0048	W	0x00000000	Power Up Status Register
DDR_PCTL_CMDTSTAT	0x004c	W	0x00000000	Command Timers Status Register
DDR_PCTL_CMDTSTATEN	0x0050	W	0x00000000	Command Timers Status Enable Register
DDR_PCTL_MRRCFG0	0x0060	W	0x00000000	Mode Register Read Configuration 0
DDR_PCTL_MRRSTAT0	0x0064	W	0x00000000	Mode Register Read Status 0 Register
DDR_PCTL_MRRSTAT1	0x0068	W	0x00000000	Mode Register Read Status 0 Register
DDR_PCTL_MCFG	0x0080	W	0x00040020	Memory Configuration Register
DDR_PCTL_PPCFG	0x0084	W	0x00000000	Partially Populated Memories Configuration Register
DDR_PCTL_MSTAT	0x0088	W	0x00000000	Memory Status Register
DDR_PCTL_LPDDR2ZQCFG	0x008c	W	0xab0a560a	LPDDR2 ZQ Configuration Register
DDR_PCTL_MCFG1	0x007C	W	0x00000000	Memory Configuration 1 Register
DDR_PCTL_DTUPDES	0x0094	W	0x00000000	DTU Status Register
DDR_PCTL_DTUNA	0x0098	W	0x00000000	DTU Number of Addresses Created Register
DDR_PCTL_DTUNE	0x009c	W	0x00000000	DTU Number of Errors Register
DDR_PCTL_DTUPRD0	0x00a0	W	0x00000000	DTU Parallel Read 0 Register
DDR_PCTL_DTUPRD1	0x00a4	W	0x00000000	DTU Parallel Read 1 Register
DDR_PCTL_DTUPRD2	0x00a8	W	0x00000000	DTU Parallel Read 2 Register
DDR_PCTL_DTUPRD3	0x00ac	W	0x00000000	DTU Parallel Read 3 Register
DDR_PCTL_DTUAWDT	0x00b0	W	0x00000290	DTU Address Width Register
DDR_PCTL_TOGCNT1U	0x00c0	W	0x00000064	Toggle Counter 1us Register
DDR_PCTL_TINIT	0x00c4	W	0x000000c8	t_init Timing Register
DDR_PCTL_TRSTH	0x00c8	W	0x00000000	t_rsth Timing Register
DDR_PCTL_TOGCNT100N	0x00cc	W	0x00000001	Toggle Counter 100ns
DDR_PCTL_TREFI	0x00d0	W	0x00000001	t_refi Timing Register
DDR_PCTL_TMRD	0x00d4	W	0x00000001	t_mrd Timing Register
DDR_PCTL_TRFC	0x00d8	W	0x00000001	t_rfc Timing Register

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Name	Offset	Size	Reset Value	Description
DDR_PCTL_TRP	0x00dc	W	0x00010006	t_trp Timing Register
DDR_PCTL_TRTW	0x00e0	W	0x00000002	t_rtw Timing Register
DDR_PCTL_TAL	0x00e4	W	0x00000000	AL Register
DDR_PCTL_TCL	0x00e8	W	0x00000004	CL Timing Register
DDR_PCTL_TCWL	0x00ec	W	0x00000003	CWL Timing Register
DDR_PCTL_TRAS	0x00f0	W	0x00000010	t_ras Timing Register
DDR_PCTL_TRC	0x00f4	W	0x00000016	t_rc Timing Register
DDR_PCTL_TRCD	0x00f8	W	0x00000006	t_rcd Timing Register
DDR_PCTL_TRRD	0x00fc	W	0x00000004	t_rrd Timing Register
DDR_PCTL_TRTP	0x0100	W	0x00000003	t_rtp Timing Register
DDR_PCTL_TWR	0x0104	W	0x00000006	t_wr Register
DDR_PCTL_TWTR	0x0108	W	0x00000004	t_wtr Timing Register
DDR_PCTL_TEXSR	0x010c	W	0x00000001	t_exsr Timing Register
DDR_PCTL_TXP	0x0110	W	0x00000001	t_xp Timing Register
DDR_PCTL_TXPDLL	0x0114	W	0x00000000	t_xpdll Timing Register
DDR_PCTL_TZQCS	0x0118	W	0x00000000	t_zqcs Timing Register
DDR_PCTL_TZQCSI	0x011c	W	0x00000000	t_zqcsi Timing Register
DDR_PCTL_TDQS	0x0120	W	0x00000001	t_dqs Timing Register
DDR_PCTL_TCKSRE	0x0124	W	0x00000000	t_cksre Timing Register
DDR_PCTL_TCKSRX	0x0128	W	0x00000000	t_cksrx Timing Register
DDR_PCTL_TCKE	0x012c	W	0x00000003	t_cke Timing Register
DDR_PCTL_TMOD	0x0130	W	0x00000000	t_mod Timing Register
DDR_PCTL_TRSTL	0x0134	W	0x00000000	Reset Low Timing Register
DDR_PCTL_TZQCL	0x0138	W	0x00000000	t_zqcl Timing Register
DDR_PCTL_TMRR	0x013c	W	0x00000002	t_mrr Timing Register
DDR_PCTL_TCKESR	0x0140	W	0x00000004	t_ckesr Timing Register
DDR_PCTL_TDPD	0x0144	W	0x00000000	t_dpd Timing Register
DDR_PCTL_DTUWACTL	0x0200	W	0x00000000	DTU Write Address Control
DDR_PCTL_DTURACTL	0x0204	W	0x00000000	DTU Read Address Control Register
DDR_PCTL_DTUCFG	0x0208	W	0x00000000	DTU Configuration Control Register
DDR_PCTL_DTUECTL	0x020c	W	0x00000000	DTU Execute Control Register
DDR_PCTL_DTUWD0	0x0210	W	0x00000000	DTU Write Data #0 Register
DDR_PCTL_DTUWD1	0x0214	W	0x00000000	DTU Write Data #1 Register
DDR_PCTL_DTUWD2	0x0218	W	0x00000000	DTU Write Data #2 Register
DDR_PCTL_DTUWD3	0x021c	W	0x00000000	DTU Write Data #3 Register
DDR_PCTL_DTUWDM	0x0220	W	0x00000000	DTU Write Data Mask Register
DDR_PCTL_DTURD0	0x0224	W	0x00000000	DTU Read Data #0 Register
DDR_PCTL_DTURD1	0x0228	W	0x00000000	DTU Read Data #1 Register
DDR_PCTL_DTURD2	0x022c	W	0x00000000	DTU Read Data #2 Register
DDR_PCTL_DTURD3	0x0230	W	0x00000000	DTU Read Data #3 Register

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Name	Offset	Size	Reset Value	Description
DDR_PCTL_DTULFSRWD	0x0234	W	0x00000000	DTU LFSR Seed for Write Data Generation Register
DDR_PCTL_DTULFSRRD	0x0238	W	0x00000000	DTU LFSR Seed for Read Data Generation Register
DDR_PCTL_DTUEAF	0x023c	W	0x00000000	DTU Error Address FIFO Register
DDR_PCTL_DFITCTRLDELAY	0x0240	W	0x00000002	DFI tctrl_delay Register
DDR_PCTL_DFIODTCFG	0x0244	W	0x00000000	DFI ODT Configuration
DDR_PCTL_DFIODTCFG1	0x0248	W	0x06060000	DFI ODT Timing Configuration 1 (for Latency and Length)
DDR_PCTL_DFIODTRANKMAP	0x024c	W	0x00008421	DFI ODT Rank Mapping
DDR_PCTL_DFITPHYWRDATA	0x0250	W	0x00000001	DFI tphy_wrdata Register
DDR_PCTL_DFITPHYWRLAT	0x0254	W	0x00000001	DFI tphy_wrlat Register
DDR_PCTL_DFITRDDATAEN	0x0260	W	0x00000001	DFI trddata_en Register
DDR_PCTL_DFITPHYRDLAT	0x0264	W	0x0000000f	DFI tphy_rdlat Register
DDR_PCTL_DFITPHYUPDTYPE0	0x0270	W	0x00000010	DFI tphyupd_type0 Register
DDR_PCTL_DFITPHYUPDTYPE1	0x0274	W	0x00000010	DFI tphyupd_type1 Register
DDR_PCTL_DFITPHYUPDTYPE2	0x0278	W	0x00000010	DFI tphyupd_type2 Register
DDR_PCTL_DFITPHYUPDTYPE3	0x027c	W	0x00000010	DFI tphyupd_type3 Register
DDR_PCTL_DFITCTRLUPDMIN	0x0280	W	0x00000010	DFI tctrlupd_min Register
DDR_PCTL_DFITCTRLUPDMAX	0x0284	W	0x00000040	DFI tctrlupd_max Register
DDR_PCTL_DFITCTRLUPDDLY	0x0288	W	0x00000008	DFI tctrlupddly Register
DDR_PCTL_DFIUPDCFG	0x0290	W	0x00000003	DFI Update Configuration Register
DDR_PCTL_DFITREFMSKI	0x0294	W	0x00000000	DFI Masked Refresh Interval
DDR_PCTL_DFITCTRLUPDI	0x0298	W	0x00000000	DFI tctrlupd_interval Register
DDR_PCTL_DFITRCFG0	0x02ac	W	0x00000000	DFI Training Configuration 0 Register
DDR_PCTL_DFITRSTAT0	0x02b0	W	0x00000000	DFI Training Status 0 Register
DDR_PCTL_DFITRWRLVLEN	0x02b4	W	0x00000000	DFI Training dfi_wrlvl_en Register
DDR_PCTL_DFITRRDLVLEN	0x02b8	W	0x00000000	DFI Training dfi_rdlvl_en Register
DDR_PCTL_DFITRRDLVLGATEEN	0x02bc	W	0x00000000	DFI Training dfi_rdlvl_gate_en Register
DDR_PCTL_DFISTSTAT0	0x02c0	W	0x00000000	DFI Status Status 0 Register
DDR_PCTL_DFISTCFG0	0x02c4	W	0x00000000	DFI Status Configuration 0 Register

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Name	Offset	Size	Reset Value	Description
DDR_PCTL_DFISTCFG1	0x02c8	W	0x00000000	DFI Status Configuration 1 Register
DDR_PCTL_DFITDRAMCLKEN	0x02d0	W	0x00000002	DFI tdram_clk_enable Register
DDR_PCTL_DFITDRAMCLKDIS	0x02d4	W	0x00000002	DFI tdram_clk_disable Register
DDR_PCTL_DFISTCFG2	0x02d8	W	0x00000000	DFI Status Configuration 2 Register
DDR_PCTL_DFISTPARCLR	0x02dc	W	0x00000000	DFI Status Parity Clear Register
DDR_PCTL_DFISTPARLOG	0x02e0	W	0x00000000	DFI Status Parity Log Register
DDR_PCTL_DFILPCFG0	0x02f0	W	0x00070000	DFI Low Power Configuration 0 Register
DDR_PCTL_DFITRWRLVLRESP0	0x0300	W	0x00000000	DFI Training dfi_wrlvl_resp Status 0 Register
DDR_PCTL_DFITRWRLVLRESP1	0x0304	W	0x00000000	DFI Training dfi_wrlvl_resp Status 1 Register
DDR_PCTL_DFITRWRLVLRESP2	0x0308	W	0x00000000	DFI Training dfi_wrlvl_resp Status 2 Register
DDR_PCTL_DFITRRDLVLRESP0	0x030c	W	0x00000000	DFI Training dfi_rdlvl_resp Status 0 Register
DDR_PCTL_DFITRRDLVLRESP1	0x0310	W	0x00000000	DFI Training dfi_rdlvl_resp Status 1 Register
DDR_PCTL_DFITRRDLVLRESP2	0x0314	W	0x00000000	DFI Training dfi_rdlvl_resp Status 2 Register
DDR_PCTL_DFITRWRLVLDELAY0	0x0318	W	0x00000000	DFI Training dfi_wrlvl_delay Configuration 0 Register
DDR_PCTL_DFITRWRLVLDELAY1	0x031c	W	0x00000000	DFI Training dfi_wrlvl_delay Configuration 1 Register
DDR_PCTL_DFITRWRLVLDELAY2	0x0320	W	0x00000000	DFI Training dfi_wrlvl_delay Configuration 2 Register
DDR_PCTL_DFITRRDLVLDELAY0	0x0324	W	0x00000000	DFI Training dfi_rdlvl_delay Configuration 0 Register
DDR_PCTL_DFITRRDLVLDELAY1	0x0328	W	0x00000000	DFI Training dfi_rdlvl_delay Configuration 1 Register
DDR_PCTL_DFITRRDLVLDELAY2	0x032c	W	0x00000000	DFI Training dfi_rdlvl_delay Configuration 2 Register
DDR_PCTL_DFITRRDLVLGATEDELAY0	0x0330	W	0x00000000	DFI Training dfi_rdlvl_gate_delay Configuration 0
DDR_PCTL_DFITRRDLVLGATEDELAY1	0x0334	W	0x00000000	DFI Training dfi_rdlvl_gate_delay Configuration 1
DDR_PCTL_DFITRRDLVLGATEDELAY2	0x0338	W	0x00000000	DFI Training dfi_rdlvl_gate_delay Configuration 2
DDR_PCTL_DFITRCMD	0x033c	W	0x00000000	DFI Training Command Register

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Name	Offset	Size	Reset Value	Description
DDR_PCTL_IPVR	0x03f8	W	0x00000000	IP Version Register
DDR_PCTL_IPTR	0x03fc	W	0x44574300	IP Type Register

Name	Offset	Size	Reset Value	Description
DDR_PUBL_RIDR	0x0000	W	0x00100140	Revision Identification Register
DDR_PUBL_PIR	0x0004	W	0x00000000	PHY Initialization Register
DDR_PUBL_PGCR	0x0008	W	0x01bc2e04	PHY General Configuration Register
DDR_PUBL_PGSR	0x000c	W	0x00000000	PHY General Status Register
DDR_PUBL_DLLGCR	0x0010	W	0x03737000	DLL General Control Register
DDR_PUBL_ACDLLCR	0x0014	W	0x40000000	AC DLL Control Register
DDR_PUBL_PTR0	0x0018	W	0x0022af9b	PHY Timing Register 0
DDR_PUBL_PTR1	0x001c	W	0x0604111d	PHY Timing Register 1
DDR_PUBL_PTR2	0x0020	W	0x042da072	PHY Timing Register 2
DDR_PUBL_ACIOCR	0x0024	W	0x33c03812	AC I/O Configuration Register
DDR_PUBL_DXCCR	0x0028	W	0x00000800	DATX8 Common Configuration Register
DDR_PUBL_DSGCR	0x002c	W	0xfa00001f	DDR System General Configuration Register
DDR_PUBL_DCR	0x0030	W	0x0000000b	DRAM Configuration Register
DDR_PUBL_DTPR0	0x0034	W	0x3092666e	DRAM Timing Parameters Register 0
DDR_PUBL_DTPR1	0x0038	W	0x09830090	DRAM Timing Parameters Register 1
DDR_PUBL_DTPR2	0x003c	W	0x1001a0c8	DRAM Timing Parameters Register 2
DDR_PUBL_MR0	0x0040	W	0x00000a52	Mode Register 0
DDR_PUBL_MR1	0x0044	W	0x00000000	Mode Register 1
DDR_PUBL_MR2	0x0048	W	0x00000000	Mode Register 2
DDR_PUBL_MR3	0x004c	W	0x00000000	Mode Register 3
DDR_PUBL_ODTCR	0x0050	W	0x00210000	ODT Configuration Register
DDR_PUBL_DTAR	0x0054	W	0x00000000	Data Training Address Register
DDR_PUBL_DTDR0	0x0058	W	0xdd22ee11	Data Training Data Register 0
DDR_PUBL_DTDR1	0x005c	W	0x7788bb44	Data Training Data Register 1
DDR_PUBL_DCUAR	0x00c0	W	0x00000000	DCU Address Register
DDR_PUBL_DCUDR	0x00c4	W	0x00000000	DCU Data Register
DDR_PUBL_DCURR	0x00c8	W	0x00000000	DCU Run Register
DDR_PUBL_DCULR	0x00cc	W	0x00000000	DCU Loop Register
DDR_PUBL_DCUGCR	0x00d0	W	0x00000000	DCU General Configuration Register
DDR_PUBL_DCUTPR	0x00d4	W	0x00000000	DCU Timing Parameters Registers
DDR_PUBL_DCUSR0	0x00d8	W	0x00000000	DCU Status Register 0
DDR_PUBL_DCUSR1	0x00dc	W	0x00000000	DCU Status Register 1
DDR_PUBL_BISTRR	0x0100	W	0x00000000	BIST Run Register
DDR_PUBL_BISTMSKR0	0x0104	W	0x00000000	BIST Mask Register 0
DDR_PUBL_BISTMSKR1	0x0108	W	0x00000000	BIST Mask Register 1
DDR_PUBL_BISTWCR	0x010c	W	0x00000020	BIST Word Count Register

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Name	Offset	Size	Reset Value	Description
DDR_PUBL_BISTLSR	0x0110	W	0x1234abcd	BIST LFSR Seed Register
DDR_PUBL_BISTAR0	0x0114	W	0x00000000	BIST Address Register 0
DDR_PUBL_BISTAR1	0x0118	W	0x0000000c	BIST Address Register 1
DDR_PUBL_BISTAR2	0x011c	W	0x7fffffff	BIST Address Register 2
DDR_PUBL_BISTUDPR	0x0120	W	0xffff0000	BIST User Data Pattern Register
DDR_PUBL_BISTGSR	0x0124	W	0x00000000	BIST General Status Register
DDR_PUBL_BISTWER	0x0128	W	0x00000000	BIST Word Error Register
DDR_PUBL_BISTBER0	0x012c	W	0x00000000	BIST Bit Error Register 0
DDR_PUBL_BISTBER1	0x0130	W	0x00000000	BIST Bit Error Register 1
DDR_PUBL_BISTBER2	0x0134	W	0x00000000	BIST Bit Error Register 2
DDR_PUBL_BISTWCSR	0x0138	W	0x00000000	BIST Word Count Status Register
DDR_PUBL_BISTFWR0	0x013c	W	0x00000000	BIST Fail Word Register 0
DDR_PUBL_BISTFWR1	0x0140	W	0x00000000	BIST Fail Word Register 1
DDR_PUBL_ZQ0CR0	0x0180	W	0x0000014a	ZQ 0 Impedance Control Register 0
DDR_PUBL_ZQ0CR1	0x0184	W	0x0000007b	ZQ 0 Impedance Control Register 1
DDR_PUBL_ZQ0SR0	0x0188	W	0x00000000	ZQ 0 Impedance Status Register 0
DDR_PUBL_ZQ0SR1	0x018c	W	0x00000000	ZQ 0 Impedance Status Register 1
DDR_PUBL_ZQ1CR0	0x0190	W	0x0000014a	ZQ 1 Impedance Control Register 0
DDR_PUBL_ZQ1CR1	0x0194	W	0x0000007b	ZQ 1 Impedance Control Register 1
DDR_PUBL_ZQ1SR0	0x0198	W	0x00000000	ZQ 1 Impedance Status Register 0
DDR_PUBL_ZQ1SR1	0x019c	W	0x00000000	ZQ 1 Impedance Status Register 1
DDR_PUBL_ZQ2CR0	0x01a0	W	0x0000014a	ZQ 2 Impedance Control Register 0
DDR_PUBL_ZQ2CR1	0x01a4	W	0x0000007b	ZQ 2 Impedance Control Register 1
DDR_PUBL_ZQ2SR0	0x01a8	W	0x00000000	ZQ 2 Impedance Status Register 0
DDR_PUBL_ZQ2SR1	0x01ac	W	0x00000000	ZQ 2 Impedance Status Register 1
DDR_PUBL_ZQ3CR0	0x01b0	W	0x0000014a	ZQ 3 Impedance Control Register 0
DDR_PUBL_ZQ3CR1	0x01b4	W	0x0000007b	ZQ 3 Impedance Control Register 1
DDR_PUBL_ZQ3SR0	0x01b8	W	0x00000000	ZQ 3 Impedance Status Register 0
DDR_PUBL_ZQ3SR1	0x01bc	W	0x00000000	ZQ 3 Impedance Status Register 1
DDR_PUBL_DX0GCR	0x01c0	W	0x00000681	DATX8 0 General Configuration Register
DDR_PUBL_DX0GSR0	0x01c4	W	0x00000000	DATX8 0 General Status Register 0
DDR_PUBL_DX0GSR1	0x01c8	W	0x00000000	DATX8 0 General Status Register 1
DDR_PUBL_DX0DLLCR	0x01cc	W	0x40000000	DATX8 0 DLL Control Register
DDR_PUBL_DX0DQTR	0x01d0	W	0xffffffff	DATX8 0 DQ Timing Register
DDR_PUBL_DX0DQSTR	0x01d4	W	0x3db05000	DATX8 0 DQS Timing Register
DDR_PUBL_DX1GCR	0x0200	W	0x00000681	DATX8 1 General Configuration Register
DDR_PUBL_DX1GSR0	0x0204	W	0x00000000	DATX8 1 General Status Register 0
DDR_PUBL_DX1GSR1	0x0208	W	0x00000000	DATX8 1 General Status Register 1
DDR_PUBL_DX1DLLCR	0x020c	W	0x40000000	DATX8 1 DLL Control Register
DDR_PUBL_DX1DQTR	0x0210	W	0xffffffff	DATX8 1 DQ Timing Register

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Name	Offset	Size	Reset Value	Description
DDR_PUBL_DX1DQSTR	0x0214	W	0x3db05000	DATX8 1 DQS Timing Register
DDR_PUBL_DX2GCR	0x0240	W	0x00000681	DATX8 2 General Configuration Register
DDR_PUBL_DX2GSR0	0x0244	W	0x00000000	DATX8 2 General Status Register 0
DDR_PUBL_DX2GSR1	0x0248	W	0x00000000	DATX8 2 General Status Register 1
DDR_PUBL_DX2DLLCR	0x024c	W	0x40000000	DATX8 2 DLL Control Register
DDR_PUBL_DX2DQTR	0x0250	W	0xffffffff	DATX8 2 DQ Timing Register
DDR_PUBL_DX2DQSTR	0x0254	W	0x3db05000	DATX8 2 DQS Timing Register
DDR_PUBL_DX3GCR	0x0280	W	0x00000681	DATX8 3 General Configuration Register
DDR_PUBL_DX3GSR0	0x0284	W	0x00000000	DATX8 3 General Status Register 0
DDR_PUBL_DX3GSR1	0x0288	W	0x00000000	DATX8 3 General Status Register 1
DDR_PUBL_DX3DLLCR	0x028c	W	0x40000000	DATX8 3 DLL Control Register
DDR_PUBL_DX3DQTR	0x0290	W	0xffffffff	DATX8 3 DQ Timing Register
DDR_PUBL_DX3DQSTR	0x0294	W	0x3db05000	DATX8 3 DQS Timing Register

*Notes: Size: **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

7.5.2 Detail Registers Description

DDR_PCTL_SCFG
Address: Operational Base + offset (0x0000)
State Configuration Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x3	bbflags_timing The n_bbflags is a NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes are scheduled by the TCU block. It may be possible to de-assert n_bbflags earlier than calculated by the TCU block. Programming bbflags_timing is used to achieve this. The maximum recommended value is: UPCTL_TCU_SED_P - TRP.t_rp. The programmed value is the maximum number of "early" cycles that n_bbflags maybe de-asserted. The actual achieved de-assertion depends on the traffic profile. In 1:2 mode the maximum allowed programmable value is 4'b0111 In 1:1 mode the value can be 4'b1111
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	nfifo_nif1_dis For internal use only for NFIFO testing. 1'b0: Only supported setting 1'b1: For internal use only
5:1	RO	0x0	reserved
0	RW	0x0	hw_low_power_en Enables the hardware low-power interface. Allows the system to request via hardware (c_sysreq input) to enter the memories into Self-Refresh. The handshaking between the request and acknowledge hardware low power signals (c_sysreq and c_sysack, respectively) is always performed, but the uPCTL response depends on the value set on this register field and by the value driven on the c_active_in input pin. 1'b0: Disabled. Requests are always denied and uPCTL is unaffected by c_sysreq 1'b1: Enabled. Requests are accepted or denied, depending on the current operational state of uPCTL and on the value of c_active_in

DDR_PCTL_SCTL
Address: Operational Base + offset (0x0004)
Operational State Control Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	state_cmd Issues an operational state transition request to the uPCTL. 3'b000: INIT (move to Init_mem from Config) 3'b001: CFG (move to Config from Init_mem or Access) 3'b010: GO (move to Access from Config) 3'b011: SLEEP (move to Low_power from Access) 3'b100: WAKEUP (move to Access from Low_power) Others: Reserved

DDR_PCTL_STAT
Address: Operational Base + offset (0x0008)
Operational State Status Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RO	0x0	lp_trig Reports the status of what triggered an entry to Low_power state. Is only set if in Low_power state. The individual bits report the following: - lp_trig[2]: Software driven due to SCTL.state_cmd==SLEEP - lp_trig[1]: Hardware driven due to Hardware Low Power Interface - lp_trig[0]: Hardware driven due to Auto Self Refresh (MCFG1.sr_idle>0) *Note: if more than one trigger happens at the exact same time, more than one bit of lp_trig may be asserted high.*
3	RO	0x0	reserved
2:0	RO	0x0	ctl_stat Returns the current operational state of the uPCTL. 3'b000: Init_mem 3'b001: Config 3'b010: Config_req 3'b011: Access 3'b100: Access_req 3'b101: Low_power 3'b110: Low_power_entry_req 3'b111: Low_power_exit_req

DDR_PCTL_INTRSTAT
Address: Operational Base + offset (0x000c)
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	parity_intr Indicates that a DFI parity error has been detected 1'b0: No error 1'b1: Parity error
0	RO	0x0	ecc_intr Indicates that an ECC error has been detected 1'b0: No error 1'b1: Parity error

DDR_PCTL_MCMD
Address: Operational Base + offset (0x0040)
Memory Command Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31	R/WSC	0x0	start_cmd Start command. When this bit is set to 1, the command operation defined in the cmd_opcode field is started. This bit is automatically cleared by the uPCTL after the command is finished. The application can poll this bit to determine when uPCTL is ready to accept another command. This bit cannot be cleared to 1'b0 by software.
30:28	RO	0x0	reserved
27:24	RW	0x0	cmd_add_del Set the additional delay associated with each command to 2^n internal timers clock cycles, where n is the bit field value. If n=0, the delay is 0. Max value is n=10.
23:20	RW	0x1	rank_sel Rank select for the command to be executed. 4'b0001: Rank 0 4'b0010: Rank 1 4'b0100: Rank 2 4'b1000: Rank 3 4'b0000: Reserved Multiple 1'b1s in rank_sel mean multiple ranks are selected, which is useful broadcasting commands in parallel to multiple ranks during initialization and configuration of the memories. If MCMD.cmd_opcode=RSTL, all ranks should be selected as it cannot be performed to individual ranks.
19:17	RW	0x0	bank_addr Mode Register address driven on the memory bank address bits, BA1, BA0, during a Mode Register Set operation, defined by cmd_opcode=MRS. For other values of cmd_opcode, this field is ignored. 3'b000: MR0 (MR in DDR2) 3'b001: MR1 (EMR in DDR2) 3'b010: MR2 (EMR(2) in DDR2) 3'b011: MR3 (EMR(3) in DDR2) Others: Reserved

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Bit	Attr	Reset Value	Description
16:4	RW	0x0000	cmd_addr Mode Register value driven on the memory address bits, A12 to A0, during a Mode Register Set operation defined by cmd_opcode=MRS. For other values of cmd_opcode this field is ignored. Refer to the memory specification for the correct settings of the various bits of this field during a MRS operation. If LPDDR2, this fields is merged into bank_addr - lpddr2_addr.
3:0	RW	0x0	cmd_opcode Command to be issued to the memory. 4'b0000: Deselect. This is only used for timing purposes, no actual direct Deselect command is passed to the memories 4'b0001: Precharge All (PREA) 4'b0010: Refresh (REF) 4'b0011: Mode Register Set (MRS) - is MRW in LPDDR2, MRS otherwise 4'b0100: ZQ Calibration Short (ZQCS, only applies to LPDDR2/DDR3) 4'b0101: ZQ Calibration Long (ZQCL, only applies to LPDDR2/DDR3) 4'b0110: Software Driven Reset (RSTL, only applies to DDR3) 4'b0111: Reserved 4'b1000: Mode Register Read (MRR) - is MRR in LPDDR2, is SRR in mDRR and is MPR in DDR3 4'b1001: Deep Power Down Entry (DPDE, only applies to mDDR/LPDDR2) Others: Reserved

DDR_PCTL_POWCTL
Address: Operational Base + offset (0x0044)
Power Up Control Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	R/WSC	0x0	power_up_start Start the memory power up sequence. When this bit is set to 1'b1, uPCTL starts the CKE and RESET power up sequence to the memories. This bit is automatically cleared by uPCTL after the sequence is completed. This bit cannot be cleared to 1'b0 by software.

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DDR_PCTL_POWSTAT
Address: Operational Base + offset (0x0048)
Power Up Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	power_up_done Returns the status of the memory power-up sequence. 1'b0: Power-up sequence has not been performed 1'b1: Power-up sequence has been performed

DDR_PCTL_CMDTSTAT
Address: Operational Base + offset (0x004c)
Command Timers Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	cmd_tstat Returns the status of the timers for memory commands. This ANDs all the command timers together. 1'b0: One or more command timers has not expired 1'b1: All command timers have expired

DDR_PCTL_CMDTSTATEN
Address: Operational Base + offset (0x0050)
Command Timers Status Enable Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	cmd_tstat_en Enables the generation of the status of the timers for memory commands. Is enabled before CMDTSTAT register is read. 1'b0: Disabled 1'b1: Enabled

DDR_PCTL_MRRCFG0
Address: Operational Base + offset (0x0060)
Mode Register Read Configuration 0

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	mrr_byte_sel Selects which byte's data to store when performing an MRR command via MCMD. LegalValues: 0 .. 8

DDR_PCTL_MRRSTAT0
Address: Operational Base + offset (0x0064)
Mode Register Read Status 0 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	mrrstat_beat3 MRR/MPR read data beat 3
23:16	RO	0x00	mrrstat_beat2 MRR/MPR read data beat 2
15:8	RO	0x00	mrrstat_beat1 MRR/MPR read data beat 1
7:0	RO	0x00	mrrstat_beat0 MRR/MPR read data beat 0

DDR_PCTL_MRRSTAT1
Address: Operational Base + offset (0x0068)
Mode Register Read Status 0 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	mrrstat_beat7 MRR/MPR read data beat 7
23:16	RO	0x00	mrrstat_beat6 MRR/MPR read data beat 6
15:8	RO	0x00	mrrstat_beat5 MRR/MPR read data beat 5
7:0	RO	0x00	mrrstat_beat4 MRR/MPR read data beat 4

DDR_PCTL_MCFG
Address: Operational Base + offset (0x0080)
Memory Configuration Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	mddr_lpddr2_clock_stop_idle Clock stop idle period in n_clk cycles. Memories are placed into clock stop mode if the NIF is idle for mddr_lpddr2_clkstop_idle n_clk cycles. The automatic clock stop function is disabled when mddr_lpddr2_clkstop_idle=0. Clock stop mode is only applicable in mDDR/LPDDR2.
23:22	RW	0x0	mddr_lpddr2_en mDDR/LPDDR2 Enable. Enables support for mDDR or LPDDR2. 2'b00: mDDR/LPDDR2 Disabled 2'b10: mDDR Enabled 2'b11: LPDDR2 Enabled Others: Reserved.
21:20	RW	0x0	mddr_lpddr2_bl mDDR/LPDDR2 Burst Length. The BL setting must be consistent with the value programmed into the BL field of MR. 2'b00: BL2, Burst length of 2 (MR.BL=3'b001, mDDR only) 2'b01: BL4, Burst length of 4 (MR.BL=3'b010, for mDDR and LPDDR2) 2'b10: BL8, Burst length of 8 (MR.BL=3'b011, for mDDR and LPDDR2) 2'b11: BL16, Burst length of 16 (MR.BL=3'b100, for mDDR and LPDDR2) This value is effective only if MCFG.mddr_lpddr2_en[1]=1'b1. Otherwise, MCFG.mem_bl is used to define uPCTL's Burst Length (for DDR2/DDR3).
19:18	RW	0x1	tfaw_cfg Sets tFAW to be 4, 5 or 6 times tRRD. 2'b00: set tFAW=4*tRRD 2'b01: set tFAW=5*tRRD 2'b10: set tFAW=6*tRRD
17	RW	0x0	pd_exit_mode Selects the mode for Power Down Exit. For DDR2/DDR3, the power down exit mode setting in uPCTL must be consistent with the value programmed into the power down exit mode bit of MR0. For mDDR/LPDDR2, only fast exit mode is valid. 1'b0: slow exit 1'b1: fast exit

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Bit	Attr	Reset Value	Description
16	RW	0x0	pd_type Sets the Power down type. 1'b0: Precharge Power Down 1'b1: Active Power Down
15:8	RW	0x00	pd_idle Power-down idle period in n_clk cycles. Memories are placed into power-down mode if the NIF is idle for pd_idle n_clk cycles. The automatic power down function is disabled when pd_idle=0.
7	RO	0x0	reserved
6	RW	0x0	lpddr2_s4 Enables LPDDR2-S4 support. 1'b0: LPDDR2-S4 disabled (LPDDR2-S2 enabled) 1'b1: LPDDR2-S4 enabled
5	RW	0x1	ddr3_en Select DDR2 or DDR3 protocol. Ignored, if mDDR or LPDDR2 support is enabled. 1'b0: DDR2 Protocol Rules 1'b1: DDR3 Protocol Rules
4	RW	0x0	stagger_cs For multi-rank commands from the DCU, stagger the assertion of CS_N to odd and even ranks by one n_clk cycle. This is useful when using RDIMMs, when multi-rank commands may be interpreted as writes to control words in the register chip. 1'b0: Do not stagger CS_N 1'b1: Stagger CS_N
3	RW	0x0	two_t_en Enables 2T timing for memory commands. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	bl8int_en Setting this bit enables the BL8 interrupt function of DDR2. This is the capability to early terminate a BL8 after only 4 DDR beats by issuing the next command two cycles earlier. This functionality is only available for DDR2 memories and this setting is ignored for mDDR/LPDDR2 and DDR3. 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	cke_or_en This bit is intended to be set for 4-rank RDIMMs, which have a 2-bit CKE input. If set, dfi_cke[0] is asserted to enable either of the even ranks (0 and 2), while dfi_cke[1] is asserted to enable either of the odd ranks (1 and 3). dfi_cke[3:2] are inactive (0) 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	mem_bl DDR Burst Length. The BL setting in DDR2 / DDR3 must be consistent with the value programmed into the BL field of MR0. 1'b0: BL4, Burst length of 4 (MR0.BL=3'b010, DDR2 only) 1'b1: BL8, Burst length of 8 (MR0.BL=3'b011 for DDR2, MR0.BL=2'b00 for DDR3)

DDR_PCTL_PPCFG
Address: Operational Base + offset (0x0084)
Partially Populated Memories Configuration Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:1	RW	0x00	rpmem_dis Reduced Population Disable bits. Setting these bits disables the corresponding NIF/DDR data lanes from writing or reading data. Lane 0 is always present, hence only 8 bits are required for the remaining lanes including the ECC lane. In 1:2 mode bit 0 of rpmem_dis covers n_wdata/n_rdata/m_ctl_d/m_phy_q[63:32], bit 1 [95:64] etc. In 1:1 mode bit 0 of rpmem_dis covers n_wdata/n_rdata/m_ctl_d/m_phy_q[31:16], bit 2 [47:32] etc. There are no restrictions on which byte lanes can be disabled, other than byte lane 0 is required. Gaps between enabled byte lanes are allowed. For each bit: 1'b0: lane exists 1'b1: lane is disabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	ppmem_en Partially Population Enable bit. Setting this bit enables the partial population of external memories where the entire application bus is routed to a reduced size memory system. The lower half of the SDRAM data bus, bit 0 up to bit UPCTL_M_DW/2-1, is the active portion when Partially Populated memories are enabled. 1'b0: Disabled 1'b1: Enabled

DDR_PCTL_MSTAT
Address: Operational Base + offset (0x0088)
Memory Status Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	self_refresh Indicates if uPCTL, through auto self refresh, has placed the memories in Self Refresh. 1'b0: Memory is not in Self Refresh 1'b1: Memory is in Self Refresh
1	RO	0x0	clock_stop Indicates if uPCTL has placed the memories in Clock Stop. 1'b0: Memory is not in Clock Stop 1'b1: Memory is in Clock Stop
0	RO	0x0	power_down Indicates if uPCTL has placed the memories in Power Down. 1'b0: Memory is not in Power Down 1'b1: Memory is in Power-Down

DDR_PCTL_LPDDR2ZQCFG
Address: Operational Base + offset (0x008c)
LPDDR2 ZQ Configuration Register

Bit	Attr	Reset Value	Description
31:24	RW	0xab	zqcl_op Value to drive on memory address bits [19:12] for an automatic hardware generated ZQCL command (LPDDR2). Corresponds to OP7 .. OP0 of Mode Register Write (MRW) command which is used to send ZQCL command to memory.

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Bit	Attr	Reset Value	Description
23:16	RW	0x0a	zqcl_ma Value to drive on memory address bits [11:4] for an automatic hardware generated ZQCL command (LPDDR2). Corresponds to MA7 .. MA0 of Mode Register Write (MRW) command which is used to send ZQCL command to memory.
15:8	RW	0x56	zqcs_op Value to drive on memory address bits [19:12] for an automatic hardware generated ZQCS command (LPDDR2). Corresponds to OP7 .. OP0 of Mode Register Write (MRW) command which is used to send ZQCS command to memory.
7:0	RW	0x0a	zqcs_ma Value to drive on memory address bits [11:4] for an automatic hardware generated ZQCS command (LPDDR2). Corresponds to MA7 .. MA0 of Mode Register Write (MRW) command which is used to send ZQCS command to memory.

DDR_PCTL_MCFG1
Address: Operational Base + offset (0x0090)
Memory Configuration 1 Register

Bit	Attr	Reset Value	Description
31	RW	0x0	hw_exit_idle_en When this bit is programmed to 1'b1 the c_active_in pin can be used to exit from the automatic clock stop, power down or self-refresh modes.
30:24	RO	0x0	reserved
23:16	RW	0x00	hw_idle Hardware idle period. The c_active output is driven high if the NIF is idle in Access state for hw_idle * 32 * n_clk cycles. The hardware idle function is disabled when hw_idle=0.
15:8	RO	0x0	reserved
7:0	RW	0x00	sr_idle Self Refresh idle period. Memories are placed into Self-Refresh mode if the NIF is idle in Access state for sr_idle * 32 * n_clk cycles. The automatic self refresh function is disabled when sr_idle=0.

DDR_PCTL_DTUPDES
Address: Operational Base + offset (0x0094)
DTU Status Register

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Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RO	0x0	dtu_rd_missing Indicates if one or more read beats of data did not return from memory
12:9	RO	0x0	dtu_eaffl Indicates the number of entries in the FIFO that is holding the log of error addresses for data comparison
8	RO	0x0	dtu_random_error Indicates that the random data generated had some failures when written and read to the memories
7	RO	0x0	dtu_err_b7 Detected at least 1 bit error for bit 7 in the programmable data buffers
6	RO	0x0	dtu_err_b6 Detected at least 1 bit error for bit 6 in the programmable data buffers
5	RO	0x0	dtu_err_b5 Detected at least 1 bit error for bit 5 in the programmable data buffers
4	RO	0x0	dtu_err_b4 Detected at least 1 bit error for bit 4 in the programmable data buffers
3	RO	0x0	dtu_err_b3 Detected at least 1 bit error for bit 3 in the programmable data buffers
2	RO	0x0	dtu_err_b2 Detected at least 1 bit error for bit 2 in the programmable data buffers
1	RO	0x0	dtu_err_b1 Detected at least 1 bit error for bit 1 in the programmable data buffers
0	RO	0x0	dtu_err_b0 Detected at least 1 bit error for bit 0 in the programmable data buffers

DDR_PCTL_DTUNA

Address: Operational Base + offset (0x0098)

DTU Number of Addresses Created Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dtu_num_address Indicates the number of addresses that were created on the NIF interface during random data generation

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DDR_PCTL_DTUNE
Address: Operational Base + offset (0x009c)
DTU Number of Errors Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dtu_num_errors Indicates the number of errors that were detected on the readback of the NIF data during random data generation.

DDR_PCTL_DTUPRD0
Address: Operational Base + offset (0x00a0)
DTU Parallel Read 0 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_1 Allows all the bit ones from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_0 Allows all the bit zeros from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUPRD1
Address: Operational Base + offset (0x00a4)
DTU Parallel Read 1 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_3 Allows all the bit threes from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_2 Allows all the bit twos from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUPRD2
Address: Operational Base + offset (0x00a8)
DTU Parallel Read 2 Register

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_5 Allows all the bit fives from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_4 Allows all the bit fours from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUPRD3
Address: Operational Base + offset (0x00ac)
DTU Parallel Read 3 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_7 Allows all the bit sevens from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_6 Allows all the bit sixes from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUAWDT
Address: Operational Base + offset (0x00b0)
DTU Address Width Register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:9	RW	0x1	number_ranks Number of supported memory ranks. 2'b00: 1 rank 2'b01: 2 ranks 2'b10: 3 ranks 2'b11: 4 ranks
8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x2	row_addr_width Width of the memory row address bits. 2'b00: 13 bits wide 2'b01: 14 bits wide 2'b10: 15 bits wide 2'b11: 16 bits wide
5	RO	0x0	reserved
4:3	RW	0x2	bank_addr_width Width of the memory bank address bits. 2'b00: 2 bits wide (4 banks) 2'b01: 3 bits wide (8 banks) Others: Reserved
2	RO	0x0	reserved
1:0	RW	0x0	column_addr_width Width of the memory column address bits. 2'b00: 7 bits wide 2'b01: 8 bits wide 2'b10: 9 bits wide 2'b11: 10 bits wide

DDR_PCTL_TOGCNT1U
Address: Operational Base + offset (0x00c0)
Toggle Counter 1us Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x064	toggle_counter_1u The number of internal timers clock cycles

DDR_PCTL_TINIT
Address: Operational Base + offset (0x00c4)
t_init Timing Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x0c8	t_init Defines the time period (in us) to hold dfi_cke and dfi_reset_n stable during the memory power up sequence. The value programmed must correspond to at least 200us. The actual time period defined is TINIT * TOGCNT1U * internal timers clock period.

DDR_PCTL_TRSTH

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Address: Operational Base + offset (0x00c8)
t_rsth Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	t_rsth Defines the time period (in us) to hold the dfi_reset_n signal high after it is de-asserted during the DDR3 Power Up/Reset sequence. The value programmed for DDR3 must correspond to minimum 500us of delay. For mDDR and DDR2, this register should be programmed to 0.The actual time period defined is TRSTH * TOGCNT1U * internal timers clock period.

DDR_PCTL_TOGCNT100N
Address: Operational Base + offset (0x00cc)
Toggle Counter 100ns

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x01	toggle_counter_100n The number of internal timers clock cycles

DDR_PCTL_TREFI
Address: Operational Base + offset (0x00d0)
t_refi Timing Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x01	t_refi Defines the time period (in 100ns units) of the Refresh interval. The actual time period defined is TREFI * TOGCNT100N * internal timers clock period.

DDR_PCTL_TMRD
Address: Operational Base + offset (0x00d4)
t_mrd Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x1	t_mrd Mode Register Set command cycle time in memory clock cycles. mDDR: Time from MRS to any valid command LPDDR2: Time from MRS (MRW) to any valid command DDR2: Time from MRS to any valid command DDR3: Time from MRS to MRS command mDDR Legal Values: 2 LPDDR2 Legal Values: 5 DDR2 Legal Values: 2..3 DDR3 Legal Values: 2..4

DDR_PCTL_TRFC
Address: Operational Base + offset (0x00d8)
t_rfc Timing Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x001	t_rfc Refresh to Active/Refresh command time in memory clock cycles. mDDR Legal Values: 7..28 LPDDR2 Legal Values: 15..112 DDR2 Legal Values: 15..131 DDR3 Legal Values: 36.. 374

DDR_PCTL_TRP
Address: Operational Base + offset (0x00dc)
t_trp Timing Register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x1	prea_extra Additional cycles required for a Precharge All (PREA) command - in addition to t_rp. In terms of memory clock cycles. mDDR Value: 0 LPDDR2 Value: Value that corresponds (tRPab -tRPpb). Rounded up in terms of memory clock cycles. Values can be 0, 1, 2. DDR2 Value: 1 if 8 Banks, 0 otherwise DDR3 Value: 0
15:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x6	t_rp Precharge period in memory clock cycles. For LPDDR2, this should be set to TRPpb. mDDR Legal Values: 2..3 LPDDR2 Legal Values: 3..13 DDR2 Legal Values: 3..7 DDR3 Legal Values: 5..14

DDR_PCTL_TRTW
Address: Operational Base + offset (0x00e0)
t_rtw Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	t_rtw Read to Write turnaround time in memory clock cycles. mDDR Legal Values: 3..11 LPDDR2 Legal Values: 1..11 DDR2 Legal Values: 2..10 DDR3 Legal Values: 2..10

DDR_PCTL_TAL
Address: Operational Base + offset (0x00e4)
AL Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	t_al Additive Latency in memory clock cycles. For DDR2 this must match the value programmed into the AL field of MR1. For DDR3 this must be 0, CL-1, CL-2 depending weather the AL value in MR1 is 0,1, or 2 respectively. CL is the CAS latency programmed into MR0. For mDDR and LPDDR2, there is no AL field in the mode registers, and this setting should be set to 0 mDDR Legal Values: 0 LPDDR2 Legal Values: 0 DDR2 Legal Values: AL DDR3 Legal Values: 0, CL-1, CL-2 (depending on AL=0,1,2 in MR1)

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DDR_PCTL_TCL
Address: Operational Base + offset (0x00e8)
CL Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x4	t_cl CAS Latency in memory clock cycles. If mDDR/DDR2/DDR3, the uPCTL setting must match the value programmed into the CL field of MR0. If LPDDR2, the uPCTL setting must match RL (ReadLatency), where RL is the value programmed into the "RL & W" field of MR2 mDDR/DDR2/3 Legal Value: CL LPDDR2 Legal Value: RL

DDR_PCTL_TCWL
Address: Operational Base + offset (0x00ec)
CWL Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x3	t_cwl CAS Write Latency in memory clock cycles. For mDDR, the setting must be 1. For LPDDR2 the setting must match WL (Write Latency), where WL is the value programmed into the "RL & WL" field of MR2. For DDR2 the setting must match CL-1, where CL is the value programmed into the CL field of MR0. For DDR3, the setting must match the value programmed in the memory CWL field of MR2. mDDR Legal Value: 1 LPDDR2 Legal Values: WL DDR2 Legal Value: CL-1 DDR3 Legal Value: CWL

DDR_PCTL_TRAS
Address: Operational Base + offset (0x00f0)
t_ras Timing Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x10	t_ras Activate to Precharge command time in memory clock cycles. mDDR Legal Values: 4..8 LPDDR2 Legal Values: 7..23 DDR2 Legal Values: 8..24 DDR3 Legal Values: 15..38

DDR_PCTL_TRC
Address: Operational Base + offset (0x00f4)
t_rc Timing Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x16	t_rc Row Cycle time in memory clock cycles. Specifies the minimum Activate to Activate distance for accesses to same bank. mDDR Legal Values: 5..11 LPDDR2 Legal Values: 10..36 DDR2 Legal Values: 11..31 DDR3 Legal Values: 20..52

DDR_PCTL_TRCD
Address: Operational Base + offset (0x00f8)
t_rcd Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x6	t_rcd Row to Column delay in memory clock cycles. Specifies the minimum Activate to Column distance. mDDR Legal Values: 2..3 LPDDR2 Legal Values: 3..13 DDR2 Legal Values: 3..7 DDR3 Legal Values: 5..14

DDR_PCTL_TRRD
Address: Operational Base + offset (0x00fc)
t_rrd Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x4	t_rrd Row-to-Row delay in memory clock cycles. Specifies the minimum Activate-to-Activate distance for consecutive accesses to different banks in the same rank. mDDR Legal Values: 1..2 LPDDR2 Legal Values: 2..6 DDR2 Legal Values: 2..6 DDR3 Legal Values: 4..8

DDR_PCTL_TRTP
Address: Operational Base + offset (0x0100)
t_rtp Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x3	t_rtp Read to Precharge time in memory clock cycles. Specifies the minimum distance Read to Precharge for consecutive accesses to same bank. mDDR Value: 0 LPDDR2 Legal Values: 2..4 DDR2 Legal Values: 2..4 DDR3 Legal Values: 3..8

DDR_PCTL_TWR
Address: Operational Base + offset (0x0104)
t_wr Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x06	t_wr Write recovery time in memory clock cycles. When using close page the uPCTL setting must be consistent with the WR field setting of MR0. mDDR Legal Values: 2..3 LPDDR2 Legal Values: 3..8 DDR2 Legal Values: 3..8 DDR3 Legal Values: 6..16

DDR_PCTL_TWTR
Address: Operational Base + offset (0x0108)
t_wtr Timing Register

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x4	t_wtr Write to Read turnaround time, in memory clock cycles. mDDR Legal Values: 1..2 LPDDR2 Legal Values: 2..4 DDR2 Legal Values: 2..4 DDR3 Legal Values: 3..8

DDR_PCTL_TEXSR
Address: Operational Base + offset (0x010c)
t_exsr Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x001	t_exsr Exit Self Refresh to first valid command delay, in memory clock cycles. For mDDR, this should be programmed to match tXSR. For LPDDR2, this should be programmed to match tXSR. For DDR2, this should be programmed to match tXSRD (SRE to read-related command) as defined by the memory device specification. For DDR3, this should be programmed to match tXSDLL (SRE to a command requiring DLL locked) as defined by the memory device specification. mDDR Legal Values: 17..40 LPDDR2 Legal Values: 17..117 DDR2 Typical Value: 200 DDR3 Typical Value: 512

DDR_PCTL_TXP
Address: Operational Base + offset (0x0110)
t_xp Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x1	t_xp Exit Power Down to first valid command delay when DLL is on (fast exit), measured in memory clock cycles. Legal Values: 1..7

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DDR_PCTL_TXPDLL
Address: Operational Base + offset (0x0114)
t_xpdll Timing Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	t_xpdll Exit Power Down to first valid command delay when DLL is off (slow exit), measured in memory clock cycles. mDDR/LPDDR2 Value: 0 DDR2/DDR3 Legal Values: 3..63

DDR_PCTL_TZQCS
Address: Operational Base + offset (0x0118)
t_zqcs Timing Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	t_zqcs SDRAM ZQ Calibration Short period, in memory clock cycles. Should be programmed to match the tZQCS timing value as defined in the memory specification. mDDR Value: 0 LPDDR2 Legal Values: 15..48 DDR2 Value: 0 DDR3 Typical Value: 64

DDR_PCTL_TZQCSI
Address: Operational Base + offset (0x011c)
t_zqcsi Timing Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t_zqcsi SDRAM ZQCS interval, measured in Refresh interval units. The total time period defined is TZQCSI*TREFI * TOGCNT100N * internal timers clock period. Programming a value of 0 in t_zqcsi disables the auto-ZQCS functionality in uPCTL. mDDR Value: 0 LPDDR2 Legal Values: 0..4294967295 DDR2 Value: 0 DDR3 Legal Values: 0..4294967295

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DDR_PCTL_TDQS
Address: Operational Base + offset (0x0120)
t_dqs Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x1	t_dqs Additional data turnaround time in memory clock cycles for accesses to different ranks. Used to increase the distance between column commands to different ranks, allowing more tolerance as the driver source changes on the bidirectional DQS and/or DQ signals. mDDR Legal Values: 1..7 LPDDR2 Legal Values: 1..7 DDR2 Legal Values: 1..7 DDR3 Legal Values: 1..7

DDR_PCTL_TCKSRE
Address: Operational Base + offset (0x0124)
t_cksre Timing Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	t_cksre In DDR3, this is the time after Self Refresh Entry that CKE is held high before going low. In memory clock cycles. Specifies the clock disable delay after SRE. This should be programmed to match the greatest value between 10ns and 5 memory clock periods. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 5..15

DDR_PCTL_TCKSRX
Address: Operational Base + offset (0x0128)
t_cksrx Timing Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	t_cksrx In DDR3, this is the time (before Self Refresh Exit) that CKE is maintained high before issuing SRX. In memory clock cycles. Specifies the clock stable time before SRX. This should be programmed to match the greatest value between 10ns and 5 memory clock periods. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 5..15

DDR_PCTL_TCKE
Address: Operational Base + offset (0x012c)
t_cke Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x3	t_cke CKE minimum pulse width in memory clock cycles. mDDR Legal Value: 2 LPDDR2 Legal Values: 3 DDR2 Legal Value: 3 DDR3 Legal Values: 3..6

DDR_PCTL_TMOD
Address: Operational Base + offset (0x0130)
t_mod Timing Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	t_mod In DDR3 mode, this is the time from MRS to any valid non-MRS command (except DESELECT or NOP) in memory clock cycles. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 0..31

DDR_PCTL_TRSTL
Address: Operational Base + offset (0x0134)
Reset Low Timing Register

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Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	t_rstl Memory Reset Low time, in memory clock cycles. Defines the time period to hold dfi_reset_n signal low during a software driven DDR3 Reset Operation. The value programmed must correspond to at least 100ns of delay. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 1..127

DDR_PCTL_TZQCL
Address: Operational Base + offset (0x0138)
t_zqcl Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	t_zqcl SDRAM ZQ Calibration Long period in memory clock cycles. If LPDDR2, should be programmed to tZQCL. If DDR3, should be programmed to match the memory tZQinit timing value for the first ZQCL command during memory initialization; should be programmed to match tZQoper timing value after reset and initialization. mDDR Value: 0 LPDDR2 Legal Values: 60..192 DDR2 Value: 0 DDR3 Legal Values: 0..1023

DDR_PCTL_TMRR
Address: Operational Base + offset (0x013c)
t_mrr Timing Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x02	t_mrr Time for a Mode Register Read (MRR command from MCMD)

DDR_PCTL_TCKESR
Address: Operational Base + offset (0x0140)

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t_ckesr Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x4	t_ckesr Minimum CKE low width for Self Refresh entry to exit timing in memory clock cycles. Recommended settings: mDDR: t_ckesr = 0 LPDDR2: t_ckesr = tCKESR setting from memories, rounded up in terms of memory cycles. DDR2: t_ckesr = 0 DDR3: t_ckesr = t_cke + 1 mDDR Value: 0 LPDDR2 Legal Values: 3..8 DDR2 Value: 0 DDR3 Legal Values: 4..7

DDR_PCTL_TDPD
Address: Operational Base + offset (0x0144)
t_dpd Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	t_dpd Minimum Deep Power Down time. Is in terms of us. When a MCMD.DPDE command occurs, TDPD time is waited before MCMD.start_cmd can be cleared. MCMD_cmd_add_del (if any) does not start until TDPD has completed. This ensures TDPD requirement for the memory is not violated. The actual time period defined is TDPD* TOGCNT1U * internal timers clock period. Only applies for mDDR and LPDDR2 as Deep Power Down (DPD) is only valid for these memory types. For mDDR, tDPD=0, while for LPDDR2, tDPD=500 us. For LPDDR2, if 500 us is waited externally by system, then set tDPD=0. mDDR Value: 0 LPDDR2 Legal Values: 0 or 500 DDR2 Legal Value: 0 DDR3 Legal Values: 0

DDR_PCTL_DTUWACTL
Address: Operational Base + offset (0x0200)
DTU Write Address Control

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	dtu_wr_rank Write rank to where data is to be targeted
29	RO	0x0	reserved
28:13	RW	0x0000	dtu_wr_row Write row to where data is to be targeted
12:10	RW	0x0	dtu_wr_bank Write bank to where data is to be targeted
9:0	RW	0x000	dtu_wr_col FWrite column to where data is to be targeted

DDR_PCTL_DTURACTL
Address: Operational Base + offset (0x0204)
DTU Read Address Control Register

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dtu_rd_rank Read rank from where data comes
29	RO	0x0	reserved
28:13	RW	0x0000	dtu_rd_row Read row from where data comes
12:10	RW	0x0	dtu_rd_bank Read bank from where data comes
9:0	RW	0x000	dtu_rd_col Read column from where data comes

DDR_PCTL_DTUCFG
Address: Operational Base + offset (0x0208)
DTU Configuration Control Register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x00	dtu_row_increments Number of times to increment the row address when generating random data, up to a maximum of 127 times.
15	RW	0x0	dtu_wr_multi_rd When set puts the DTU into write once multiple reads mode
14	RW	0x0	dtu_data_mask_en Controls whether random generated data masks are transmitted. Unless enabled all data bytes are written to memory and expected to be read from memory.

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Bit	Attr	Reset Value	Description
13:10	RW	0x0	dtu_target_lane Selects one of the byte lanes for data comparison into the programmable read data buffer
9	RW	0x0	dtu_generate_random Generate transfers using random data, otherwise generate transfers from the programmable write data buffers.
8	RW	0x0	dtu_incr_banks When the column address rolls over increment the bank address until we reach and conclude bank 7.
7	RW	0x0	dtu_incr_cols Increment the column address until we saturate. Return to zero if DTUCFG.dtu_incr_banks is set to 1 and we are not at bank 7.
6:1	RW	0x00	dtu_nalen Length of the NIF transfer sequence that is passed through the uPCTL for each created address.
0	RW	0x0	dtu_enable When set, allows the DTU module to take ownership of the NIF interface: 1'b1: DTU enabled 1'b0: DTU disabled

DDR_PCTL_DTUECTL
Address: Operational Base + offset (0x020c)
DTU Execute Control Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	R/WSC	0x0	wr_multi_rd_rst When set, resets the DTU in write once multiple reads mode, to allow a new write to be performed. This bit automatically clears.
1	R/WSC	0x0	run_error_reports When set, initiates the calculation of the error status bits. This bit automatically clears when the re-calculation is done. This is only used in debug mode to verify the comparison logic.
0	R/WSC	0x0	run_dtu When set, initiates the running of the DTU read and write transfer. This bit automatically clears when the transfers are completed.

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DDR_PCTL_DTUWD0
Address: Operational Base + offset (0x0210)
DTU Write Data #0 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte3 Write data byte
23:16	RW	0x00	dtu_wr_byte2 Write data byte
15:8	RW	0x00	dtu_wr_byte1 Write data byte
7:0	RW	0x00	dtu_wr_byte0 Write data byte

DDR_PCTL_DTUWD1
Address: Operational Base + offset (0x0214)
DTU Write Data #1 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte7 Write data byte
23:16	RW	0x00	dtu_wr_byte6 Write data byte
15:8	RW	0x00	dtu_wr_byte5 Write data byte
7:0	RW	0x00	dtu_wr_byte4 Write data byte

DDR_PCTL_DTUWD2
Address: Operational Base + offset (0x0218)
DTU Write Data #2 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte11 Write data byte
23:16	RW	0x00	dtu_wr_byte10 Write data byte
15:8	RW	0x00	dtu_wr_byte9 Write data byte
7:0	RW	0x00	dtu_wr_byte8 Write data byte

DDR_PCTL_DTUWD3
Address: Operational Base + offset (0x021c)
DTU Write Data #3 Register

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte15 Write data byte
23:16	RW	0x00	dtu_wr_byte14 Write data byte
15:8	RW	0x00	dtu_wr_byte13 Write data byte
7:0	RW	0x00	dtu_wr_byte12 Write data byte

DDR_PCTL_DTUWDM
Address: Operational Base + offset (0x0220)
DTU Write Data Mask Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	dm_wr_byte0 Write data mask bit, one bit for each byte. Each bit should be 0 for a byte lane that contains valid write data.

DDR_PCTL_DTURD0
Address: Operational Base + offset (0x0224)
DTU Read Data #0 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte3 Read byte
23:16	RO	0x00	dtu_rd_byte2 Read byte
15:8	RO	0x00	dtu_rd_byte1 Read byte
7:0	RO	0x00	dtu_rd_byte0 Read byte

DDR_PCTL_DTURD1
Address: Operational Base + offset (0x0228)
DTU Read Data #1 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte7 Read byte
23:16	RO	0x00	dtu_rd_byte6 Read byte

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	dtu_rd_byte5 Read byte
7:0	RO	0x00	dtu_rd_byte4 Read byte

DDR_PCTL_DTURD2
Address: Operational Base + offset (0x022c)
DTU Read Data #2 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte11 Read byte
23:16	RO	0x00	dtu_rd_byte10 Read byte
15:8	RO	0x00	dtu_rd_byte9 Read byte
7:0	RO	0x00	dtu_rd_byte8 Read byte

DDR_PCTL_DTURD3
Address: Operational Base + offset (0x0230)
DTU Read Data #3 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte15 Read byte
23:16	RO	0x00	dtu_rd_byte14 Read byte
15:8	RO	0x00	dtu_rd_byte13 Read byte
7:0	RO	0x00	dtu_rd_byte12 Read byte

DDR_PCTL_DTULFSRWD
Address: Operational Base + offset (0x0234)
DTU LFSR Seed for Write Data Generation Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dtu_lfsr_wseed This is the initial seed for the random write data generation LFSR (linear feedback shift register), shared with the write mask generation.

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DDR_PCTL_DTULFSRRD
Address: Operational Base + offset (0x0238)
DTU LFSR Seed for Read Data Generation Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dtu_lfsr_rseed This is the initial seed for the random read data generation LFSR (linear feedback shift register), this is shared with the read mask generation. The read data mask is reconstructed the same as the write data mask was created, allowing the " on the fly comparison" ignore bytes which were not written.

DDR_PCTL_DTUEAF
Address: Operational Base + offset (0x023c)
DTU Error Address FIFO Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	ea_rank Indicates the rank that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.
29	RO	0x0	reserved
28:13	RO	0x0000	ea_row Indicates the row that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.
12:10	RO	0x0	ea_bank Indicates the bank that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.
9:0	RO	0x000	ea_column Indicates the column address that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.

DDR_PCTL_DFITCTRLDELAY
Address: Operational Base + offset (0x0240)
DFI tctrl_delay Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	tctrl_delay Specifies the number of DFI clock cycles after an assertion or deassertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.

DDR_PCTL_DFIODTCFG
Address: Operational Base + offset (0x0244)
DFI ODT Configuration

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	rank3_odt_default Default ODT value of rank 3 when there is no read/write activity
27	RW	0x0	rank3_odt_write_sel Enable/disable ODT for rank 3 when a write access is occurring on this rank
26	RW	0x0	rank3_odt_write_nse Enable/disable ODT for rank 3 when a write access is occurring on a different rank
25	RW	0x0	rank3_odt_read_sel Enable/disable ODT for rank 3 when a read access is occurring on this rank
24	RW	0x0	rank3_odt_read_nsel Enable/disable ODT for rank 3 when a read access is occurring on a different rank
23:21	RO	0x0	reserved
20	RW	0x0	rank2_odt_default Default ODT value of rank 2 when there is no read/write activity
19	RW	0x0	rank2_odt_write_sel Enable/disable ODT for rank 2 when a write access is occurring on this rank
18	RW	0x0	rank2_odt_write_nse Enable/disable ODT for rank 2 when a write access is occurring on a different rank
17	RW	0x0	rank2_odt_read_sel Enable/disable ODT for rank 2 when a read access is occurring on this rank

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Bit	Attr	Reset Value	Description
16	RW	0x0	rank2_odt_read_nsel Enable/disable ODT for rank 2 when a read access is occurring on a different rank
15:13	RO	0x0	reserved
12	RW	0x0	rank1_odt_default Default ODT value of rank 1 when there is no read/write activity
11	RW	0x0	rank1_odt_write_sel Enable/disable ODT for rank 1 when a write access is occurring on this rank
10	RW	0x0	rank1_odt_write_nse Enable/disable ODT for rank 1 when a write access is occurring on a different rank
9	RW	0x0	rank1_odt_read_sel Enable/disable ODT for rank 1 when a read access is occurring on this rank
8	RW	0x0	rank1_odt_read_nsel Enable/disable ODT for rank 1 when a read access is occurring on a different rank
7:5	RO	0x0	reserved
4	RW	0x0	rank0_odt_default Default ODT value of rank 0 when there is no read/write activity
3	RW	0x0	rank0_odt_write_sel Enable/disable ODT for rank 0 when a write access is occurring on this rank
2	RW	0x0	rank0_odt_write_nse Enable/disable ODT for rank 0 when a write access is occurring on a different rank
1	RW	0x0	rank0_odt_read_sel Enable/disable ODT for rank 0 when a read access is occurring on this rank
0	RW	0x0	rank0_odt_read_nsel Enable/disable ODT for rank 0 when a read access is occurring on a different rank

DDR_PCTL_DFIODTCFG1
Address: Operational Base + offset (0x0248)
DFI ODT Timing Configuration 1 (for Latency and Length)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26:24	RW	0x6	odt_len_bl8_r ODT length for BL8 read transfers Length of dfi_odt signal for BL8 reads. This is in terms of SDR cycles. For BL4 reads, the length of dfi_odt is always 2 cycles shorter than the value in this register field.
23:19	RO	0x0	reserved
18:16	RW	0x6	odt_len_bl8_w ODT length for BL8 write transfers Length of dfi_odt signal for BL8 writes. This is in terms of SDR cycles. For BL4 writes, the length of dfi_odt is always 2 cycles shorter than the value in this register field.
15:13	RO	0x0	reserved
12:8	RW	0x00	odt_lat_r ODT latency for reads Latency after a read command that dfi_odt is set. This is in terms of SDR cycles.
7:5	RO	0x0	reserved
4:0	RW	0x00	odt_lat_w ODT latency for writes Latency after a write command that dfi_odt is set. This is in terms of SDR cycles.

DDR_PCTL_DFIODTRANKMAP
Address: Operational Base + offset (0x024c)
DFI ODT Rank Mapping

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x8	odt_rank_map3 Rank mapping for dfi_odt[3] Determines whether dfi_odt[3] should be asserted Bit 15 = 1: dfi_odt[3] will be asserted to terminate rank 3 Bit 14 = 1: dfi_odt[3] will be asserted to terminate rank 2 Bit 13 = 1: dfi_odt[3] will be asserted to terminate rank 1 Bit 12 = 1: dfi_odt[3] will be asserted to terminate rank 0 This field exists only if UPCTL_M_NRANKS = 4

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	odt_rank_map2 Rank mapping for dfi_odt[2] Determines which rank access(es) will cause dfi_odt[2] to be asserted Bit 11 = 1: dfi_odt[2] will be asserted to terminate rank 3 Bit 10 = 1: dfi_odt[2] will be asserted to terminate rank 2 Bit 9 = 1: dfi_odt[2] will be asserted to terminate rank 1 Bit 8 = 1: dfi_odt[2] will be asserted to terminate rank 0 This field exists only if UPCTL_M_NRANKS = 4
7:4	RW	0x2	odt_rank_map1 Rank mapping for dfi_odt[1] Determines which rank access(es) will cause dfi_odt[1] to be asserted Bit 7 = 1: dfi_odt[1] will be asserted to terminate rank 3 Bit 6 = 1: dfi_odt[1] will be asserted to terminate rank 2 Bit 5 = 1: dfi_odt[1] will be asserted to terminate rank 1 Bit 4 = 1: dfi_odt[1] will be asserted to terminate rank 0
3:0	RW	0x1	odt_rank_map0 Rank mapping for dfi_odt[0] Determines which rank access(es) will cause dfi_odt[0] to be asserted Bit 3 = 1: dfi_odt[0] will be asserted to terminate rank 3 Bit 2 = 1: dfi_odt[0] will be asserted to terminate rank 2 Bit 1 = 1: dfi_odt[0] will be asserted to terminate rank 1 Bit 0 = 1: dfi_odt[0] will be asserted to terminate rank 0

DDR_PCTL_DFITPHYWRDATA
Address: Operational Base + offset (0x0250)
DFI tphy_wrdata Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x01	tphy_wrdata Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted to when the associated write data is driven on the dfi_wrdata signal. This has no impact on performance, only adjusts the relative time between enable and data transfer.

DDR_PCTL_DFITPHYWRLAT
Address: Operational Base + offset (0x0254)
DFI tphy_wrlat Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x01	tphy_wrlat Specifies the number of DFI clock cycles between when a write command is sent on the DFI control interface and when the dfi_wrdata_en signal is asserted.

DDR_PCTL_DFITRDDATAEN
Address: Operational Base + offset (0x0260)
DFI trddata_en Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x01	trddata_en Specifies the number of DFI clock cycles from the assertion of a read command on the DFI to the assertion of the dfi_rddata_en signal.

DDR_PCTL_DFITPHYRDLAT
Address: Operational Base + offset (0x0264)
DFI tphy_rdlat Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x0f	tphy_rdlat Specifies the maximum number of DFI clock cycles allowed from the assertion of the dfi_rddata_en signal to the assertion of the dfi_rddata_valid signal.

DDR_PCTL_DFITPHYUPDTYPE0

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Address: Operational Base + offset (0x0270)
DFI tphyupd_type0 Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type0 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x0. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITPHYUPDTYPE1
Address: Operational Base + offset (0x0274)
DFI tphyupd_type1 Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type1 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x1. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITPHYUPDTYPE2
Address: Operational Base + offset (0x0278)
DFI tphyupd_type2 Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type2 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x2. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITPHYUPDTYPE3
Address: Operational Base + offset (0x027c)
DFI tphyupd_type3 Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type3 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x3. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITCTRLUPDMIN
Address: Operational Base + offset (0x0280)
DFI tctrlupd_min Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0010	tctrlupd_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted.

DDR_PCTL_DFITCTRLUPDMAX
Address: Operational Base + offset (0x0284)
DFI tctrlupd_max Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0040	tctrlupd_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert.

DDR_PCTL_DFITCTRLUPDDLY
Address: Operational Base + offset (0x0288)
DFI tctrlupddly Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x8	tctrlupd_dly Delay in DFI clock cycles between time a uPCTL-initiated update could be started and time uPCTL-initated update actually starts (dfi_ctrlupd_req going high).

DDR_PCTL_DFIUPDCFG
Address: Operational Base + offset (0x0290)

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DFI Update Configuration Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates: 1'b0 = Disabled 1'b1 = Enabled
0	RW	0x1	dfi_ctrlupd_en Enables the generation of uPCTL-initiated updates 1'b0: Disabled 1'b1: Enabled

DDR_PCTL_DFITREFMSKI
Address: Operational Base + offset (0x0294)
DFI Masked Refresh Interval

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	trefmski Time period of the masked Refresh interval. This value is only used if TREFI==0. Defines the time period (in 100ns units) of the masked Refresh (REFMSK) interval. The actual time period defined is DFITREFMSKI* TOGCNT100N * internal timers clock period.

DDR_PCTL_DFITCTRLUPDI
Address: Operational Base + offset (0x0298)
DFI tctrlupd_interval Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tctrlupd_interval DFI uPCTL-initiated updates interval, measured in terms of Refresh interval units. If TREFI != 0, the time period is defined as DFITCTRLUPDI*TREFI * TOGCNT100N * internal timers clock period. If TREFI == 0 and DFITREFMSKI != 0, the period changes to DFITCTRLUPDI * DFITREFMSKI * TOGCNT100N * internal timers clock period. Programming a value of 0 is the same as programming a value of 1; for instance, a uPCTL-initiated update occurs every Refresh interval.

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DDR_PCTL_DFITRCFG0
Address: Operational Base + offset (0x02ac)
DFI Training Configuration 0 Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	dfi_wrlvl_rank_sel Determines the value to drive on the output signal dfi_wrlvl_cs_n. The value on dfi_wrlvl_cs_n is the inverse of the setting in this field.
15:13	RO	0x0	reserved
12:4	RW	0x000	dfi_rdlvl_edge Determines the value to drive on the output signal dfi_rdlvl_edge. The value on dfi_rdlvl_edge is the same as the setting in this field.
3:0	RW	0x0	dfi_rdlvl_rank_sel Determines the value to drive on the output signal dfi_rdlvl_cs_n. The value on dfi_rdlvl_cs_n is the inverse of the setting in this field.

DDR_PCTL_DFITRSTAT0
Address: Operational Base + offset (0x02b0)
DFI Training Status 0 Register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RO	0x0	dfi_wrlvl_mode Reports the value of the input signal dfi_wrlvl_mode
15:10	RO	0x0	reserved
9:8	RO	0x0	dfi_rdlvl_gate_mode Reports the value of the input signal dfi_rdlvl_gate_mode
7:2	RO	0x0	reserved
1:0	RO	0x0	dfi_rdlvl_mode Reports the value of the input signal dfi_rdlvl_mode

DDR_PCTL_DFITRWRLVLEN
Address: Operational Base + offset (0x02b4)
DFI Training dfi_wrlvl_en Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	dfi_wrlvl_en Determines the value to drive on the output signal dfi_wrlvl_en

DDR_PCTL_DFITRRDLVLEN
Address: Operational Base + offset (0x02b8)
DFI Training dfi_rdlvl_en Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	dfi_rdlvl_en Determines the value to drive on the output signal dfi_rdlvl_en

DDR_PCTL_DFITRRDLVLGATEEN
Address: Operational Base + offset (0x02bc)
DFI Training dfi_rdlvl_gate_en Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	dfi_rdlvl_gate_en Determines the value to drive on the output signal dfi_rdlvl_gate_en

DDR_PCTL_DFISTSTAT0
Address: Operational Base + offset (0x02c0)
DFI Status Status 0 Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RO	0x000	dfi_data_byte_disable Reports the value of the output signal dfi_data_byte_disable
15:6	RO	0x0	reserved
5:4	RO	0x0	dfi_freq_ratio Reports the value of the output signal dfi_freq_ratio
3:2	RO	0x0	reserved
1	RO	0x0	dfi_init_start Reports the value of the output signal dfi_init_start
0	RO	0x0	dfi_init_complete Reports the value of the input signal dfi_init_complete

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DDR_PCTL_DFISTCFG0
Address: Operational Base + offset (0x02c4)
DFI Status Configuration 0 Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	dfi_data_byte_disable_en Enables the driving of the dfi_data_byte_disable signal. The value driven on dfi_data_byte_disable is dependent on the setting of PPCFG register. 1'b0: Drive dfi_data_byte_disable to default value of all zeroes 1'b1: Drive dfi_data_byte_disable according to value as defined by PPCFG register setting *Note: should be set to 1'b1 only after PPCFG is correctly set*
1	RW	0x0	dfi_freq_ratio_en Enables the driving of the dfi_freq_ratio signal. When enabled, the dfi_freq_ratio value driven is dependent on configuration parameter UPCTL_FREQ_RATIO: 2'b00 is driven when UPCTL_FREQ_RATIO=1; 2'b01 is driven when UPCTL_FREQ_RATIO=2. 1'b0: Drive dfi_freq_ratio to default value of 2'b00 1'b1: Drive dfi_freq_ratio value according to how configuration parameter is set
0	RW	0x0	dfi_init_start Sets the value of the dfi_init_start signal 1'b0: dfi_init_start is driven low 1'b1: dfi_init_start is driven high

DDR_PCTL_DFISTCFG1
Address: Operational Base + offset (0x02c8)
DFI Status Configuration 1 Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	dfi_dram_clk_disable_en_dpd Enables support of the dfi_dram_clk_disable signal with Deep Power Down (DPD). DPD is only for mDDR/LPDDR2. 1'b0: Disable dfi_dram_clk_disable support in relation to DPD 1'b1: Enable dfi_dram_clk_disable support in relation to DPD

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Bit	Attr	Reset Value	Description
0	RW	0x0	dfi_dram_clk_disable_en Enables support of the dfi_dram_clk_disable signal with Self Refresh (SR). 1'b0: Disable dfi_dram_clk_disable support in relation to SR 1'b1: Enable dfi_dram_clk_disable support in relation to SR

DDR_PCTL_DFITDRAMCLKEN
Address: Operational Base + offset (0x02d0)
DFI tdram_clk_enable Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	tdram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value.

DDR_PCTL_DFITDRAMCLKDIS
Address: Operational Base + offset (0x02d4)
DFI tdram_clk_disable Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	tdram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value.

DDR_PCTL_DFISTCFG2
Address: Operational Base + offset (0x02d8)
DFI Status Configuration 2 Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	parity_en Enables the DFI parity generation feature (driven on output signal dfi_parity_in) 1'b0: Disable DFI parity generation 1'b1: Enable DFI parity generation
0	RW	0x0	parity_intr_en Enable interrupt generation for DFI parity error (from input signal dfi_parity_error) 1'b0: Disable interrupt 1'b1: Enable interrupt

DDR_PCTL_DFISTPARCLR
Address: Operational Base + offset (0x02dc)
DFI Status Parity Clear Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	R/WSC	0x0	parity_log_clr Set this bit to 1'b1 to clear the DFI Status Parity Log register (DFISTPARLOG) 1'b0: Do not clear DFI status Parity Log register 1'b1: Clear DFI status Parity Log register
0	R/WSC	0x0	parity_intr_clr Set this bit to 1'b1 to clear the interrupt generated by an DFI parity error (as enabled by DFISTCFG2.parity_intr_en). It also clears the INTRSTAT.parity_intr register field. It is automatically cleared by hardware when the interrupt has been cleared.

DDR_PCTL_DFISTPARLOG
Address: Operational Base + offset (0x02e0)
DFI Status Parity Log Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	parity_err_cnt Increments any time the DFI parity logic detects a parity error(s) (on dfi_parity_error)

DDR_PCTL_DFILPCFG0
Address: Operational Base + offset (0x02f0)
DFI Low Power Configuration 0 Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_lp_wakeup_dpd Value to drive on dfi_lp_wakeup signal when Deep Power Down mode is entered. Determines the DFI's tlp_wakeup time: 4'b0000: 16 cycles 4'b0001: 32 cycles 4'b0010: 64 cycles 4'b0011: 128 cycles 4'b0100: 256 cycles 4'b0101: 512 cycles 4'b0110: 1024 cycles 4'b0111: 2048 cycles 4'b1000: 4096 cycles 4'b1001: 8192 cycles 4'b1010: 16384 cycles 4'b1011: 32768 cycles 4'b1100: 65536 cycles 4'b1101: 131072 cycles 4'b1110: 262144 cycles 4'b1111: Unlimited
27:25	RO	0x0	reserved
24	RW	0x0	dfi_lp_en_dpd Enables DFI Low Power interface handshaking during Deep Power Down Entry/Exit 1'b0: Disabled 1'b1: Enabled
23:20	RO	0x0	reserved
19:16	RW	0x7	dfi_tlp_resp Setting for tlp_resp time. Same value is used for both Power Down and Self refresh and Deep Power Down modes. DFI 2.1 specification, recommends using value of 7 always.

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	dfi_lp_wakeup_sr Value to drive on dfi_lp_wakeup signal when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time: 4'b0000: 16 cycles 4'b0001: 32 cycles 4'b0010: 64 cycles 4'b0011: 128 cycles 4'b0100: 256 cycles 4'b0101: 512 cycles 4'b0110: 1024 cycles 4'b0111: 2048 cycles 4'b1000: 4096 cycles 4'b1001: 8192 cycles 4'b1010: 16384 cycles 4'b1011: 32768 cycles 4'b1100: 65536 cycles 4'b1101: 131072 cycles 4'b1110: 262144 cycles 4'b1111: Unlimited
11:9	RO	0x0	reserved
8	RW	0x0	dfi_lp_en_sr Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	dfi_lp_wakeup_pd Value to drive on dfi_lp_wakeup signal when Power Down mode is entered. Determines the DFI's tlp_wakeup time: 4'b0000: 16 cycles 4'b0001: 32 cycles 4'b0010: 64 cycles 4'b0011: 128 cycles 4'b0100: 256 cycles 4'b0101: 512 cycles 4'b0110: 1024 cycles 4'b0111: 2048 cycles 4'b1000: 4096 cycles 4'b1001: 8192 cycles 4'b1010: 16384 cycles 4'b1011: 32768 cycles 4'b1100: 65536 cycles 4'b1101: 131072 cycles 4'b1110: 262144 cycles 4'b1111: Unlimited
3:1	RO	0x0	reserved
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit 1'b0: Disabled 1'b1: Enabled

DDR_PCTL_DFITRWRLVLRESP0
Address: Operational Base + offset (0x0300)
DFI Training dfi_wrlvl_resp Status 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_wrlvl_resp0 Reports the status of the dfi_wrlvl_resp[31:0] signal

DDR_PCTL_DFITRWRLVLRESP1
Address: Operational Base + offset (0x0304)
DFI Training dfi_wrlvl_resp Status 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_wrlvl_resp1 Reports the status of the dfi_wrlvl_resp[63:32] signal

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DDR_PCTL_DFITRWRLVLRESP2
Address: Operational Base + offset (0x0308)
DFI Training dfi_wrlvl_resp Status 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	dfi_wrlvl_resp2 Reports the status of the dif_wrlvl_resp[71:64] signal

DDR_PCTL_DFITRRDLVLRESP0
Address: Operational Base + offset (0x030c)
DFI Training dfi_rdlvl_resp Status 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rdlvl_resp0 Reports the status of the dif_rdlvl_resp[31:0] signal

DDR_PCTL_DFITRRDLVLRESP1
Address: Operational Base + offset (0x0310)
DFI Training dfi_rdlvl_resp Status 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rdlvl_resp1 Reports the status of the dif_rdlvl_resp[63:32] signal

DDR_PCTL_DFITRRDLVLRESP2
Address: Operational Base + offset (0x0314)
DFI Training dfi_rdlvl_resp Status 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	dfi_rdlvl_resp2 Reports the status of the dif_rdlvl_resp[71:64] signal

DDR_PCTL_DFITRWRLVLDELAY0
Address: Operational Base + offset (0x0318)
DFI Training dfi_wrlvl_delay Configuration 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_wrlvl_delay0 Sets the value to be driven on the signal dfi_wrlvl_delay_x[31:0]

DDR_PCTL_DFITRWRLVLDELAY1
Address: Operational Base + offset (0x031c)
DFI Training dfi_wrlvl_delay Configuration 1 Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_wrlvl_delay1 Sets the value to be driven on the signal dfi_wrlvl_delay_x[63:32]

DDR_PCTL_DFITRWRLVLDELAY2
Address: Operational Base + offset (0x0320)
DFI Training dfi_wrlvl_delay Configuration 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	dfi_wrlvl_delay2 Sets the value to be driven on the signal dfi_wrlvl_delay_x[71:64]

DDR_PCTL_DFITRRDLVLDELAY0
Address: Operational Base + offset (0x0324)
DFI Training dfi_rdlvl_delay Configuration 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_delay0 Sets the value to be driven on the signal dfi_rdlvl_delay_x[31:0]

DDR_PCTL_DFITRRDLVLDELAY1
Address: Operational Base + offset (0x0328)
DFI Training dfi_rdlvl_delay Configuration 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_delay1 Sets the value to be driven on the signal dfi_rdlvl_delay_x[63:32]

DDR_PCTL_DFITRRDLVLDELAY2
Address: Operational Base + offset (0x032c)
DFI Training dfi_rdlvl_delay Configuration 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	dfi_rdlvl_delay2 Sets the value to be driven on the signal dfi_rdlvl_delay_x[71:64]

DDR_PCTL_DFITRRDLVLGATEDELAY0
Address: Operational Base + offset (0x0330)
DFI Training dfi_rdlvl_gate_delay Configuration 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_gate_delay0 Sets the value to be driven on the signal dfi_rdlvl_gate_delay_x[31:0]

DDR_PCTL_DFITRRDLVLGATEDELAY1
Address: Operational Base + offset (0x0334)
DFI Training dfi_rdlvl_gate_delay Configuration 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_gate_delay1 Sets the value to be driven on the signal dfi_rdlvl_gate_delay_x[63:32]

DDR_PCTL_DFITRRDLVLGATEDELAY2
Address: Operational Base + offset (0x0338)
DFI Training dfi_rdlvl_gate_delay Configuration 2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	dfi_rdlvl_gate_delay2 Sets the value to be driven on the signal dfi_rdlvl_gate_delay_x[71:64]

DDR_PCTL_DFITRCMD
Address: Operational Base + offset (0x033c)
DFI Training Command Register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	dfitrcmd_start DFI Training Command Start. When this bit is set to 1, the command operation defined in the dfitrcmd_opcode field is started. This bit is automatically cleared by the uPCTL after the command is finished. The application can poll this bit to determine when uPCTL is ready to accept another command. This bit cannot be cleared to 1’b0 by software.
30:13	RO	0x0	reserved
12:4	RW	0x000	dfitrcmd_en DFI Training Command Enable. Selects which bits of chosen DFI Training command to drive to 1'b1.
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	dfitrcmd_opcode DFI Training Command Opcode. Select which DFI Training command to generate for one n_clk cycle: 2'b00: dfi_wrlvl_load 2'b01: dfi_wrlvl_strobe 2'b10: dfi_rdlvl_load 2'b11: Reserved.

DDR_PCTL_IPVR
Address: Operational Base + offset (0x03f8)
IP Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ip_version ASCII value for each number in the version, followed by a *.

DDR_PCTL_IPTR
Address: Operational Base + offset (0x03fc)
IP Type Register

Bit	Attr	Reset Value	Description
31:0	RO	0x44574300	ip_type Contains the IP's identification code, which is an ASCII value to identify the component and it is currently set to the string "DWC". This value never changes.

DDR_PUBL_RIDR
Address: Operational Base + offset (0x0000)
Revision Identification Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	UDRID User-Defined Revision ID General purpose revision identification set by the user
23:20	RO	0x1	PHYMJR PHY Major Revision Indicates major revision of the PHY such addition of the features that make the new version not compatible with previous versions

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	PHYMDR PHY Moderate Revision Indicates moderate revision of the PHY such as addition of new features. Normally the new version is still compatible with previous versions.
15:12	RO	0x0	PHYMNR PHY Minor Revision Indicates minor update of the PHY such as bug fixes. Normally no new features are included.
11:8	RO	0x1	PUBMJR PUB Major Revision Indicates major revision of the PUB such addition of the features that make the new version not compatible with previous versions.
7:4	RO	0x4	PUBMDR PUB Moderate Revision Indicates moderate revision of the PUB such as addition of new features. Normally the new version is still compatible with previous versions.
3:0	RO	0x0	PUBMNR PUB Minor Revision Indicates minor update of the PUB such as bug fixes. Normally no new features are included.

DDR_PUBL_PIR
Address: Operational Base + offset (0x0004)
PHY Initialization Register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	INITBYP Initialization Bypass Bypasses or stops, if set, all initialization routines currently running, including PHY initialization, DRAM initialization, and PHY training. Initialization may be triggered manually using INIT and the other relevant bits of the PIR register. This bit is self-clearing.
30	R/WSC	0x0	ZCALBYP Impedance Calibration Bypass Bypasses or stops, if set, impedance calibration of all ZQ control blocks that automatically triggers after reset. Impedance calibration may be triggered manually using INIT and ZCAL bits of the PIR register. This bit is self-clearing.

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Bit	Attr	Reset Value	Description
29	R/WSC	0x0	LOCKBYP DLL Lock Bypass Bypasses or stops, if set, the waiting of DLLs to lock. DLL lock wait is automatically triggers after reset. DLL lock wait may be triggered manually using INIT and DLLLOCK bits of the PIR register. This bit is self-clearing.
28	R/WSC	0x0	CLRSR Clear Status Registers A write of '1' to this bit will clear (reset to '0' all status registers, including PGSR and DXnGSR. The clear status register bit is self-clearing. This bit is primarily for debug purposes and is typically not needed during normal functional operation. It can be used when PGSR.IDONE=1, to manually clear the PGSR status bits, although starting a new init process will automatically clear the PGSR status bits. Or it can be used to manually clear the DXnGSR status bits, although starting a new data training process will automatically clear the DXnGSR status bits.
27:19	RO	0x0	reserved
18	RW	0x0	CTLDINIT Controller DRAM Initialization Indicates if set that DRAM initialization will be performed by the controller. Otherwise if not set it indicates that DRAM initialization will be performed using the built-in initialization sequence or using software through the configuration port.
17	RW	0x0	DLLBYP DLL Bypass A setting of 1 on this bit will put all PHY DLLs in bypass mode. A bypassed DLL is also powered down (disabled).

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Bit	Attr	Reset Value	Description
16	RW	0x0	ICPC Initialization Complete Pin Configuration Specifies how the DFI 2.1 initialization complete output pin should be used to indicate the status of initialization. Valid value are: 1'b0: Asserted after PHY initialization (DLL locking and impedance calibration) is complete. 1'b1: Asserted after PHY initialization is complete and the triggered the PUBL initialization (DRAM initialization, data training, or initialization trigger with no selected initialization) is complete.
15:9	RO	0x0	reserved
8	RW	0x0	RVTRN Read Valid Training Executes a PUB training routine to determine the optimum position of the read valid signal for maximum system timing margins.
7	RW	0x0	QSTRN Read DQS Training Executes a PUBL training routine to determine the optimum position of the read data DQS strobe for maximum system timing margins.
6	RW	0x0	DRAMINIT DRAM Initialization Executes the DRAM initialization sequence
5	RW	0x0	DRAMRST DRAM Reset (DDR3 Only) Issues a reset to the DRAM (by driving the DRAM reset pin low) and wait 200us. This can be triggered in isolation or with the full DRAM initialization (DRAMINIT). For the later case, the reset is issued and 200us is waited before starting the full initialization sequence.
4	RW	0x0	ITMSRST Interface Timing Module Soft Reset Soft resets the interface timing modules for the data and data strobes, i.e., it asserts the ITM soft reset (srstb) signal.
3	RW	0x0	ZCAL Impedance Calibrate Performs PHY impedance calibration
2	RW	0x0	DLLLOCK DLL Lock Waits for the PHY DLLs to lock

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Bit	Attr	Reset Value	Description
1	RW	0x0	DLLSRST DLL Soft Rest Soft resets all PHY DLLs by driving the DLL soft reset pin
0	RW	0x0	INIT Initialization Trigger A write of '1' to this bit triggers the DDR system initialization, including PHY initialization, DRAM initialization, and PHY training. The exact initialization steps to be executes are specified in bits 1 to 6 of this register. A bit setting of 1 means the step will be executed as part of the initialization sequence, while a setting of 0 means the step will be bypassed. The initialization trigger bit is self-clearing.

DDR_PUBL_PGCR
Address: Operational Base + offset (0x0008)
PHY General Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	LBMODE Loopback Mode Indicates if set that the PHY/PUB is in loopback mode
30	RW	0x0	LBGDQS Loopback DQS Gating Selects the DQS gating mode that should be used when the PHY is in loopback mode, including BIST loopback mode. Valid values are: 1'b0: DQS gate training will be triggered on the PUB 1'b1: DQS gate is set manually using software
29	RW	0x0	LBDQSS Loopback DQS Shift Selects how the read DQS is shifted during loopback to ensure that the read DQS is centered into the read data eye. Valid values are: 1'b0: PUB sets the read DQS delay to 0; DQS is already shifted 90 degrees by write path 1'b1: The read DQS shift is set manually through software

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Bit	Attr	Reset Value	Description
28:25	RW	0x0	RFSHDT Refresh During Training A non-zero value specifies that a burst of refreshes equal to the number specified in this field should be sent to the SDRAM after training each rank except the last rank.
24	RW	0x1	PDDISDX Power Down Disabled Byte Indicates if set that the DLL and I/Os of a disabled byte should be powered down
23:22	RW	0x2	ZCKSEL Impedance Clock Divider Select Selects the divide ratio for the clock used by the impedance control logic relative to the clock used by the memory controller and SDRAM. Valid values are: 2'b00: Divide by 2 2'b01: Divide by 8 2'b10: Divide by 32 2'b11: Divide by 64
21:18	RW	0xf	RANKEN Rank Enable Specifies the ranks that are enabled for data-training. Bit 0 controls rank 0, bit 1 controls rank 1, bit 2 controls rank 2, and bit 3 controls rank 3. Setting the bit to '0' enables the rank, and setting it to '1' disables the rank.
17:16	RW	0x0	IODDRM I/O DDR Mode (D3F I/O Only) Selects the DDR mode for the I/Os
15	RW	0x0	IOLB I/O Loop-Back Select Selects where inside the I/O the loop-back of signals happens. Valid values are: 1'b0: Loopback is after output buffer; output enable must be asserted 1'b1: Loopback is before output buffer; output enable is don't care
14	RW	0x0	CKINV CK Invert Specifies if set that CK/CK# should be inverted. Otherwise CK/CK# toggles with normal polarity.

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	CKDV CK Disable Value Specifies the static value that should be driven on CK/CK# pair(s) when the pair(s) is disabled. CKDV[0] specifies the value for CK and CKDV[1] specifies the value for CK#.
11:9	RW	0x7	CKEN CK Enable Controls whether the CK going to the SDRAM is enabled (toggling) or disabled (static value defined by CKDV). One bit for each of the three CK pairs.
8:5	RW	0x0	DTOSEL Digital Test Output Select Selects the PHY digital test output that should be driven onto PHY digital test output (phy_dto) pin: Valid values are: 4'b0000: DATX8 0 DLL digital test output 4'b0001: DATX8 1 DLL digital test output 4'b0010: DATX8 2 DLL digital test output 4'b0011: DATX8 3 DLL digital test output 4'b0100: DATX8 4 DLL digital test output 4'b0101: DATX8 5 DLL digital test output 4'b0110: DATX8 6 DLL digital test output 4'b0111: DATX8 7 DLL digital test output 4'b1000: DATX8 8 DLL digital test output 4'b1001: AC DLL digital test output 4'b1010, 4'b01111: Reserved
4:3	RW	0x0	DFTLMT DQS Drift Limit Specifies the expected limit of drift on read data strobes. A drift of this value or greater is reported as a drift error through the host port error flag. Valid values are: 2'b00: No limit (no error reported) 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg or more drift *Note: Although reported through the error flag, this is not an error requiring any action. It is simply an indicator that the drift is greater than expected.*

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Bit	Attr	Reset Value	Description
2	RW	0x1	DFTCMP DQS Drift Compensation Enables or disables DQS drift compensation. Valid values are: 1'b0: Disables data strobe drift compensation 1'b1: Enables data strobe drift compensation By default, drift compensation is enabled. *Note: Drift compensation must be disabled for LPDDR2.*
1	RW	0x0	DQSCFG DQS Gating Configuration Selects one of the two DQS gating schemes: 1'b0: DQS gating is shut off using the rising edge of DQS_b (active windowing mode) 1'b1: DQS gating blankets the whole burst (passive windowing mode) *Note: Passive windowing must be used for LPDDR2.*
0	RW	0x0	ITMDMD ITM DDR Mode Selects whether ITMS uses DQS and DQS# or it only uses DQS. Valid values are: 1'b0: ITMS uses DQS and DQS# 1'b1: ITMS uses DQS only *Note: The only valid value for DDR is 1*

DDR_PUBL_PGSR
Address: Operational Base + offset (0x000c)
PHY General Status Register

Bit	Attr	Reset Value	Description
31	RO	0x0	TQ Temperature Output (LPDDR Only) Connected to the DRAM TQ pin which is defined to go high when the LPDDR device temperature equals to or exceeds 85C, otherwise it is low.
30:10	RO	0x0	reserved
9	RO	0x0	RVEIRR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training, such as a pass was followed by a fail then followed by another pass.

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Bit	Attr	Reset Value	Description
8	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training.
7	RO	0x0	DFTERR DQS Drift Error If set, indicates that at least one of the read data strobes has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR).
6	RO	0x0	DTIERR Data Training Intermittent Error If set, indicates that there was an intermittent error during data training, such as a pass was followed by a fail then followed by another pass.
5	RO	0x0	DTERR Data Training Error If set, indicates that a valid DQS gating window could not be found during data training.
4	RO	0x0	DTDONE Data Training Done Indicates, if set, that the PHY has finished doing data training
3	RO	0x0	DIDONE DRAM Initialization Done Indicates if set that DRAM initialization has completed
2	RO	0x0	ZCDONE Impedance Calibration Done Indicates if set that impedance calibration has completed
1	RO	0x0	DLDONE DLL Lock Done Indicates if set that DLL locking has completed
0	RO	0x0	IDONE Initialization Done Indicates if set that the DDR system initialization has completed. This bit is set after all the selected initialization routines in PIR register have completed.

DDR_PUBL_DLLGCR
Address: Operational Base + offset (0x0010)
DLL General Control Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	LOCKDET Master lock detector enable.
28	RO	0x0	reserved
27:20	RW	0x37	SBIAS Slave Bias Trim Used to trim the bias for the slave DLL
19:12	RW	0x37	MBIAS Master Bias Trim Used to trim the bias for the master DLL
11	RW	0x0	TESTSW Test Switch Selects the test signals of either the master DLL ('0') or the slave DLL ('1')
10:9	RW	0x0	ATC Analog Test Control Selects the analog signal to be output on the DLL analog test output (test_out_a) when TESTEN is high (Output is Vss when TESTEN is low). The test output either comes from the master DLL or the slave DLL, depending on the setting of the test switch (TESTSW). Both master DLL and slave DLL output similar analog test signals. Valid settings for analog test control are: 2'b00: Filter output (Vc) 2'b01: Replica bias output for NMOS (Vbn) 2'b10: Replica bias output for PMOS (Vbp) 2'b11: Vdd 00

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Bit	Attr	Reset Value	Description
8:6	RW	0x0	DTC Digital Test Control Selects the digital signal to be output on the DLL digital test output (test_out_d[1]) when TESTEN is high (Output is '0' when TESTEN is low). Valid settings for master DLL (such as, when TESTSW = '0'): 3'b000: 0 output clock (clk_0) 3'b001: 90 output clock (clk_90) 3'b010: 180 output clock (clk_180) 3'b011: 270 output clock (clk_270) 3'b100: 360 internal clock (clk_360_int) 3'b101: Speed-up pulse (spdup) 3'b110: Slow-down pulse (slwdn) 3'b111: 0 MCTL logic clock (cclk_0) Valid settings for slave DLL (such as when TESTSW = '1'): 3'b000: Input DQS strobe (dqs) 3'b001: Input clock reference (clk_90_in) 3'b010: Internal feedback clock (clk_0_out) 3'b011: 90 output DQS_b strobe (dqsb_90) 3'b100: 90 output DQS strobe (dqs_90) 3'b101: Speed-up pulse (spdup) 3'b110: Slow-down pulse (slwdn) 3'b111: Auto-lock enable signal
5	RW	0x0	TESTEN Test Enable Enables digital and analog test outputs selected by DTC and ATC respectively
4:2	RW	0x0	IPUMP Charge Pump Current Trim Used to trim charge pump current: 3'b000: maximum current 3'b111: minimum current
1:0	RW	0x0	DRES Delta Resistor Trim Used to trim reference current versus resistor value variation: 2'b00: Rnom 2'b01: Rnom - 20% 2'b1x: Rnom + 20%

DDR_PUBL_ACDLLCR
Address: Operational Base + offset (0x0014)

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AC DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the AC DLL by driving the DLL soft reset pin
29:19	RO	0x0	reserved
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.
17:12	RO	0x0	Reserved
11:9	RW	0x0	MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay
5:0	RO	0x0	Reserved

DDR_PUBL_PTR0
Address: Operational Base + offset (0x0018)
PHY Timing Register 0

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:18	RW	0x8	tITMSRST ITM Soft Reset Time Number of controller clock cycles that the ITM soft reset pin must remain asserted when the soft reset is applied to the ITMs. This must correspond to a value that is equal to or more than 8 controller clock cycles. Default value corresponds to 8 controller clock cycles.

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Bit	Attr	Reset Value	Description
17:6	RW	0xabe	tDLLLOCK DLL Lock Time Number of clock cycles for the DLL to stabilize and lock, i.e. number of clock cycles from when the DLL reset pin is de-asserted to when the DLL has locked and is ready for use. Refer to the PHY databook for the DLL lock time. Default value corresponds to 5.12us at 533MHz.
5:0	RW	0x1b	tDLLSRST DLL Soft Reset Time Number of controller clock cycles that the DLL soft reset pin must remain asserted when the soft reset is triggered through the PHY Initialization Register (PIR). This must correspond to a value that is equal to or more than 50ns or 8 controller clock cycles, whichever is bigger. Default value corresponds to 50ns at 533MHz.

DDR_PUBL_PTR1
Address: Operational Base + offset (0x001c)
PHY Timing Register 1

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:19	RW	0xc0	tDINIT1 DRAM Initialization Time 1 DRAM initialization time corresponding to the following: DDR3: CKE high time to first command (tRFC +10 ns or 5 tCK, whichever value is larger) DDR2: CKE high time to first command (400 ns) DDR: CKE high time to first command (400 ns or 1 tCK) LPDDR2: CKE low time with power and clock stable (100 ns) Default value corresponds to DDR3 360ns at 533MHz.

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Bit	Attr	Reset Value	Description
18:0	RW	0x4111d	tDINIT0 DRAM Initialization Time 0 DRAM initialization time corresponding to the following: DDR3: CKE low time with power and clock stable (500 us) DDR2: CKE low time with power and clock stable (200 us) DDR: CKE low time with power and clock stable (200 us) LPDDR: CKE high time to first command (200 us) LPDDR2: CKE high time to first command (200 us) Default value corresponds to DDR3 500 us at 533MHz.

DDR_PUBL_PTR2
Address: Operational Base + offset (0x0020)
PHY Timing Register 2

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:17	RW	0x216	tDINIT3 DRAM Initialization Time 3 DRAM initialization time corresponding to the following: LPDDR2: Time from ZQ initialization command to first command (1 us) Default value corresponds to the LPDDR2 1 us at 533MHz.
16:0	RW	0x1a072	tDINIT2 DRAM Initialization Time 2 DRAM initialization time corresponding to the following: DDR3: Reset low time (200 us on power-up or 100 ns after power-up) LPDDR2: Time from reset command to end of auto initialization (1 us + 10 us = 11 us) Default value corresponds to DDR3 200 us at 533MHz.

DDR_PUBL_ACIOCR
Address: Operational Base + offset (0x0024)
AC I/O Configuration Register

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	ACSR Address/Command Slew Rate (D3F I/O Only) Selects slew rate of the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
29	RW	0x1	RSTIOM SDRAM Reset I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for SDRAM Reset
28	RW	0x1	RSTPDR SDRAM Reset Power Down Receiver Powers down, when set, the input receiver on the I/O for SDRAM RST# pin
27	RW	0x0	RSTPDD SDRAM Reset Power Down Driver Powers down, when set, the output driver on the I/O for SDRAM RST# pin
26	RW	0x0	RSTODT SDRAM Reset On-Die Termination Enables, when set, the on-die termination on the I/O for SDRAM RST# pin
25:22	RW	0xf	RANKPDR Rank Power Down Receiver Powers down, when set, the input receiver on the I/O CKE[3:0], ODT[3:0], and CS#[3:0] pins. RANKPDR[0] controls the power down for CKE[0], ODT[0], and CS#[0], RANKPDR[1] controls the power down for CKE[1], ODT[1], and CS#[1], and so on.
21:18	RW	0x0	CSPDD CS# Power Down Driver Powers down, when set, the output driver on the I/O for CS#[3:0] pins. PDD[0] controls the power down for CS#[0], PDD[1] controls the power down for CS#[1], and so on. CKE and ODT driver power down is controlled by DSGCR register.
17:14	RW	0x0	RANKODT Rank On-Die Termination Enables, when set, the on-die termination on the I/O for CKE[3:0], ODT[3:0], and CS#[3:0] pins. RANKODT[0] controls the on-die termination for CKE[0], ODT[0], and CS#[0], RANKODT[1] controls the on-die termination for CKE[1], ODT[1], and CS#[1], and so on.

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Bit	Attr	Reset Value	Description
13:11	RW	0x7	CKPDR CK Power Down Receiver Powers down, when set, the input receiver on the I/O for CK[0], CK[1], and CK[2] pins, respectively
10:8	RW	0x0	CKPDD CK Power Down Driver Powers down, when set, the output driver on the I/O for CK[0], CK[1], and CK[2] pins, respectively
7:5	RW	0x0	CKODT CK On-Die Termination Enables, when set, the on-die termination on the I/O for CK[0], CK[1], and CK[2] pins, respectively
4	RW	0x1	ACPDR AC Power Down Receiver Powers down, when set, the input receiver on the I/O for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
3	RW	0x0	ACPDD AC Power Down Driver Powers down, when set, the output driver on the I/O for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
2	RW	0x0	ACODT Address/Command On-Die Termination Enables, when set, the on-die termination on the I/O for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
1	RW	0x1	ACOE Address/Command Output Enable Enables, when set, the output driver on the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
0	RW	0x0	ACIOM Address/Command I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.

DDR_PUBL_DXCCR
Address: Operational Base + offset (0x0028)

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DATX8 Common Configuration Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	AWDT Active Window Data Train Indicates if set that data training (DQS gate training and read valid training) should be performed with active DQS gate window. This is just for debug purposes. The default is to perform training with passive windowing.
15	RW	0x0	RVSEL ITMD Read Valid Select Selects the scheme used for ITMD read valid. Valid values are: 1'b0: ITMD read valid signal is generated by delayed DFI read enable signal. 1'b1: ITMD read valid is generated by the ITMD itseld using asynchronous crossing.
14	RO	0x0	reserved
13:12	RW	0x0	DXSR Data Slew Rate (D3F I/O Only) Selects slew rate of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros.
11:8	RW	0x8	DQSNRES DQS# Resistor Selects the on-die pull-up/pull-down resistor for DQS# pins. Same encoding as DQSRES. *Note: DQS# resistor must be connected for LPDDR2*
7:4	RW	0x0	DQSRES DQS Resistor Selects the on-die pull-down/pull-up resistor for DQS pins. DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1). DQSRES[2:0] selects the resistor value as follows: 3'b000: Open: On-die resistor disconnected 3'b001: 688 ohms 3'b010: 611 ohms 3'b011: 550 ohms 3'b100: 500 ohms 3'b101: 458 ohms 3'b110: 393 ohms 3'b111: 344 ohms *Note: DQS resistor must be connected for LPDDR2*

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Bit	Attr	Reset Value	Description
3	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDR configuration bit of the individual DATX8.
2	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDD configuration bit of the individual DATX8.
1	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the IOM configuration bit of the individual DATX8.
0	RW	0x0	DXODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8.

DDR_PUBL_DSGCR
Address: Operational Base + offset (0x002c)
DDR System General Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x1	CKEOE SDRAM CKE Output Enable Enables, when set, the output driver on the I/O for SDRAM CKE pins
30	RW	0x1	RSTOE SDRAM Reset Output Enable Enables, when set, the output driver on the I/O for SDRAM RST# pin
29	RW	0x1	ODTOE SDRAM ODT Output Enable Enables, when set, the output driver on the I/O for SDRAM ODT pins

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Bit	Attr	Reset Value	Description
28	RW	0x1	CKOE SDRAM CK Output Enable Enables, when set, the output driver on the I/O for SDRAM CK/CK# pins
27	RW	0x1	TPDOE SDRAM TPD Output Enable (LPDDR Only) Enables, when set, the output driver on the I/O for SDRAM TPD pin
26	RW	0x0	TPDPD DRAM TPD Power Down Driver (LPDDR Only) Powers down, when set, the output driver on the I/O for SDRAM TPD pin. Note that the power down of the receiver on the I/O for SDRAM TPD pin is controlled by ACIOCR[ACPDR] register bit.
25	RW	0x1	NL2OE Non-LPDDR2 Output Enable Enables, when set, the output driver on the I/O for non-LPDDR2 (ODT, RAS#, CAS#, WE#, and BA) pins. This may be used when a chip that is designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode. For these pins, the I/O output enable signal (OE) is an AND of this bit and the respective output enable bit in ACIOCR or DSGCR registers.
24	RW	0x0	NL2PD Non-LPDDR2 Power Down Powers down, when set, the output driver and the input receiver on the I/O for non-LPDDR2 (ODT, RAS#, CAS#, WE#, and BA) pins. This may be used when a chip that is designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode. For these pins, the I/O power down signal (PDD or PDR) is an OR of this bit and the respective power-down bit in ACIOCR register.
23:20	RW	0x0	ODTPDD ODT Power Down Driver Powers down, when set, the output driver on the I/O for ODT[3:0] pins. ODTPDD[0] controls the power down for ODT[0], ODTPDD[1] controls the power down for ODT[1], and so on.

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	CKEPDD CKE Power Down Driver Powers down, when set, the output driver on the I/O for CKE[3:0] pins. CKEPDD[0] controls the power down for CKE[0], CKEPDD[1] controls the power down for CKE[1], and so on.
15:13	RO	0x0	reserved
12	RW	0x0	FXDLAT Fixed Latency Specified whether all reads should be returned to the controller with a fixed read latency. Enabling fixed read latency increases the read latency. Valid values are: 1'b0: Disable fixed read latency 1'b1: Enable fixed read latency If the design is compiled for HDR mode, then either NOBUB or FXDLAT must be set to 1.
11	RW	0x0	NOBUB No Bubbles Specified whether reads should be returned to the controller with no bubbles. Enabling no-bubble reads increases the read latency. Valid values are: 1'b0: Bubbles are allowed during reads 1'b1: Bubbles are not allowed during reads If the design is compiled for HDR mode, then either NOBUB or FXDLAT must be set to 1.
10:8	RW	0x0	DQSGE DQS Gate Early Specifies the number of clock cycles for which the DQS gating must be enabled earlier than its normal position. Only applicable when using PDQSR I/O cell, passive DQS gating and no drift compensation. This field is recommended to be set to zero for all DDR types other than LPDDR2. For LPDDR2 it should be set to (tDQSCKmax - tDQSCK) divide by clock period and rounded up.

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	DQSGX DQS Gate Extension Specifies the number of clock cycles for which the DQS gating must be extended beyond the normal burst length width. Only applicable when using PDQSR I/O cell, passive DQS gating and no drift compensation. This field is recommended to be set to zero for all DDR types other than LPDDR2. For LPDDR2 it should be set to (tDQSCKmax - tDQSCK) divide by clock period and rounded up.
4	RW	0x1	LPDLLPD Low Power DLL Power Down Specifies if set that the PHY should respond to the DFI low power opportunity request and power down the DLL of the byte if the wakeup time request satisfies the DLL lock time.
3	RW	0x1	LPIOPD Low Power I/O Power Down Specifies if set that the PHY should respond to the DFI low power opportunity request and power down the I/Os of the byte.
2	RW	0x1	ZUEN Impedance Update Enable Specifies if set that the PHY should perform impedance calibration (update) whenever there is a controller initiated DFI update request. Otherwise the PHY will ignore an update request from the controller.
1	RW	0x1	BDISEN Byte Disable Enable Specifies if set that the PHY should respond to DFI byte disable request. Otherwise the byte disable from the DFI is ignored in which case bytes can only be disabled using the DXnGCR register.
0	RW	0x1	PUREN PHY Update Request Enable Specifies if set, that the PHY should issue PHY-initiated DFI update request when there is DQS drift of more than 3/4 of a clock cycle within one continuous (back-to-back) read burst. By default the PHY issues PHY-initiated update requests and the controller should respond otherwise the PHY may return erroneous values. The option to disable it is provided only for silicon evaluation and testing.

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DDR_PUBL_DCR
Address: Operational Base + offset (0x0030)
DRAM Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	TPD Test Power Down (LPDDR Only) If set will place the DRAM in deep power down mode
30:29	RO	0x0	reserved
28	RW	0x0	DDR2T DDR 2T Timing Indicates if set that 2T timing should be used by PUB internally generated SDRAM transactions.
27	RW	0x0	NOSRA No Simultaneous Rank Access Specifies if set that simultaneous rank access on the same clock cycle is not allowed. This means that multiple chip select signals should not be asserted at the same time. This may be required on some DIMM systems.
26:10	RO	0x0	reserved
9:8	RW	0x0	DDRTYPE DDR Type Selects the DDR type for the specified DDR mode. Valid values for LPDDR2 are: 2'b00: LPDDR2-S4 2'b01: LPDDR2-S2 2'b10: LPDDR2-NVM 2'b11: Reserved
7	RW	0x0	MPRDQ Multi-Purpose Register (MPR) DQ (DDR3 Only) Specifies the value that is driven on non-primary DQ pins during MPR reads. Valid values are: 1'b0: Primary DQ drives out the data from MPR (0-1-0-1); non-primary DQs drive '0' 1'b1: Primary DQ and non-primary DQs all drive the same data from MPR (0-1-0-1)
6:4	RW	0x0	PDQ Primary DQ (DDR3 Only) Specifies the DQ pin in a byte that is designated as a primary pin for Multi-Purpose Register (MPR) reads. Valid values are 0 to 7 for DQ[0] to DQ[7], respectively.

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Bit	Attr	Reset Value	Description
3	RW	0x1	DDR8BNK DDR 8-Bank Indicates if set that the SDRAM used has 8 banks. tRPA = tRP+1 and tFAW are used for 8-bank DRAMs, other tRPA = tRP and no tFAW is used. Note that a setting of 1 for DRAMs that have fewer than 8 banks still results in correct functionality but less tighter DRAM command spacing for the parameters described here.
2:0	RW	0x3	DDRMD DDR Mode SDRAM DDR mode. Valid values are: 3'b000: LPDDR (Mobile DDR) 3'b001: DDR 3'b010: DDR2 3'b011: DDR3 3'b100: LPDDR2 (Mobile DDR2) 3'b101, 3'b111: Reserved

DDR_PUBL_DTPR0
Address: Operational Base + offset (0x0034)
DRAM Timing Parameters Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	tCCD Read to read and write to write command delay. Valid values are: 1'b0: BL/2 for DDR2 and 4 for DDR3 1'b1: BL/2 + 1 for DDR2 and 5 for DDR3
30:25	RW	0x18	tRC Activate to activate command delay (same bank). Valid values are 2 to 42.
24:21	RW	0x4	tRRD Activate to activate command delay (different banks). Valid values are 1 to 8.
20:16	RW	0x12	tRAS Activate to precharge command delay. Valid values are 2 to 31.
15:12	RW	0x6	tRCD Activate to read or write delay. Minimum time from when an activate command is issued to when a read or write to the activated row can be issued. Valid values are 2 to 11.

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Bit	Attr	Reset Value	Description
11:8	RW	0x6	tRP Precharge command period The minimum time between a precharge command and any other command. Note that the Controller automatically derives tRPA for 8-bank DDR2 devices by adding 1 to tRP . Valid values are 2 to 11.
7:5	RW	0x3	tWTR Internal write to read command delay. Valid values are 1 to 6.
4:2	RW	0x3	tRTP Internal read to precharge command delay. Valid values are 2 to 6. Note that even though RTP does not apply to JEDEC DDR devices, this parameter must still be set to a minimum value of 2 for DDR because the Controller always uses the DDR2 equation, AL + BL/2 + max(RTP,2) - 2, to compute the read to precharge timing (which is BL/2 for JEDEC DDR).
1:0	RW	0x2	tMRD Load mode cycle time The minimum time between a load mode register command and any other command. For DDR3 this is the minimum time between two load mode register commands. Valid values for DDR2 are 2 to 3. For DDR3, the value used for tMRD is 4 plus the value programmed in these bits, i.e. tMRD value for DDR3 ranges from 4 to 7.

DDR_PUBL_DTPR1
Address: Operational Base + offset (0x0038)
DRAM Timing Parameters Register 1

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x1	tDQSCKmax Maximum DQS output access time from CK/CK# (LPDDR2 only). This value is used for implementing read-to-write spacing. Valid values are 1 to 7.

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Bit	Attr	Reset Value	Description
26:24	RW	0x1	tDQSCK DQS output access time from CK/CK# (LPDDR2 only). This value is used for computing the read latency. Valid values are 1 to 7.. This value is derived from the corresponding parameter in the SDRAM datasheet divided by the clock cycle time without rounding up. The fractional remainder is automatically adjusted for by data training in quarter clock cycle units. If data training is not performed then this fractional remainder must be converted to quarter clock cycle units and the gating registers (DXnDQSTR) adjusted accordingly.
23:16	RW	0x83	tRFC Refresh-to-Refresh: Indicates the minimum time, in clock cycles, between two refresh commands or between a refresh and an active command. This is derived from the minimum refresh interval from the datasheet, tRFC(min), divided by the clock cycle time. The default number of clock cycles is for the largest JEDEC tRFC(min) parameter value supported.
15:12	RO	0x0	reserved
11	RW	0x0	tRTODT Read to ODT delay (DDR3 only). Specifies whether ODT can be enabled immediately after the read post-amble or one clock delay has to be added. Valid values are: 1'b0: ODT may be turned on immediately after read post-amble 1'b1: ODT may not be turned on until one clock after the read post-amble If tRTODT is set to 1, then the read-to-write latency is increased by 1 if ODT is enabled.
10:9	RW	0x0	tMOD Load mode update delay (DDR3 only). The minimum time between a load mode register command and a non-load mode register command. Valid values are: 2'b00: 12 2'b01: 13 2'b10: 14 2'b11: 15

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Bit	Attr	Reset Value	Description
8:3	RW	0x12	tFAW 4-bank activate period. No more than 4-bank activate commands may be issued in a given tFAW period. Only applies to 8-bank devices. Valid values are 2 to 31.
2	RW	0x0	tRTW Read to Write command delay. Valid values are: 1'b0: standard bus turn around delay 1'b1: add 1 clock to standard bus turn around delay This parameter allows the user to increase the delay between issuing Write commands to the SDRAM when preceded by Read commands. This provides an option to increase bus turn-around margin for high frequency systems.
1:0	RW	0x0	tAOND_tAOFD ODT turn-on/turn-off delays (DDR2 only). The delays are in clock cycles. Valid values are: 2'b00: 2/2.5 2'b01: 3/3.5 2'b10: 4/4.5 2'b11: 5/5.5 Most DDR2 devices utilize a fixed value of 2/2.5. For non-standard SDRAMs, the user must ensure that the operational Write Latency is always greater than or equal to the ODT turn-on delay. For example, a DDR2 SDRAM with CAS latency set to 3 and CAS additive latency set to 0 has a Write Latency of 2. Thus 2/2.5 can be used, but not 3/3.5 or higher.

DDR_PUBL_DTPR2
Address: Operational Base + offset (0x003c)
DRAM Timing Parameters Register 2

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:19	RW	0x200	tDLLK DLL locking time. Valid values are 2 to 1023.
18:15	RW	0x3	tCKE CKE minimum pulse width. Also specifies the minimum time that the SDRAM must remain in power down or self refresh mode. For DDR3 this parameter must be set to the value of tCKESR which is usually bigger than the value of tCKE. Valid values are 2 to 15.

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Bit	Attr	Reset Value	Description
14:10	RW	0x08	tXP Power down exit delay. The minimum time between a power down exit command and any other command. This parameter must be set to the maximum of the various minimum power down exit delay parameters specified in the SDRAM datasheet, i.e. max(tXP , tXARD, tXARDS) for DDR2 and max(tXP , tXPDLL) for DDR3. Valid values are 2 to 31.
9:0	RW	0x0c8	tXS Self refresh exit delay. The minimum time between a self refresh exit command and any other command. This parameter must be set to the maximum of the various minimum self refresh exit delay parameters specified in the SDRAM datasheet, i.e. max(tXSNR, tXSRD) for DDR2 and max(tXS, tXSDLL) for DDR3. Valid values are 2 to 1023.

DDR_PUBL_MR0
Address: Operational Base + offset (0x0040)
Mode Register 0

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	PD Power-Down Control Controls the exit time for power-down modes. Refer to SDRAM datasheet for details on power-down modes. Valid values are: 1'b0: Slow exit (DLL off) 1'b1: Fast exit (DLL on)

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Bit	Attr	Reset Value	Description
11:9	RW	0x5	WR Write Recovery This is the value of the write recovery in clock cycles. It is calculated by dividing the datasheet write recovery time, tWR (ns) by the datasheet clock cycle time, tCK (ns) and rounding up a non-integer value to the next integer. Valid values are: 3'b001: 5 3'b010: 6 3'b011: 7 3'b100: 8 3'b101: 10 3'b110: 12 All other settings are reserved and should not be used. *NOTE: tWR (ns) is the time from the first SDRAM positive clock edge after the last data-in pair of a write command, to when a precharge of the same bank can be issued.*
8	RW	0x0	DR DLL Reset Writing a '1' to this bit will reset the SDRAM DLL. This bit is self-clearing, i.e. it returns back to '0' after the DLL reset has been issued.
7	RW	0x0	TM Operating Mode Selects either normal operating mode (0) or test mode (1). Test mode is reserved for the manufacturer and should not be used.
6:4	RW	0x5	CL_1 CAS Latency The delay, in clock cycles, between when the SDRAM registers a read command to when data is available. Valid values are: 4'b0010: 5 4'b0100: 6 4'b0110: 7 4'b1000: 8 4'b1010: 9 4'b1100: 10 4'b1110: 11 All other settings are reserved and should not be used.

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Bit	Attr	Reset Value	Description
3	RW	0x0	BT Burst Type Indicates whether a burst is sequential (0) or interleaved (1).
2	RW	0x0	CL_0 CAS Latency merged with bit6-4
1:0	RW	0x2	BL Burst Length Determines the maximum number of column locations that can be accessed during a given read or write command. Valid values for DDR3 are: 2'b00: 8 (Fixed) 2'b01: 4 or 8 (On the fly) 2'b10: 4 (Fixed) 2'b11: Reserved

DDR_PUBL_MR1
Address: Operational Base + offset (0x0044)
Mode Register 1

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	QOFF Output Enable/Disable When '0' all outputs function normal; when '1' all SDRAM outputs are disabled removing output buffer current. This feature is intended to be used for IDD characterization of read current and should not be used in normal operation.
11	RW	0x0	TDQS Termination Data Strobe When enabled ('1') TDQS provides additional termination resistance outputs that may be useful in some system configurations. Refer to the SDRAM datasheet for details.
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	RTT_2 On Die Termination Selects the effective resistance for SDRAM on die termination. Valid values are: 3'b000: ODT disabled 3'b001: RZQ/4 3'b010: RZQ/2 3'b011: RZQ/6 3'b100: RZQ/12 3'b101: RZQ/8 All other settings are reserved and should not be used.
8	RO	0x0	reserved
7	RW	0x0	LEVEL Write Leveling Enable Enables write-leveling when set
6	RW	0x0	RTT_1 On Die Termination merged with bit9.
5	RW	0x0	DIC_1 Output Driver Impedance Control Controls the output drive strength. Valid values are: 2'b00: Reserved for RZQ/6 2'b01: RZQ7 2'b10: Reserved 2'b11: Reserved
4:3	RW	0x0	AL Posted CAS Additive Latency Setting additive latency that allows read and write commands to be issued to the SDRAM earlier than normal (refer to SDRAM datasheet for details). Valid values are: 2'b00: 0 (AL disabled) 2'b01: CL - 1 2'b10: CL - 2 2'b11: Reserved
2	RW	0x0	RTT_0 On Die Termination merged with bit9.
1	RW	0x0	DIC_0 Output Driver Impedance Control Controls the output drive strength. Merged with bit5.

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Bit	Attr	Reset Value	Description
0	RW	0x0	DE DLL Enable/Disable Enable (0) or disable (1) the DLL. DLL must be enabled for normal operation.

DDR_PUBL_MR2
Address: Operational Base + offset (0x0048)
Mode Register 2

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:9	RW	0x0	RTTWR Dynamic ODT Selects RTT for dynamic ODT. Valid values are: 2'b00: Dynamic ODT off 2'b01: RZQ/4 2'b10: RZQ/2 2'b11: Reserved
8	RO	0x0	reserved
7	RW	0x0	SRT Self-Refresh Temperature Range Selects either normal ('0') or extended ('1') operating temperature range during self-refresh.
6	RW	0x0	ASR Auto Self-Refresh When enabled ('1'), SDRAM automatically provides self-refresh power management functions for all supported operating temperature values. Otherwise the SRT bit must be programmed to indicate the temperature range.
5:3	RW	0x0	CWL CAS Write Latency The delay, in clock cycles, between when the SDRAM registers a write command to when write data is available. Valid values are: 3'b000: 5 (tCK = 2.5ns) 3'b001: 6 (2.5ns > tCK = 1.875ns) 3'b010: 7 (1.875ns > tCK = 1.5ns) 3'b011: 8 (1.5ns > tCK = 1.25ns) All other settings are reserved and should not be used

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	PASR Partial Array Self Refresh Specifies that data located in areas of the array beyond the specified location will be lost if self refresh is entered. Valid settings for 4 banks are: 3'b000: Full Array 3'b001: Half Array (BA[1:0] = 00 & 01) 3'b010: Quarter Array (BA[1:0] = 00) 3'b011: Not defined 3'b100: 3/4 Array (BA[1:0] = 01, 10, & 11) 3'b101: Half Array (BA[1:0] = 10 & 11) 3'b110: Quarter Array (BA[1:0] = 11) 3'b111: Not defined Valid settings for 8 banks are: 3'b000: Full Array 3'b001: Half Array (BA[2:0] = 000, 001, 010 & 011) 3'b010: Quarter Array (BA[2:0] = 000, 001) 3'b011: 1/8 Array (BA[2:0] = 000) 3'b100: 3/4 Array (BA[2:0] = 010, 011, 100, 101, 110 & 111) 3'b101: Half Array (BA[2:0] = 100, 101, 110 & 111) 3'b110: Quarter Array (BA[2:0] = 110 & 111) 3'b111: 1/8 Array (BA[2:0] 111)

DDR_PUBL_MR3
Address: Operational Base + offset (0x004c)
Mode Register 3

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	MPR Multi-Purpose Register Enable Enables, if set, that read data should come from the Multi-Purpose Register. Otherwise read data come from the DRAM array.
1:0	RW	0x0	MPRLOC Multi-Purpose Register (MPR) Location Selects MPR data location: Valid value are: 2'b00: Predefined pattern for system calibration All other settings are reserved and should not be used.

DDR_PUBL_ODTCR

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Address: Operational Base + offset (0x0050)
ODT Configuration Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x2	WRODT1 Write ODT Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a write command is sent to rank 0. WRODT0, WRODT1 specify ODT settings when a write is to rank 0, rank 1 respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to enable ODT only on rank being written to.
19:16	RW	0x1	WRODT0 Write ODT Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a write command is sent to rank 0. WRODT0, WRODT1 specify ODT settings when a write is to rank 0, rank 1 respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to enable ODT only on rank being written to.
15:8	RO	0x0	reserved
7:4	RW	0x0	RDODT1 Read ODT Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a read command is sent to rank 1. RDODT0, RDODT1 specify ODT settings when a read is to rank 0, and rank 1, respectively. The two bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to disable ODT during reads.
3:0	RW	0x0	RDODT0 Read ODT Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a read command is sent to rank 0. RDODT0, RDODT1 specify ODT settings when a read is to rank 0, and rank 1, respectively. The two bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to disable ODT during reads.

DDR_PUBL_DTAR

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Address: Operational Base + offset (0x0054)
Data Training Address Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DTMPR Data Training Using MPR (DDR3 Only) Specifies, if set, that data-training should use the SDRAM Multi-Purpose Register (MPR) register. Otherwise data-training is performed by first writing to some locations in the SDRAM and then reading them back.
30:28	RW	0x0	DTBANK Data Training Bank Address Selects the SDRAM bank address to be used during data training
27:12	RW	0x0000	DTROW Data Training Row Address Selects the SDRAM row address to be used during data training
11:0	RW	0x000	DTCOL Data Training Column Address Selects the SDRAM column address to be used during data training. The lower four bits of this address must always be "0000"

DDR_PUBL_DTDR0
Address: Operational Base + offset (0x0058)
Data Training Data Register 0

Bit	Attr	Reset Value	Description
31:24	RW	0xdd	DTBYTE3 Data Training Data The fourth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
23:16	RW	0x22	DTBYTE2 Data Training Data The third 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.

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Bit	Attr	Reset Value	Description
15:8	RW	0xee	DTBYTE1 Data Training Data The second 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
7:0	RW	0x11	DTBYTE0 Data Training Data The first 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.

DDR_PUBL_DTDR1
Address: Operational Base + offset (0x005c)
Data Training Data Register 1

Bit	Attr	Reset Value	Description
31:24	RW	0x77	DTBYTE7 Data Training Data The eighth4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
23:16	RW	0x88	DTBYTE6 Data Training Data The seventh 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
15:8	RW	0xbb	DTBYTE5 Data Training Data The sixth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
7:0	RW	0x44	DTBYTE4 Data Training Data The fifth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.

DDR_PUBL_DCUAR

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Address: Operational Base + offset (0x00c0)
DCU Address Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	ATYPE Access Type Specifies the type of access to be performed using this address. Valid values are: 1'b0: Write access 1'b1: Read access
10	RW	0x0	INCA Increment Address Specifies, if set, that the cache address specified in WADDR and SADDR should be automatically incremented after each access of the cache. The increment happens in such a way that all the slices of a selected word are first accessed before going to the next word.
9:8	RW	0x0	CSEL Cache Select Selects the cache to be accessed. Valid values are: 2'b00: Command cache 2'b01: Expected data cache 2'b10: Read data cache 2'b11: Reserved
7:4	RW	0x0	CSADDR Cache Slice Address Address of the cache slice to be accessed
3:0	RW	0x0	CWADDR Cache Word Address Address of the cache word to be accessed

DDR_PUBL_DCUDR
Address: Operational Base + offset (0x00c4)
DCU Data Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CDATA Cache Data Data to be written to or read from a cache. This data corresponds to the cache word slice specified by the DCU Address Register.

DDR_PUBL_DCURR
Address: Operational Base + offset (0x00c8)
DCU Run Register

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Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	XCEN Expected Compare Enable Indicates if set that read data coming back from the SDRAM should be should be compared with the expected data
22	RW	0x0	RCEN Read Capture Enable Indicates if set that read data coming back from the SDRAM should be captured into the read data cache
21	RW	0x0	SCOF Stop Capture On Full Specifies if set that the capture of read data should stop when the capture cache is full
20	RW	0x0	SONF Stop On Nth Fail Specifies if set that the execution of commands and the capture of read data should stop when there are N read data failures. The number of failures is specified by NFAIL. Otherwise commands execute until the end of the program or until manually stopped using a STOP command.
19:12	RW	0x00	NFAIL Number of Failures Specifies the number of failures after which the execution of commands and the capture of read data should stop if SONF bit of this register is set. Execution of commands and the capture of read data will stop after (NFAIL+1) failures if SONF is set.
11:8	RW	0x0	EADDR End Address Cache word address where the execution of command should end
7:4	RW	0x0	SADDR Start Address Cache word address where the execution of commands should begin

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	DINST DCU Instruction Selects the DCU command to be executed: Valid values are: 4'b0000: NOP: No operation 4'b0001: Run: Triggers the execution of commands in the command cache. 4'b0010: Stop: Stops the execution of commands in the command cache. 4'b0011: Stop Loop: Stops the execution of an infinite loop in the command cache. 4'b0100: Reset: Resets all DCU run time registers. 4'b0101 - 4'b1111: Reserved

DDR_PUBL_DCULR
Address: Operational Base + offset (0x00cc)
DCU Loop Register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	XLEADDR Expected Data Loop End Address The last expected data cache word address that contains valid expected data. Expected data should looped between 0 and this address.
27:18	RO	0x0	reserved
17	RW	0x0	IDA Increment DRAM Address Indicates if set that DRAM addresses should be incremented every time a DRAM read/write command inside the loop is executed
16	RW	0x0	LINF Loop Infinite Indicates if set that the loop should be executed indefinitely until stopped by the STOP command. Otherwise the loop is execute LCNT times.
15:8	RW	0x00	LCNT Loop Count The number of times that the loop should be executed if LINF is not set
7:4	RW	0x0	LEADDR Loop End Address Command cache word address where the loop should end

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	LSADDR Loop Start Address Command cache word address where the loop should start

DDR_PUBL_DCUGCR
Address: Operational Base + offset (0x00d0)
DCU General Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	RCSW Read Capture Start Word The capture and compare of read data should start after Nth word. For example setting this value to 12 will skip the first 12 read data.

DDR_PUBL_DCUTPR
Address: Operational Base + offset (0x00d4)
DCU Timing Parameters Registers

Bit	Attr	Reset Value	Description
31:24	RW	0x00	tDCUT3 DCU Generic Timing Parameter 3.
23:16	RW	0x00	tDCUT2 DCU Generic Timing Parameter 2.
15:8	RW	0x00	tDCUT1 DCU Generic Timing Parameter 1.
7:0	RW	0x00	tDCUT0 DCU Generic Timing Parameter 0.

DDR_PUBL_DCUSR0
Address: Operational Base + offset (0x00d8)
DCU Status Register 0

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	CFULL Capture Full Indicates if set that the capture cache is full

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Bit	Attr	Reset Value	Description
1	RO	0x0	CFAIL Capture Fail Indicates if set that at least one read data word has failed
0	RO	0x0	RDONE Run Done: Indicates if set that the DCU has finished executing the commands in the command cache. This bit is also set to indicate that a STOP command has successfully been executed and command execution has stopped.

DDR_PUBL_DCUSR1
Address: Operational Base + offset (0x00dc)
DCU Status Register 1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	LPCNT Loop Count Indicates the value of the loop count. This is useful when the program has stooped because of failures to assess how many reads were executed before first fail.
23:16	RO	0x00	FLCND Fail Count Number of read words that have failed
15:0	RO	0x0000	RDCNT Read Count Number of read words returned from the SDRAM

DDR_PUBL_BISTRR
Address: Operational Base + offset (0x0100)
BIST Run Register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25:23	RW	0x0	BCKSEL BIST CK Select Selects the CK to be used for capturing loopback data on the address/command lane. Valid values are: 3'b000: CK[0] 3'b001: CK[1] 3'b010: CK[2] 3'b011: Reserved 3'b100: CK#[0] 3'b101: CK#[1] 3'b110: CK#[2] 3'b111: Reserved
22:19	RW	0x0	BDXSEL BIST DATX8 Select Select the byte lane for comparison of loopback/read data. Valid values are 0 to 8.
18:17	RW	0x0	BDPAT BIST Data Pattern Selects the data pattern used during BIST. Valid values are: 2'b00: Walking 0 2'b01: Walking 1 2'b10: LFSR-based pseudo-random 2'b11: User programmable
16	RW	0x0	BDMEN BIST Data Mask Enable Enables if set that the data mask BIST should be included in the BIST run, i.e. data pattern generated and loopback data compared. This is valid only for loopback mode.
15	RW	0x0	BACEN BIST AC Enable Enables the running of BIST on the address/command lane PHY. This bit is exclusive with BDXEN, i.e. both cannot be set to '1' at the same time.
14	RW	0x0	BDXEN BIST DATX8 Enable Enables the running of BIST on the data byte lane PHYs. This bit is exclusive with BACEN, i.e. both cannot be set to '1' at the same time.

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Bit	Attr	Reset Value	Description
13	RW	0x0	BSONF BIST Stop On Nth Fail Specifies if set that the BIST should stop when an nth data word or address/command comparison error has been encountered.
12:5	RW	0x00	NFAIL Number of Failures Specifies the number of failures after which the execution of commands and the capture of read data should stop if BSONF bit of this register is set. Execution of commands and the capture of read data will stop after (NFAIL+1) failures if BSONF is set.
4	RW	0x0	BINF BIST Infinite Run Specifies if set that the BIST should be run indefinitely until when it is either stopped or a failure has been encountered. Otherwise BIST is run until number of BIST words specified in the BISTWCR register has been generated.
3	RW	0x0	BMODE BIST Mode Selects the mode in which BIST is run. Valid values are: 1'b0: Loopback mode: Address, commands and data loop back at the PHY I/Os. 1'b1: DRAM mode: Address, commands and data go to DRAM for normal memory accesses.
2:0	RW	0x0	BINST BIST Instruction Selects the BIST instruction to be executed: Valid values are: 3'b000: NOP: No operation 3'b001: Run: Triggers the running of the BIST. 3'b010: Stop: Stops the running of the BIST. 3'b011: Reset: Resets all BIST run-time registers, such as error counters. 3'b100 - 3'b111: Reserved

DDR_PUBL_BISTMSKR0
Address: Operational Base + offset (0x0104)
BIST Mask Register 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	ODTMSK Mask bit for each of the up to 4 ODT bits
27:24	RW	0x0	CSMSK Mask bit for each of the up to 4 CS# bits
23:20	RW	0x0	CKEMSK Mask bit for each of the up to 4 CKE bits
19	RW	0x0	WEMSK Mask bit for the WE#
18:16	RW	0x0	BAMSK Mask bit for each of the up to 3 bank address bits
15:0	RW	0x0000	AMSK Mask bit for each of the up to 16 address bits

DDR_PUBL_BISTMSKR1
Address: Operational Base + offset (0x0108)
BIST Mask Register 1

Bit	Attr	Reset Value	Description
31	RW	0x0	TPDMSK Mask bit for the TPD. LPDDR Only.
30	RW	0x0	PARMSK Mask bit for the PAR_IN. Only for DIMM parity support.
29:20	RO	0x0	reserved
19	RW	0x0	CASMSK Mask bit for the CAS
18	RW	0x0	RASMSK Mask bit for the RAS
17:16	RW	0x0	DMMSK Mask bit for the data mask (DM) bits
15:0	RW	0x0000	DQMSK Mask bit for each of the 8 data (DQ) bits

DDR_PUBL_BISTWCR
Address: Operational Base + offset (0x010c)
BIST Word Count Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0020	BWCNT BIST Word Count Indicates the number of words to generate during BIST. This must be a multiple of DRAM burst length (BL) divided by 2, e.g. for BL=8, valid values are 4, 8, 12, 16, and so on.

DDR_PUBL_BISTLSR
Address: Operational Base + offset (0x0110)
BIST LFSR Seed Register

Bit	Attr	Reset Value	Description
31:0	RW	0x1234abcd	SEED LFSR seed for pseudo-random BIST patterns.

DDR_PUBL_BISTAR0
Address: Operational Base + offset (0x0114)
BIST Address Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	BBANK BIST Bank Address Selects the SDRAM bank address to be used during BIST
27:12	RW	0x0000	BROW BIST Row Address Selects the SDRAM row address to be used during BIST
11:0	RW	0x000	BCOL BIST Column Address Selects the SDRAM column address to be used during BIST. The lower bits of this address must be "0000" for BL16, "000" for BL8, "00" for BL4 and "0" for BL2.

DDR_PUBL_BISTAR1
Address: Operational Base + offset (0x0118)
BIST Address Register 1

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:4	RW	0x000	BAINC BIST Address Increment Selects the value by which the SDRAM address is incremented for each write/read access. This value must be at the beginning of a burst boundary, i.e. the lower bits must be "0000" for BL16, "00" for BL8, "00" for BL4 and "0" for BL2.
3:2	RW	0x3	BMRANK BIST Maximum Rank Specifies the maximum SDRAM rank to be used during BIST. The default value is set to maximum ranks minus 1. Example default shown here is for a 4-rank system
1:0	RW	0x0	BRANK BIST Rank Selects the SDRAM rank to be used during BIST. Valid values range from 0 to maximum ranks minus 1.

DDR_PUBL_BISTAR2
Address: Operational Base + offset (0x011c)
BIST Address Register 2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x7	BMBANK BIST Maximum Bank Address Specifies the maximum SDRAM bank address to be used during BIST before the address increments to the next rank.
27:12	RW	0xffff	BMROW BIST Maximum Row Address Specifies the maximum SDRAM row address to be used during BIST before the address increments to the next bank.
11:0	RW	0xfff	BMCOL BIST Maximum Column Address Specifies the maximum SDRAM column address to be used during BIST before the address increments to the next row.

DDR_PUBL_BISTUDPR
Address: Operational Base + offset (0x0120)
BIST User Data Pattern Register

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Bit	Attr	Reset Value	Description
31:16	RW	0xffff	BUDP1 BIST User Data Pattern 1 Data to be applied on odd DQ pins during BIST
15:0	RW	0x0000	BUDP0 BIST User Data Pattern 0 Data to be applied on even DQ pins during BIST

DDR_PUBL_BISTGSR
Address: Operational Base + offset (0x0124)
BIST General Status Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	CASBER CAS Bit Error Indicates the number of bit errors on CAS
29:28	RO	0x0	RASBER RAS Bit Error Indicates the number of bit errors on RAS
27:24	RO	0x0	DMBER DM Bit Error Indicates the number of bit errors on data mask (DM) bit. DMBER[1:0] are for the first DM beat, and DMBER[3:2] are for the second DM beat.
23:22	RO	0x0	TPDBER TPD Bit Error (LPDDR Only) Indicates the number of bit errors on TPD
21:20	RO	0x0	PARBER PAR_IN Bit Error (DIMM Only) Indicates the number of bit errors on PAR_IN
19:3	RO	0x0	reserved
2	RO	0x0	BDXERR BIST Data Error Indicates if set that there is a data comparison error in the byte lane
1	RO	0x0	BACERR BIST Address/Command Error Indicates if set that there is a data comparison error in the address/command lane
0	RO	0x0	BDONE BIST Done Indicates if set that the BIST has finished executing. This bit is reset to zero when BIST is triggered.

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DDR_PUBL_BISTWER
Address: Operational Base + offset (0x0128)
BIST Word Error Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	DXWER Byte Word Error Indicates the number of word errors on the byte lane. An error on any bit of the data bus including the data mask bit increments the error count.
15:0	RO	0x0000	ACWER Address/Command Word Error Indicates the number of word errors on the address/command lane. An error on any bit of the address/command bus increments the error count.

DDR_PUBL_BISTBER0
Address: Operational Base + offset (0x012c)
BIST Bit Error Register 0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ABER Address Bit Error Each group of two bits indicate the bit error count on each of the up to 16 address bits. [1:0] is the error count for A[0], [3:2] for A[1], and so on.

DDR_PUBL_BISTBER1
Address: Operational Base + offset (0x0130)
BIST Bit Error Register 1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ODTBER ODT Bit Error Each group of two bits indicates the bit error count on each of the up to 4 ODT bits. [1:0] is the error count for ODT[0], [3:2] for ODT[1], and so on.
23:16	RO	0x00	CSBER CS# Bit Error Each group of two bits indicates the bit error count on each of the up to 4 CS# bits. [1:0] is the error count for CS#[0], [3:2] for CS#[1], and so on.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	CKEBER CKE Bit Error Each group of two bits indicates the bit error count on each of the up to 4 CKE bits. [1:0] is the error count for CKE[0], [3:2] for CKE[1], and so on.
7:6	RO	0x0	WEBER WE# Bit Error Indicates the number of bit errors on WE#
5:0	RO	0x00	BABER Bank Address Bit Error Each group of two bits indicates the bit error count on each of the up to 3 bank address bits. [1:0] is the error count for BA[0], [3:2] for BA[1], and so on.

DDR_PUBL_BISTBER2
Address: Operational Base + offset (0x0134)
BIST Bit Error Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DQBER Data Bit Error The first 16 bits indicate the error count for the first data beat (i.e. the data driven out on DQ[7:0] on the rising edge of DQS). The second 16 bits indicate the error on the second data beat (i.e. the error count of the data driven out on DQ[7:0] on the falling edge of DQS). For each of the 16-bit group, the first 2 bits are for DQ[0], the second for DQ[1], and so on.

DDR_PUBL_BISTWCSR
Address: Operational Base + offset (0x0138)
BIST Word Count Status Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	DXWCNT Byte Word Count Indicates the number of words received from the byte lane
15:0	RO	0x0000	ACWCNT Address/Command Word Count Indicates the number of words received from the address/command lane

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DDR_PUBL_BISTFWR0
Address: Operational Base + offset (0x013c)
BIST Fail Word Register 0

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	ODTWEBS Bit status during a word error for each of the up to 4 ODT bits
27:24	RO	0x0	CSWEBS Bit status during a word error for each of the up to 4 CS# bits
23:20	RO	0x0	CKEWEBS Bit status during a word error for each of the up to 4 CKE bits
19	RO	0x0	WEWEBS Bit status during a word error for the WE#
18:16	RO	0x0	BAWEBS Bit status during a word error for each of the up to 3 bank address bits
15:0	RO	0x0000	AWEBS Bit status during a word error for each of the up to 16 address bits

DDR_PUBL_BISTFWR1
Address: Operational Base + offset (0x0140)
BIST Fail Word Register 1

Bit	Attr	Reset Value	Description
31	RO	0x0	TPDWEBS Bit status during a word error for the TPD. LPDDR Only.
30	RO	0x0	PARWEBS Bit status during a word error for the PAR_IN. Only for DIMM parity support.
29:20	RO	0x0	reserved
19	RO	0x0	CASWEBS Bit status during a word error for the CAS
18	RO	0x0	RASWEBS Bit status during a word error for the RAS
17:16	RO	0x0	DMWEBS Bit status during a word error for the data mask (DM) bit. DMWEBS [0] is for the first DM beat, and DMWEBS [1] is for the second DM beat.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	DQWEBS Bit status during a word error for each of the 8 data (DQ) bits. The first 8 bits indicate the status of the first data beat (i.e. the status of the data driven out on DQ[7:0] on the rising edge of DQS). The second 8 bits indicate the status of the second data beat (i.e. the status of the data driven out on DQ[7:0] on the falling edge of DQS). For each of the 8-bit group, the first bit is for DQ[0], the second bit is for DQ[1], and so on.

DDR_PUBL_ZQ0CR0
Address: Operational Base + offset (0x0180)
ZQ 0 Impedance Control Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic.

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Bit	Attr	Reset Value	Description
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ0CR1
Address: Operational Base + offset (0x0184)
ZQ 0 Impedance Control Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ0SR0
Address: Operational Base + offset (0x0188)
ZQ 0 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:0	RO	0x0000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ0SR1
Address: Operational Base + offset (0x018c)
ZQ 0 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_ZQ1CR0
Address: Operational Base + offset (0x0190)
ZQ 1 Impedance Control Register 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic.
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ1CR1
Address: Operational Base + offset (0x0194)
ZQ 1 Impedance Control Register 1

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ1SR0
Address: Operational Base + offset (0x0198)
ZQ 1 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved
27:0	RO	0x0000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ1SR1
Address: Operational Base + offset (0x019c)
ZQ 1 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_ZQ2CR0
Address: Operational Base + offset (0x01a0)
ZQ 2 Impedance Control Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.

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Bit	Attr	Reset Value	Description
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic.
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ2CR1
Address: Operational Base + offset (0x01a4)
ZQ 2 Impedance Control Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ2SR0
Address: Operational Base + offset (0x01a8)
ZQ 2 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed

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Bit	Attr	Reset Value	Description
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved
27:0	RO	0x0000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ2SR1
Address: Operational Base + offset (0x01ac)
ZQ 2 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

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DDR_PUBL_ZQ3CR0
Address: Operational Base + offset (0x01b0)
ZQ 3 Impedance Control Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ3CR1
Address: Operational Base + offset (0x01b4)

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ZQ 3 Impedance Control Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ3SR0
Address: Operational Base + offset (0x01b8)
ZQ 3 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved
27:0	RO	0x0000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ3SR1
Address: Operational Base + offset (0x01bc)
ZQ 3 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_DX0GCR
Address: Operational Base + offset (0x01c0)
DATX8 0 General Configuration Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:14 19:17	RW	0x3 0x3	R0RVSL R1RVSL Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are: 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	RTTOAL RTT On Additive Latency Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are: 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	RTTOH RTT Output Hold Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.

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Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

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Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX0GSR0
Address: Operational Base + offset (0x01c4)
DATX8 0 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX0GSR1
Address: Operational Base + offset (0x01c8)
DATX8 0 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX0DLLCR
Address: Operational Base + offset (0x01cc)
DATX8 0 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

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Bit	Attr	Reset Value	Description
17:14	RW	0x0	SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings: 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking: 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX0DQTR
Address: Operational Base + offset (0x01d0)
DATX8 0 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
27:24	RW	0xf	DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
19:16	RW	0xf	DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
11:8	RW	0xf	DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX0DQSTR
Address: Operational Base + offset (0x01d4)
DATX8 0 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	DMDLY DM Delay Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
25:23	RW	0x3	DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x2	R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

DDR_PUBL_DX1GCR
Address: Operational Base + offset (0x0200)
DATX8 1 General Configuration Register

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Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
16:14 19:17	RW	0x3 0x3	R0RVSL R1RVSL Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are: 3’b000: read valid system latency = ideal placement - 3 3’b001: read valid system latency = ideal placement - 2 3’b010: read valid system latency = ideal placement - 1 3’b011: read valid system latency = ideal placement 3’b100: read valid system latency = ideal placement + 1 3’b101: read valid system latency = ideal placement + 2 3’b110: read valid system latency = ideal placement + 3 3’b111: Reserved
13	RW	0x0	RTTOAL RTT On Additive Latency Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are: 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	RTTOH RTT Output Hold Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.

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Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

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Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX1GSR0
Address: Operational Base + offset (0x0204)
DATX8 1 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX1GSR1
Address: Operational Base + offset (0x0208)
DATX8 1 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX1DLLCR
Address: Operational Base + offset (0x020c)
DATX8 1 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

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Bit	Attr	Reset Value	Description
17:14	RW	0x0	SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings: 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking: 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX1DQTR
Address: Operational Base + offset (0x0210)
DATX8 1 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
27:24	RW	0xf	DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
19:16	RW	0xf	DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
11:8	RW	0xf	DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX1DQSTR
Address: Operational Base + offset (0x0214)
DATX8 1 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	DMDLY Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
25:23	RW	0x3	DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x2	R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

DDR_PUBL_DX2GCR
Address: Operational Base + offset (0x0240)
DATX8 2 General Configuration Register

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Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
16:14 19:17	RW	0x3 0x3	R0RVSL R1RVSL Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are: 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	RTTOAL RTT On Additive Latency Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are: 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	RTTOH RTT Output Hold Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.

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Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

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Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX2GSR0
Address: Operational Base + offset (0x0244)
DATX8 2 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX2GSR1
Address: Operational Base + offset (0x0248)
DATX8 2 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX2DLLCR
Address: Operational Base + offset (0x024c)
DATX8 2 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

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Bit	Attr	Reset Value	Description
17:14	RW	0x0	SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings: 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking: 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX2DQTR
Address: Operational Base + offset (0x0250)
DATX8 2 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
27:24	RW	0xf	DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
19:16	RW	0xf	DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
11:8	RW	0xf	DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX2DQSTR
Address: Operational Base + offset (0x0254)
DATX8 2 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	DMDLY DM Delay Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
25:23	RW	0x3	DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x2	R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

DDR_PUBL_DX3GCR

Address: Operational Base + offset (0x0280)

DATX8 3 General Configuration Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
16:14 19:17	RW	0x3 0x3	R0RVSL R1RVSL Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are: 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	RTTOAL RTT On Additive Latency Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are: 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	RTTOH RTT Output Hold Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.

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Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

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Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX3GSR0
Address: Operational Base + offset (0x0284)
DATX8 3 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX3GSR1
Address: Operational Base + offset (0x0288)
DATX8 3 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX3DLLCR
Address: Operational Base + offset (0x028c)
DATX8 3 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

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Bit	Attr	Reset Value	Description
17:14	RW	0x0	SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings: 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking: 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX3DQTR
Address: Operational Base + offset (0x0290)
DATX8 3 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay DQ Delay: Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
27:24	RW	0xf	DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
19:16	RW	0xf	DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
11:8	RW	0xf	DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX3DQSTR
Address: Operational Base + offset (0x0294)
DATX8 3 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	DMDLY DM Delay Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

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Bit	Attr	Reset Value	Description
25:23	RW	0x3	DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are: 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x2	R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are: 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are: 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

7.6 Interface description

DDR IOs for each channel are listed as following Table.

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Pin Name	Description
CK	Active-high clock signal to the memory device.
CK_B	Active-low clock signal to the memory device.
CKEi (i=0,1)	Active-high clock enable signal to the memory device for two chip select.
CS_Bi (i=0,1)	Active-low chip select signal to the memory device. AThere are two chip select.
RAS_B	Active-low row address strobe to the memory device.
CAS_B	Active-low column address strobe to the memory device.
WE_B	Active-low write enable strobe to the memory device.
BA[2:0]	Bank address signal to the memory device.
A[15:0]	Address signal to the memory device.
DQ[31:0]	Bidirectional data line to the memory device.
DQS[3:0]	Active-high bidirectional data strobes to the memory device.
DQS_B[3:0]	Active-low bidirectional data strobes to the memory device.
DM[3:0]	Active-low data mask signal to the memory device.
ODTi (i=0,1)	On-Die Termination output signal for two chip select.
RET_EN	Active-low retention latch enable input.
VREFi (i=0,1,2)	Reference Voltage input for three regions of DDR IO.
ZQ_PIN	ZQ calibration pad which connects 240ohm±1% resistor.
RESET	DDR3 reset signal.

7.7 Application Notes

7.7.1 State transition of PCTL

To operate PCTL, the programmer must be familiar with the available operational states and how to transition to each state from the current state.

Every software programmable register is accessible only during certain operational states. For information about what registers are accessible in each state, refer to "Software Registers," which provides this information in each register description. The general rule is that the PCTL must be in the Init_mem or Config states to successfully write most of the registers.

The following tables provide the programming sequences for moving to the various states of the state machine.

Moving to the Init_mem State

Step	Application	PCTL
1	Read STAT register	Returns the current PCTL state.
2	If STAT.ctl_stat = Init_mem, go to END.	
3	If STAT.ctl_stat =Config, go to Step9.	
4	If STAT.ctl_stat =Access, go to Step8.	
5	If STAT.ctl_stat = Low_power, go to Step7.	
6	Goto Step1.	PCTL is in a Transitional state and not in any of the previous operational states.
7	Write WAKEUP to SCTL.state_cmd and poll STAT.ctl_stat= Access.	Issues SRX, moves to the Access state, updates STAT.ctl_stat =Access when complete.

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Step	Application	PCTL
8	Write CFG to SCTL.state_cmd and poll STAT.ctl_stat= Config.	PCTL stalls the NIF; completes any pending transaction; issues PREA if required; moves into the Config state; updates STAT.ctl_stat =Config whencomplete.
9	Write INIT to SCTL.state_cmd and poll STAT.ctl_stat=Init_mem	Moves into the Init_mem state and updates STAT.ctl_stat =Init_mem.
END		PCTL is in Init_mem state.

Moving to Config State

Step	Application	PCTL
1	Read STAT register.	Returns the current PCTL state.
2	If STAT.ctl_stat= Config, goto END.	
3	If STAT.ctl_stat= Low_power, go toStep6.	
4	If STAT.ctl_stat= Init_mem or Access, go toStep7.	
5	Go to Step1.	PCTL is in a transitional state and is not in any of the previous operational states.
6	Write WAKEUP to CTL.state_cmd and poll STAT.ctl_stat= Access.	Issues SRX, moves to the Access state, and updates STAT.ctl_stat= Access when complete.
7	Write CFG to SCTL.state_cmd and poll STAT.ctl_stat= Config.	PCTL stalls the NIF; completes any pending transaction; issues PREA if required; moves into the Config state; and updates STAT.ctl_stat = Config when complete.
END		PCTL is in Config state.

Moving to Access State

Step	Application	PCTL
1	Read STATregister	Returns the current PCTL state.
2	IfSTAT.ctl_stat= Access, go to END.	
3	IfSTAT.ctl_stat= Config, go to Step9	
4	IfSTAT.ctl_stat= Init_mem, go to Step8	
5	IfSTAT.ctl_stat= Low_power, go to Step7.	
6	Goto Step1.	PCTL is in a transitional state and is not in any of the previous operational states.
7	Write WAKEUP to SCTL.state_cmd and poll STAT.ctl_stat= Access. Goto END	Issues SRX, moves to the Access state, updates STAT.ctl_stat= Access when complete.
8	Write CFG to SCTL.state_cmd and pollSTAT.ctl_stat= Config.	Moves into the Config state, updates STAT.ctl_stat= Config when complete.
9	Write GO to SCTL.state_cmd and poll STAT.ctl_stat= Access.	Moves into the Access state, updates STAT.ctl_stat= Access when complete.
END		PCTL is in Access state.

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Moving to Low Power State

Step	Application	PCTL
1	Read STAT register.	Returns current PCTL state.
2	If STAT.ctl_stat =Low_power, go to END.	
3	If STAT.ctl_stat = Access, go to Step9	
4	If STAT.ctl_stat = Config, go to Step8	
5	If STAT.ctl_stat = Init_mem, go to Step7.	
6	Goto Step1.	PCTL is in transitional state and is not in any of the previous operational states.
7	Write CFG to SCTL.state_cmd and poll STAT.ctl_stat= Config.	Moves into the Config state, updates STAT.ctl_stat = Config when complete.
8	Write GO to SCTL.state_cmd and poll STAT.ctl_stat= Access.	Moves into the Access state, updates STAT.ctl_stat =Access when complete.
9	Write SLEEP to SCTL.state_cmd and poll STAT.ctl_stat= Low_power.	Issues PDX if necessary; completes any pending transactions; issues PREA command; finally, issues SRE and updates STAT.ctl_stat = Low_power.
END		PCTL is in Low Power state

7.7.2 Initialization

Figure 1-14 shows a high-level illustration of the initialization sequence of the PHY. A detailed sequence description and timing diagrams are described in the following. This section assumes a generic configuration port and therefore cfg_clk and cfg_rst_n are shown as the configuration clock and reset, respectively. These signals must be replaced by pclk and presetn if the design is compiled to use the APB configuration port.

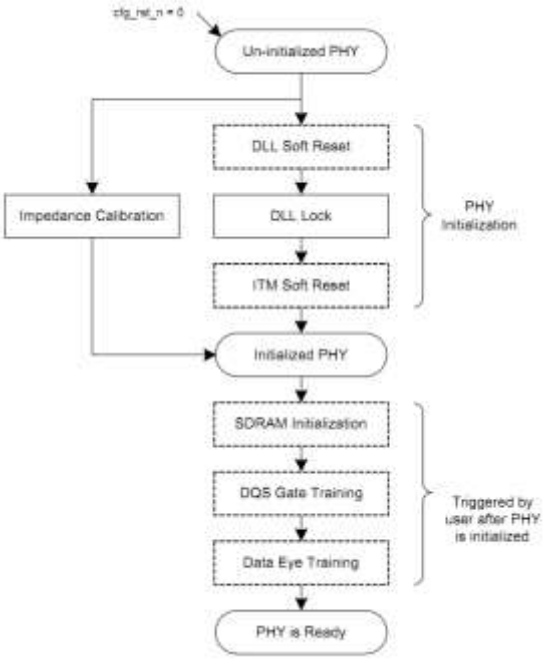

Fig. 7-10 Protocol controller architecture

PHY Initialization

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The initialization sequence has two phases. The first phase happens automatically at reset and is as follows:
1. Before and during configuration reset (i.e. if cfg_rst_n is asserted), the PHY is un-initialized and remains in this state until the reset is de-asserted.
2. At reset de-assertion, the PHY moves into the DLL initialization (lock) phase. This phase may be bypassed at any time by writing a '1' to the DLL initialization bypass register bit (PIR[LOCKBYP]).
3. In parallel to DLL initialization, the impedance calibration phase also starts at reset de-assertion.
This phase can also be bypassed by writing a '1' to the impedance calibration bypass register bit-PIR[ZCALBYP].
4. If the PHY initialization sequence was triggered by the user, a soft reset may optionally be selected to be issued to the ITMs. Initialization that is automatically triggered on reset does not issue a soft reset to the ITMs because the components will already have been reset by the main reset.
5. Once the DLL initialization and impedance calibration phases are done and after the ITMs are reset, the PHY is initialized. Note that if these phases were bypassed, it is up to the user to perform them in software or trigger them at a later time before the PHY can be used.

SDRAM Initialization
The second phase of initialization starts after the PHY is initialized. Each step of this phase is triggered by the user or memory controller and is as follows:
1. Prior to normal operation, DDR SDRAMs must be initialized. The PHYCTL has a built-in SDRAM initialization routine that may be triggered by software or memory controller by writing to the PHY Initialization Register (PIR). The initialization routine built into the PHYCTL is generic and does not require any knowledge of the type or configuration of external SDRAMs to be properly executed. The routine is designed with the relevant JEDEC specifications for the fastest & slowest SDRAMs supported by the PHYCTL to result in a universal initialization sequence. This generic sequence is applicable to DDR3, DDR2, LPDDR2, LPDDR, and DDR SDRAMs.
It is recommended to use the built-in PHYCTL routine to initialize the SDRAM. However, there may be cases such as during system debug when the built-in PHYCTL DRAM initialization is not triggered and DRAM initialization is performed by software or the controller. In these cases the system must first wait for the PHY to initialize, i.e. DLL locked and impedance calibration done, then it must write a '1' to PIR[INIT] bit with PIR[CTLDINT] set to '1' (for controller initialization) or '0' (for software or PHYCTL initialization) to inform the PHYCTL that DRAM initialization will be done later, by software, the controller or by re-triggering on the PHYCTL. The software or controller then executes the initialization sequence by sending relevant commands to the DRAM, respecting the various timing requirements of the initialization sequence.
2. After the SDRAM is initialized, the user or memory controller performs, or triggers the PHYCTL to perform DQS gate training (“Built-in DQS Gate Training” on page 114). The SDRAM must be initialized before triggering DQS gate training.
3. The user or memory controller performs, or triggers the PHYCTL to perform read data eye training. Note that the current version of the PHYCTL does not have the read eye training designed in.
4. The PHY is now ready for SDRAM read/write accesses.

DDR3 Initialization Sequence
The initialization steps for DDR3 SDRAMs are as follows:
1. Optionally maintain RESET# low for a minimum of either 200 us (power-up initialization) or 100ns (power-on initialization). The PHYCTL drives RESET# low from the beginning of reset assertion and therefore this step may be skipped when DRAM initialization is triggered if enough time may already have expired to satisfy the RESET# low time.
2. After RESET# is de-asserted, wait a minimum of 500 us with CKE low.
3. Apply NOP and drive CKE high.
4. Wait a minimum of tXPR.
5. Issue a load Mode Register 2 (MR2) command.

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6. Issue a load Mode Register 3 (MR3) command.
7. Issue a load Mode Register (MR1) command (to set parameters and enable DLL).
8. Issue a load Mode Register (MR0) command to set parameters and reset DLL.
9. Issue ZQ calibration command.
10. Wait 512 SDRAM clock cycles for the DLL to lock (tDLLK) and ZQ calibration (tZQinit) to finish. This wait time is relative to Step 8, i.e. relative to when the DLL reset command was issued onto the SDRAM command bus.

LPDDR2 Initialization Sequence
The initialization steps for LPDDR2 SDRAMs are as follows:
1. Wait a minimum of 100 ns (tINIT1) with CKE driven low.
2. Apply NOP and set CKE high.
3. Wait a minimum of 200 us (tINIT3).
4. Issue a RESET command.
5. Wait a minimum of 1 us + 10 us (tINIT4 + tINIT5).
6. Issue a ZQ calibration command.
7. Wait a minimum of 1 us (tZQINIT).
8. Issue a Write Mode Register to MR1.
9. Issue a Write Mode Register to MR2
10. Issue a Write Mode Register to MR3

Initialization Triggered and bypass
All initialization steps shown in Figure 3-1 on page 34 can be triggered using the PHY Initialization Register (PIR) as described in "PHY Initialization Register (PIR)" on page 47. Writing a '1' to PIR[INIT] register bit will start initialization, with the routines to be run being selected by the corresponding PIR register bits. If multiple routines are selected, they are run in the order shown in Figure 3-1 on page 34. This is also the order of the select bits in PIR register. The completion of the routines is indicated in the PHY General Status Register (PGSR) with the corresponding done status bits (see "PHY General Status Register (PGSR)" on page 52). The PGSR[IDONE] bit indicates the overall completion of the initialization sequence. An initialization done status register bit is cleared (reset to '0') when the corresponding routine is re-triggered.
The de-assertion of reset will automatically trigger the PHYCTL to perform DLL initialization (locking) and impedance calibration. Once the DLL has locked and impedance calibration has completed, the SDRAM initialization and DQS gating may be triggered or performed by software or memory controller.
Since the PHYCTL allows the selection of individual routines to be run when initialization is triggered using PIR register, only those routines that automatically trigger on reset de-assertion have individual bypass capability. This means that DLL locking and/or impedance calibration may be bypassed any time by writing a '1' to the corresponding bypass register bit in the PIR register. Once a routine is bypassed, it is internally registered as completed and the corresponding done status register bit is set in the PGSR register.
It is up to the user to re-trigger or perform the bypassed routine at a later time before the PHY can be used. The PIR[INITBYP] register bit provides the option to bypass the whole initialization sequence.

7.7.3 MDLL and MSDLL Reset Requirements

Reset issued to the MDLL and MSDLL must always meet the following requirements:
1. Reset must always be asserted for a minimum of 50ns to ensure proper reset of the DLL.
2. On power-up, reset must be held for a minimum of 50ns after MVDD has been raised to its full value.
3. After reset has been asserted and then de-asserted, a number of clock cycles must pass for the DLL to achieve lock.
4. The input clock to the DLL must be stable for a minimum of 50ns before DLL reset is de-asserted.
The following additional requirements apply when transitioning to/from bypass mode:

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1. There must be at least 50ns between reset de-assertion and DLL bypass mode entry.
2. The DLL bypass pin must be asserted for at least 1000ns.
3. Reset must always be issued after the DLL mode has changed from bypass to normal mode.
4. A minimum of 100ns is required between bypass de-assertion and reset assertion.
5. Reset must be issued whenever DLL control/trim/option input bits are modified, with the exception of:
   a. Analog/digital test controls
   b. Slave DLL phase trim (if applicable).

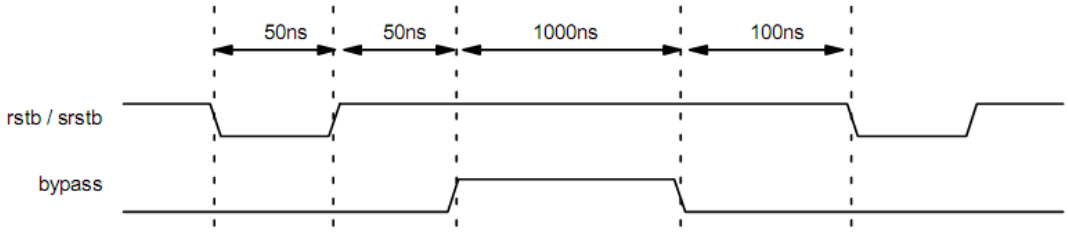

Fig. 7-11 DLL reset requirements

7.7.4 Data Training

Built-in DQS Gate Training

The PHYCTL has a built-in DQS gate training routine that may be triggered by software or memory controller using the PIR register.

DQS gate training returns a number of status, including the done and error status. There are two types of errors. The first type is when no valid window was found for the byte. This is indicated by DTERR register bit in DXnGSR and PGSR registers. This is usually an indication of bad configuration. The second type is when some passing configurations were found but these were interspersed by failures. This is not expected in a working system. A typical window is signified by consecutive passes followed by consecutive failures, e.g. FPPPPPF and not FPPFPPF. This type of error is called an intermittent error and is indicated by the DTIERR register bit in DXnGSR and PGSR registers. Provided for debug purpose is the status of how many passing configurations were found for each byte on each rank. This is indicated by DTPASS field in the DXnGSR register.

Software DQS Gate Training

DQS gate training may also be executed in software using the controller and/or the PUB DCU. Figure 13-16 shows the DQS gate training software algorithm. This is followed by a description of the main phases of the training.

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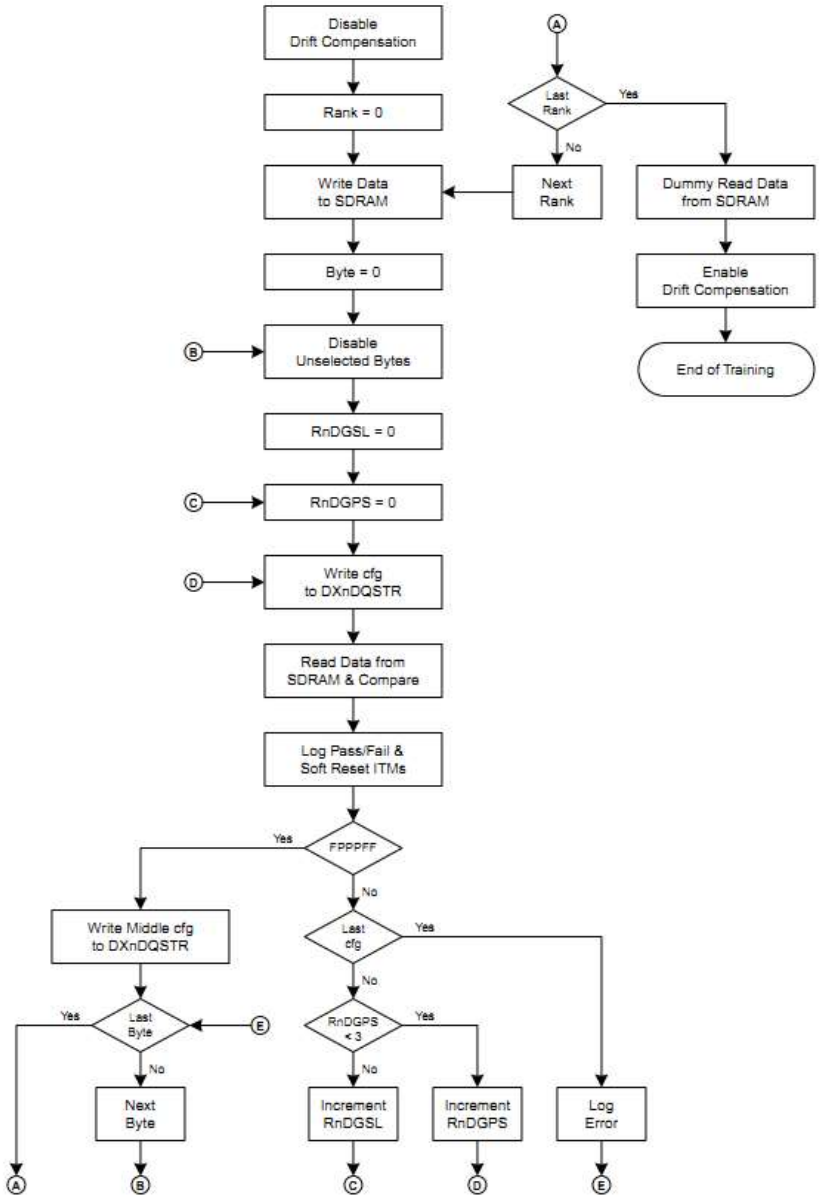

Fig. 7-12 DLL reset requirements

The software DQS gate training phases are as follows:
1. Disable drift compensation by writing '0' to PGCR.DFTCMP register.
2. Start with rank 0, i.e. rank 0 is selected for training.
3. Execute a minimum of two writes to the SDRAM. Any type of data and any SDRAM address can be used for DQS gate training. It is however not recommended to use data that is all zeroes since this may mask read data comparison. The data mask must be set to 0 to enable writing of all bytes. The number of writes must be chosen such that it results in a minimum of eight data beats at the SDRAM. This means at least two write commands when using SDRAM burst length of 4.
4. Start with byte 0 (i.e. byte 0 is selected for training).
5. Disable all the other bytes except the byte that has been selected for training. Bytes are enabled/disabled by writing 1/0 to DXnDGCR.DXEN.
6. Start with the selected rank byte DQS gating system latency (DXnDQSTR.RnDGSL) of 0.
7. Start with the selected rank byte DQS gating phase select (DXnDQSTR.RnDGPS) of 0.
8. Write the selected DQS gating configurations (RnDGSL and RnDGPS) to DXnDQSTR register of the selected byte, making sure the fields for the unselected ranks remain unchanged.
9. Execute reads from the SDRAM locations previously written. The number of reads must be equal to the number of writes used in Step 3. Compare the read data with the expected (written) data and log the pass/fail status as a sequence or history of flags for each trained

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RnDGSL/RnDGPS configuration (e.g. FFPPPPFF). A fail is either when there is a data miscompare or when fewer data than expected is returned. Note that a controller that is designed to always wait for the correct number of read data may need a time-out in case the trained configuration results in fewer data than expected. This is not as issue when using the PUB DCU because it does not wait for the expected number of reads; rather the read count status will indicate if fewer reads were returned.
10. Once the read data has been compared and the pass/fail status logged, issue an ITM soft reset to clear the status of the read data logic in the PHY. This is important because the ITM read data FIFO pointers may be in the wrong state at the end of training an RnDGSL/RnDGPS configuration that resulted in wrong DQS gating window.
11. If two consecutive fails and some passes exist, then this is the end of the training for this rank byte. In this case, do the following:

Select the middle of the passes and write the values to the corresponding fields of DXnDQSTR register, making sure the fields for the unselected ranks remain unchanged
If this is not the last byte, then select the next byte and go to Step 5
If this is the last byte but not the last rank, then select the next rank and go to Step 3
If this is the last byte and the last rank, then go to Step 12 to do final clean-up before the end of the DQS gate training.
If the condition of two consecutive fails and some passes does not exist, then this signals that more RnDGSL/RnDGPS configurations need to be trained for this rank byte. If this is the case, do the following:
if RnDGPS is less than 3, then increment RnDGPS and go to Step 8
if RnDGPS is equal to 3 but RnDGSL is less than 7, then increment RnDGSL and go to Step 7
if RnDGPS is equal to 3 and RnDGSL is equal to 7, then log an error because this is a signal that something in the system is very wrong such that no passing configuration is possible for this rank byte. With such an error condition, you can either terminate the whole training to investigate the system or you can go to train the next byte.

12. Once the training of all ranks and all bytes is finished, issue one or more dummy reads to the same SDRAM locations. This will flush out the DQS drift compensation logic in the PHY and therefore avoid reporting any false drift events caused by previous DQS gating settings.
13. Once the dummy reads have completed, re-enable drift compensation by writing 1 to PGCR.DFTCMP register. This is the end of DQS gate training. Regular memory operations can now commence.

7.7.5 Impedance Calibration

The impedance calibration circuit, which controls the impedance values for ODT and driver output impedance, consists of the following components:

ZQ calibration cell - PZQ
External RZQ precision resistor
Impedance control logic - zctrl
VREF cell (for code encoding and level shifting)
Functional I/O cells

The connectivity of these components is shown as follow figure:

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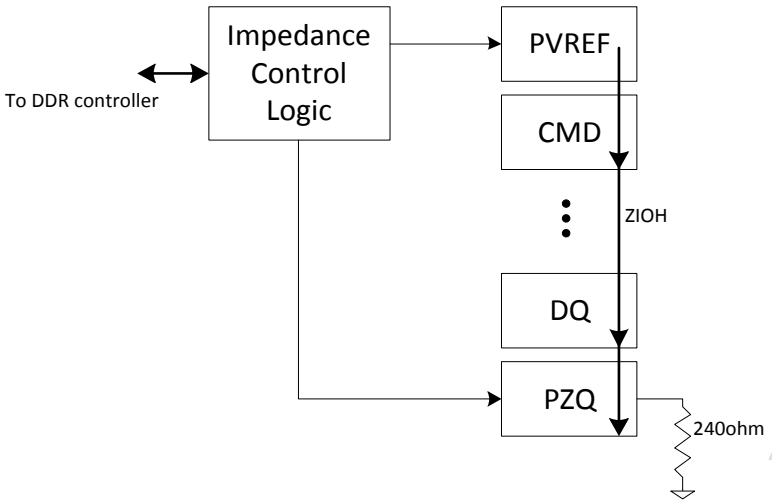

Fig. 7-13 Impedance Calibration Circuit

A single calibration cell (PZQ) is used for the interface. The user connects the PZQ pin through an external 240ohm±1% resistor to ground. One or multiple VREF cells exist in the interface, depending on the total data width of the interface. The ZCTRL bus from the impedance control logic is connected to all VREF cells in the interface. It is not permitted to have a VREF cell in the interface that is not connected to the impedance control logic.
The impedance control logic sends an impedance code through the ZCTRL bus to the VREF cells. The VREF cells encodes this data, level shifts it to the VDDQ power domain, and sends it to both the functional I/O cells and the PZQ cell through the ZIOH bus embedded within the SSTL cells. The PZQ cell also receives the desired divide ratios from the Memory Controller or the user logic. The PZQ cell compares the impedance control code received from the PVREF cell with the external resistor, taking into account the selected divide ratio. The PZQ cell then sends ZCOMP back to the impedance control logic to relay information about impedance matching. The impedance control logic then sends a new impedance code to the PVREF cells. This results in a closed-loop system.
The four impedance elements are calibrated sequentially:

- Pull-up termination impedance
- Pull-down termination impedance
- Pull-up output impedance
- Pull-down output impedance

The ZPROG bus is used to signal which element is being calibrated. The state machine is implemented on the Impedance Controller RTL block.
The impedance control logic connects to the Memory Controller or customer logic to allow full controllability and observability of the loop operation.
The impedance control loop operates with a low bandwidth as compared to the memory system, thus the impedance control logic contains a clock divider to permit operation at a reduced clock frequency.
There are three basic modes of operation:

- Direct Calibration - uses ZPROG settings.
- Override Setting - uses ctrl_ovrd_data settings.
- Custom Calibration - extends calibration beyond the values available on ZPROG

Direct Calibration
In this mode, the user is setting independently the value for ODT (ZPROG[7:4]) and Output Impedance (ZPROG[3:0]) and runs the calibration sequence:
1. Output impedance pulldown
2. Output impedance pull-up
3. On-Die termination (ODT) pull-down
4. ODT pull-up

Override Setting

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In this mode, the user is not using the calibration loop, and instead directly controls the impedance control using zctrl_ovrd_data[19:0] bus, which is parsed in four nibbles that independently control driver pull-down/up and ODT pull-down/up impedance in 31 steps. For example, assuming one step is associated to current I and the calibration voltage is VREF, the programmed impedance for index N is:

ZPROG = K * VREF/(N * I)

K is correction factor, which is approximately equal to 1.Based on the formula, it can be concluded that if index N is increased, then the impedance is decreased.

Custom Calibration

This mode is a two-step procedure combining the previous two modes.

1. The user provides a Direct Calibration using a convenient value and records the Impedance control results from status register.
2. The user applies the correction factor that provides the custom impedance.

The following example assumes that it is required to program Driver Output Impedance to 18 ohms.

1. The user performs a Direct Calibration for driver Zo=36 ohms. For example, assume the result shows that Driver pull-up index is 12, and Driver pull-down index is 13.
2. Calculate and apply the Override Data for 18 ohm impedance adjustment as follows:

   (<cal_value>/<req_value>) * <cal_index>

   Driver pull-down (36/18) * 13 = 26

   Driver pull-up (36/18) * 12 = 24

7.7.6 Retention Functional

The purpose of the retention function is to retain a known state on the signals to the SDRAMs while the system is placed in a low power mode, specifically when the core VDD supply is powered down. The general concept is that an external input signal (RET_EN) is driven low to put the SSTL I/O cells into retention mode shortly before the core VDD supply is powered down. The user must set the SSTL I/O outputs in the state required during power down before asserting RET_EN. This ensures that the output state of all SSTL I/Os are held static in the desired state while core VDD is power down. After core VDD is restored, the user must re-initialize the core logic to a known state before de-asserting the RET_EN signal.
Following figure provides the I/O cell arrangement with retention.

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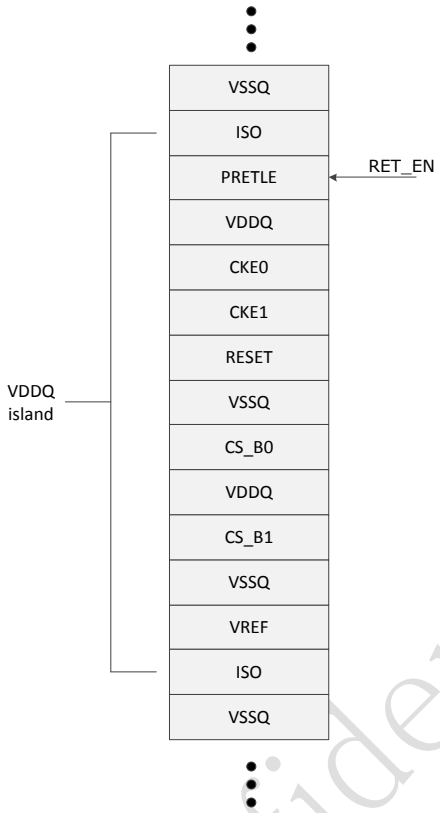

Fig. 7-14 I/O cell arrangement with retention

IOs between two ISO is a VDDQ island, they will maintain power on when other IOs are powered down by RET_EN active.

Following figure provides a sequence of events to enter and exit retention.

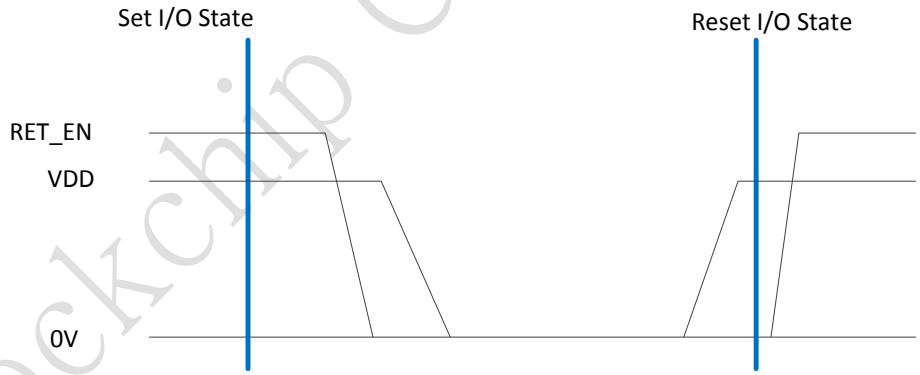

Fig. 7-15 Sequence of Events to Enter and Exit Retention

CKE Retention Mode

An alternative CKE retention mode is supported. This scheme works by placing the SDRAMs into self-refresh mode and then driving the CKE signal low. Core VDD and VDDQ can then both be powered down except for a small VDDQ island supplying the CKE output cell. Two of the special 5um spacer cells ISO are used to break the VDDQ rail in order to create a separate CKE VDDQ island, which is kept powered while core VDD and the main VDDQ are powered down. The sequence of events is as follows:

1. Enter self-refresh mode using the Self-Refresh Command
2. Set CKE low
3. Stop CK/CKB
4. Assert RET_EN (low)
5. Power-Off
6. Power-On
7. After reset is released, execute initialization

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8. De-assert RET_EN (high)
9. Start CK/CKB
10. Set CKE high
11. Exit self-refresh mode

7.7.7 Low Power Operation

Low_power state can be entered/exited via following ways:
Software control of PCTL State machine (highest priority)
Hardware Low Power Interface (middle priority)
Auto Self Refresh feature (lowest priority)
Note the priority of requests from Access to Low_power is highlighted above. The STAT.lp_trig register field reports which of the 3 requests caused the entry to Low_power state.

Software control of PCTL State
The application can request via software to enter the memories into Self Refresh state by issuing the SLEEP command by programming SCTL.PCTL responds to the software request by moving into the Low_power operational state and issuing the SRE command to the memories. Note that the Low_power state can only be reached from the Access state.
In a similar fashion, the application requests to exit the memories from Self Refresh by issuing a WAKEUP command by programming SCTL.. PCTL responds to the WAKEUP command issuing SRX and restoring normal NIF address channel operation.

Hardware Low Power Interface
The hardware low power interface can also be used to enter/exit Self Refresh. The functionality is enabled by setting SCFG.hw_low_power_en=1. Once that bit is set, the input c_sysreq has the ability to trigger entry into the Low Power configuration state just like the software methodology (SCTL.state_cmd = SLEEP). A hardware Low Power entry trigger will be ignored/denied if the input c_active_in=1 or n_avalid=1. It may be accepted if c_active_in=0 and n_avalid=0, depending on the current state of the PCTL. When SCFG.hw_low_power_en=1, the outputs c_sysack and c_active provide feedback as required by the AXI low power interface specification (this interface's operation is defined by the AXI specification). c_sysack acknowledges the request to go into the Low_power state, and c_active indicates when the PCTL is actually in the Low_power state.
The c_active output could also be used by an external Low Power controller to decide when to request a transistion to low power. When MCFG1.hw_idle > 0, c_active = 1'b0 indicates that the NIF has been idle for at least MCFG1.hw_idle * 32 * n_clk cycles while in the Access state. When in low power the c_active output can used by an external Low Power controller to trigger a low power exit. c_active will be driven high when either c_active_in or n_avalid are high. The path from c_active_in and n_valid to c_active is asynhronous so even if the clocks have been removed c_active will assert. The Low Power controller should re-enable the clocks when c_active is driven high while in the Low_power state.

Auto Clock Stop/Power Down/Self Refresh
The Clock Stop and/or Power Down and/or Self Refresh sequence is automatically started by PCTL when the NIF address channel is idle for a number of cycles, depending on the programmed value in MCFG.mddr_lpddr2_clkstop_idle and MCFG.pd_idle and MCFG1.sr_idle. Following table outlines the effect of these settings in conjunction with NIF being idle.

mddr_lpddr2_ clkstop_idle	pd_idle	sr_idle	Memory modes	Memory Type
0	0	0	none	All
>0	0	0	Clock Stop	mDDR/LPDDR2 only
0	>0	0	Power Down	All
>0	>0	0	Clock Stop -> Power Down①	mDDR/LPDDR2 only
0	0	>0	Self Refresh	All

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mddr_lpddr2_ clkstop_idle	pd_idle	sr_idle	Memory modes	Memory Type
>0	0	>0	Clock Stop -> Self Refresh②	mDDR/LPDDR2 only
0	>0	>0	Power Down -> Self Refresh③	All
>0	>0	>0	Clock Stop -> Power Down -> Self Refresh④	mDDR/LPDDR2 only

Note:

①: Clock Stop is entered if NIF is idle for mddr_lpddr2_clkstop_idle. Following on from that, if NIF continues to be idle for a further pd_idle cycles, Clock Stop is exited and Power Down is entered.

*②: Clock Stop is entered if NIF is idle for mddr_lpddr2_clkstop_idle. Following on from that, if NIF continues to be idle for a further sr_idle*32 cycles, Clock Stop is exited and Self Refresh is entered.*

*③: Power Down is entered if NIF is idle for pd_idle. Following on from that, if NIF continues to be idle for a further sr_idle*32 cycles, Power Down is exited and Self Refresh is entered.*

*④: Clock Stop is entered if NIF is idle for mddr_lpddr2_clkstop_idle. Following on from that, if NIF continues to be idle for a further pd_idle cycles, Clock Stop is exited and Power Down is entered. Following on from that, if NIF continues to be idle for a further sr_idle*32 cycles, Power Down is exited and Self Refresh is entered.*

Removing PCTL's n_clk

In LPDDR2 and DDR3, the relationship between SRE/SRX and stopping/starting the memory clock (CK) are formalized and are accounted for automatically by PCTL. With LPDDR2 and DDR3, CK should only be stopped after PCTL has reached the Low_power state. The current operational state can be verified by reading STAT.ctl_stat. The CK must be started and stable before the Software or Hardware Low Power Interface attempts to take the memory out of Self Refresh.

PCTL's n_clk can be safely removed when PCTL is in Low Power state. The sequences outlined in following table should be followed for safe operation:

Step	Application	PCTL
1	Write SLEEP to SCTL.state_cmd and poll STAT.ctl_stat = LOW_POWER.	Tells PCTL to move memories into Self Refresh and waits until this completes.
2	Write TREFI=0. Also, write DFITCRLUPDI=0 and DFIREFMSKI=0, if they are not already 0.	Stops any MC-driven DFI updates occurring internally with PCTL
3	Wait a minimum interval which is equivalent to the PCTL's Refresh Interval (previous value of TREFI*TOGCNT100N*internal timers clock period;	Ensures any already scheduled PHY/PVT updates have completed successfully.
4	Stop toggling n_clk to PCTL.	n_clk logic inside PCTL is stopped.
end		

Step	Application	PCTL
1	Drive c_active_in low	Confirms that system external to PCTL can accept a Low- power request
2	Drive c_sysreq low	System Low-power request
3	Wait for PCTL to drive c_sysack low	PCTL Low-power request acknowledgement
4	Check value of c_active when Step 3 occurs. - if c_active=1, request denied. Cannot remove n_clk. Go to END. - if c_active=0, request accepted.	PCTL low-power request status response
5	Stop toggling n_clk to PCTL	n_clk logic inside PCTL is stopped
end		

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Deep Power-Down

Compared with DDR2/DDR3, mDDR and LPDDR2 has an additional low power mode (Deep Power Down) :

Software-driven Deep Power Down Entry – on reception of DPDE from the application, PCTL drives CKE low for TDPD.t_dpd. After TDPD, MCMD.start_cmd will be cleared to 1'b0. The following are recommended values for TDPD:
mDDR: TDPD=0
LPDDR2: dependent on if the system wants to immediately power off the PCTL after Deep Power down is entered:
If PCTL not Powered off: TDPD=500μs
Else if PCTL is Powered off: TDPD=0 - up to higher level system to meet tDPD requirement.
To Exit Deep Power Mode, full initialization of the memories must be performed.

7.7.8 PHY Power Down

The PHYCTL includes several registers for putting certain components of the PHY in power down mode. The PHTCTL also supports DFI-initiated power-down of its components using the DFI low-power protocol.
Several components of the PHY can be powered down using PHYCTL registers. There are separate power-down register bits for the address/command lane and for each byte lane. Also there are separate controls for powering down the I/Os versus powering down the DLL.
Following table describes the registers that are used to power down various components of the PHY.

Register Name	Bit Field	Description
PIR	DLLBYP	Bypasses, and hence disables or powers down all PHY DLLs.
ACDLLCR	DLLDIS	Disables (powers down) the address/command lane DLL
ACIOCR	ACPDD	Powers down the output drivers for address/command lane signal I/Os. Different groups of signals have dedicated driver power-down control registers to allow finer selection of signals to power down, especially that some signals, such as CKE and RST#, are required to remain powered up when the SDRAM is in self-refresh mode. Each rank CS# signal and each CK/CK# pair has dedicated driver power down control registers, with the other rank-specific signals (CKE and ODT) of each rank being controlled by separate power down control registers in a separate PUB register (DSGCR). There is also a dedicated driver power down control register for SDRAM reset signal. However, the rest of the signals going to the SDRAM (address, bank address, RAS#, CAS#, WE#, and PAR_IN) share a common driver power down register just dedicated for this group. The LPDDR TPD signal has a dedicated output driver power down control register in a separate PUB register (DSGCR).
ACIOCR	ACPDR	Powers down the input receivers for address/command lane signal I/Os. Different groups of signals have dedicated receiver power-down control registers to allow finer selection of signals to power down. Each rank and each CK/CK# pair has dedicated receiver power down control register, with all rank-specific signals (CKE, ODT, and CS#) of each rank sharing a common, but rank-specific, receiver power down control register. There is also a dedicated receiver power down control register for SDRAM reset pins. However, the rest of the signals going to the SDRAM (address, bank address, RAS#, CAS#, WE#, PAR_IN, TPD) share a common receiver power down register just dedicated for this group.
DXCCR	DXPDD	Powers down the output drivers for DQ, DM, and DQS/DQS# signal I/Os of all byte lanes. This is a convenient way of powering down the output drivers of all byte lane I/Os with just a single register write. In addition to this, each byte has a dedicated output driver power-down register control to allow only selected bytes to be powered down.
DXCCR	DXPDR	Powers down the input receivers for DQ, DM, and DQS/DQS# signal I/Os of all byte lanes. It also powers down the PDQSR cells of all bytes. This is a convenient way of powering down the input receivers of all byte lane I/Os with just a single register write.

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Register Name	Bit Field	Description
		In addition to this, each byte has a dedicated input receiver power-down register control to allow only selected bytes to be powered down.
DSGCR	CKEPDD	Powers down the output drivers for CKE I/Os. Each rank CKE has a dedicated driver power down control register to allow finer control of CKE I/O driver power-down, especially that the CKE I/O driver of an SDRAM that is in self refresh is required to remain powered up.
DSGCR	ODTPDD	Powers down the output drivers for ODT I/Os. Each rank ODT has a dedicated driver power down control register to allow finer control of ODT I/O driver power-down, especially that the ODT I/O driver of an SDRAM that is in self refresh or power down mode may be required in certain DDR modes to remain powered up.
DSGCR	TPDPD	Powers down the output driver for the optional LPDDR TPD signal I/O.
DSGCR	NL2PD	Powers down the output driver and the input receiver on the I/O for non-LPDDR2 signals (ODT, RAS#, CAS#, WE#, and BA). This may be used when a chip that is designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode, in which case one may want to power down the unused I/Os. This power down control register is in addition to (ORed with) the individual ACIOCR power down control registers for these signals.
ZQnCR0	ZQPD	Powers down the PZQ cell. Each PZQ has a dedicated power down control register.
DXnDLLCR	DLLDIS	Disables (powers down) the byte lane DLL. Each byte lane has a dedicated DLL power down control register.
DXnGCR	DXPDD	Powers down the output drivers for DQ, DM, and DQS/DQS# signal I/Os of the byte lane. Each byte lane has a dedicated output driver power down control register, in conjunction with the global output driver power down control register DXCCR.DXPDD.
DXnGCR	DXPDR	Powers down the input receivers for DQ, DM, and DQS/DQS# signal I/Os of the byte lane. Each byte lane has a dedicated input receiver power down control register, in conjunction with the global input receiver power down control register DXCCR.DXPDR
DXnGCR	DQSRPD	Powers down the PDQSR cells of the byte lane. Each byte lane has a dedicated PDQSR power down control register, in conjunction with the global PDQSR power down control register DXCCR.DXPDR.
PGCR	PDDISDX	Selects whether the I/Os and DLL of a disabled byte should automatically be powered down by the PUB. A byte can be disabled by writing a '0' to the DXnGCR.DXEN register or by using the DFI data byte disable (dfi_data_byte_disable) signal.
DSGCR	LPIOPD	Specifies whether the PHY should respond to the controller-initiated DFI low power opportunity request and power down the I/Os of the PHY.
DSGCR	LPDLLPD	Specifies whether the PHY should respond to the controller-initiated DFI low power opportunity request and power down the DLL of the PHY if the requested wakeup time is greater than 2048 clock cycles

DFI-Initiated Power-Down

There are two ways how the controller can initiate PHY power down through the DFI interface. The first method is when the controller asserts the DFI data byte disable (dfi_data_byte_disable) signal during initialization when the DFI initialization start (dfi_init_start) signal is high. In this state, the PHY will power down the DLL and I/Os of the selected bytes if it is configured through DSGCR.BDISEN to respond to DFI data byte disable and if disabled bytes are configured through PGCR.PDDISDX to be powered down. The DFI data byte disable feature is normally used as a static configuration to disable bytes that are not being used.

The controller can also initiate PHY power down by using the DFI low power control interface. This is a dynamic low power request-acknowledge protocol that the controller may use to put the PHY into low power mode when it is not being used for a prolonged time. The PHY will acknowledge a low power request from the controller and power down I/Os and DLLs if it is configured to do so through DSGCR.LPIOPD and DSGCR.LPDLLPD. If the low power wakeup time requested by the controller is less than 2048 clock cycles, then only the I/Os will be powered down. Otherwise if the wakeup time is equal to or more than 2048 cycles, then the DLLs and the I/Os are all powered down. If the DLLs are powered down, then on low power

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wakeup the PUB will soft reset the DLLs and wait for them to lock before acknowledging the low power wakeup request to the controller.

7.7.9 Dynamic ODT for I/Os

By default the DFI turns on the ODT for the PHY I/Os for DQ/DQS# only when there is read data coming back. This is called dynamic ODT control and is used to reduce power consumed by the termination resistors. The DFI uses the timing of the DQS gating to accurately place the PHY I/O ODT enable signal around the read data. Typically, the DFI turns on the byte ODT enable signal 2 clocks before the pre-amble and turns it off one clock after the post-amble. This guarantees correct setup and hold on the I/Os.
The PHY ODT signal does not go through the ITMs and therefore has to fan out to the DQ/DQS from RTL logic in the PHYCTL. This may result in different timing on these signals depending on the routing. For this reason various programmable features are provided on the ODT control signals to help mitigate some of the timing issues that may result from different implementations. These are described in the DXnGCR register. In summary, both the starting position and the width of the enable signal can be adjusted relative to the default position and lengths.

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Chapter 8 Embedded SRAM

8.1 Overview

The Embedded SRAM is the AXI slave device, which supports read and write access to provide system fast access data storage.

8.1.1 Features supported

Provide 96KB access space
Support security and non-security access
Security or non-security space is software programmable
Security space is nx4KB(up to whole memory space)
Support 64bit AXI bus

8.1.2 Features not supported

Don’t support AXI lock transaction
Don’t support AXI exclusive transaction
Don’t support AXI cache function
Don’t support AXI protection function

8.2 Block Diagram

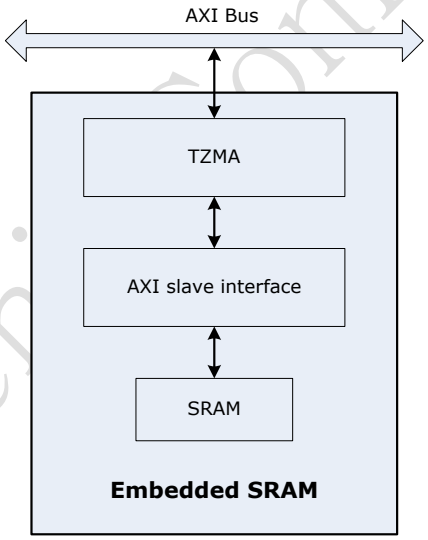

Fig. 8-1 Embedded SRAM block diagram

8.3 Function Description

8.3.1 TZMA

Please refer to 16.3.3 for TZMA functional description.

8.3.2 AXI slave interface

The AXI slave interface is bridge which translate AXI bus access to SRAM interface.

8.3.3 Embedded SRAM access path

The Embedded SRAM can only be accessed by Cortex-A17 and DMAC_BUS.

8.3.4 Remap

The Embedded SRAM support remap.

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Before remap, the Embedded SRAM address range is 0xff70_0000~0xff71_7fff,
After set remap, (ref Security GRF register SGRF_SCON0, bit[7]), the system can still access the Embedded SRAM by the old address. at same time, the system also can access the Embedded SRAM by the new address 0xfffe_0000 ~ 0xffff_7fff (include the bootaddr)

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Chapter 9 NandC(Nand Flash Controller)

9.1 Overview

Nand Flash Controller (NandC) is used to control data transmission from host to flash device or from flash device to host. NandC is connected to AHB BUS through an AHB Master and an AHB Slave. The data transmission between host and external memory can be done through AHB Master interface or AHB Slave interface.

NandC supports the following features:

- NandC AHB bus clock (hclk) is asynchronous to NandC working clock (nclk)
- Software Interface Type
  - Support directly mode
  - Support LLP(Linked List Pointer) mode
- Flash Interface Type
  - Support Asynchronous Flash Interface with 8bits datawidth ("Asyn8x" for short)
  - Support Asynchronous Flash Interface with 16bits data width ("Asyn16x" for short)
  - Support ONFI Synchronous Flash Interface ("ONFI Syn" for short)
  - Support Toggle Flash Interface ("Toggle" for short)
  - Support 8 flash devices at most
- Flash Type
  - Support Managed NAND Flash(LBA) and Raw NAND Flash(NO-LBA)
  - Support SLC/MLC/TLC Flash
- Flash Interface Timing
  - Asyn8x: configurable timing, one byte per two Nandc working clocks at the fastest speed
  - Asyn16x: configurable timing, two bytes per two Nandc working clocks at the fastest speed
  - ONFI Syn: configurable timing, two bytes per two Nandc working clocks at the fastest speed
  - Toggle: configurable timing, two byte per two Nandc working clocks at the fastest speed
- Randomizer Ability
  - Support three randomizer mode with different polynomial
  - Support two randomizer width, 8bit and 16bit parallel
- BCH/ECC Ability
  - 16bit/1KB BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 1K bytes data
  - 24bit/1KB BCH/ECC: support 24bitBCH/ECC, which can detect and correct up to 24 error bits in every 1K bytes data
  - 40bit/1KB BCH/ECC: support 40bitBCH/ECC, which can detect and correct up to 40 error bits in every 1K bytes data
  - 60bit/1KB BCH/ECC: support 60bitBCH/ECC, which can detect and correct up to 60 error bits in every 1K bytes data
  - 8bit/512B BCH/ECC: support 8bitBCH/ECC, which can detect and correct up to 8 error bits in every 512 bytes data
  - 12bit/512B BCH/ECC: support 12bitBCH/ECC, which can detect and correct up to 12 error bits in every 512 bytes data
  - 20bit/512B BCH/ECC: support 20bitBCH/ECC, which can detect and correct up to 20 error bits in every 512 bytes data
  - 30bit/512B BCH/ECC: support 30bitBCH/ECC, which can detect and correct up to 30 error bits in every 512 bytes data
  - 16bit/512B BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 512 bytes data
  - 24bit/512B BCH/ECC: support 24bitBCH/ECC, which can detect and correct up to 24

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error bits in every 512 bytes data
  - 40bit/512B BCH/ECC: support 40bitBCH/ECC, which can detect and correct up to 40 error bits in every 512 bytes data
  - 60bit/512B BCH/ECC: support 60bitBCH/ECC, which can detect and correct up to 60 error bits in every 512 bytes data
- Transmission Ability
  - Support 32K bytes data transmission at a time at most
  - Support two transfer working modes: Bypass or DMA
  - Support two transfer codeword size for Managed NAND Flash: 1024 bytes/codeword or 512 bytes/codeword
- Internal Memory
  - 2 built-in srams, and the size is 1k bytes respectively
  - Can be accessed by other masters
  - Can be operated in pingpang mode by other masters

9.2 Block Diagram

NandC comprises with:

- MIF: AHB Master Interface
- SIF : AHB Slave Interface
- SRIF : Sram Interface
- TRANSC : Transfer Controller
- LLPC : LLP Controller
- BCHENC : BCH Encoder
- BCHDEC : BCH Decoder
- RANDMZ : Randomizer
- FIF_GEN : Flash Interface Generation
- DLC : Delay Line Controller

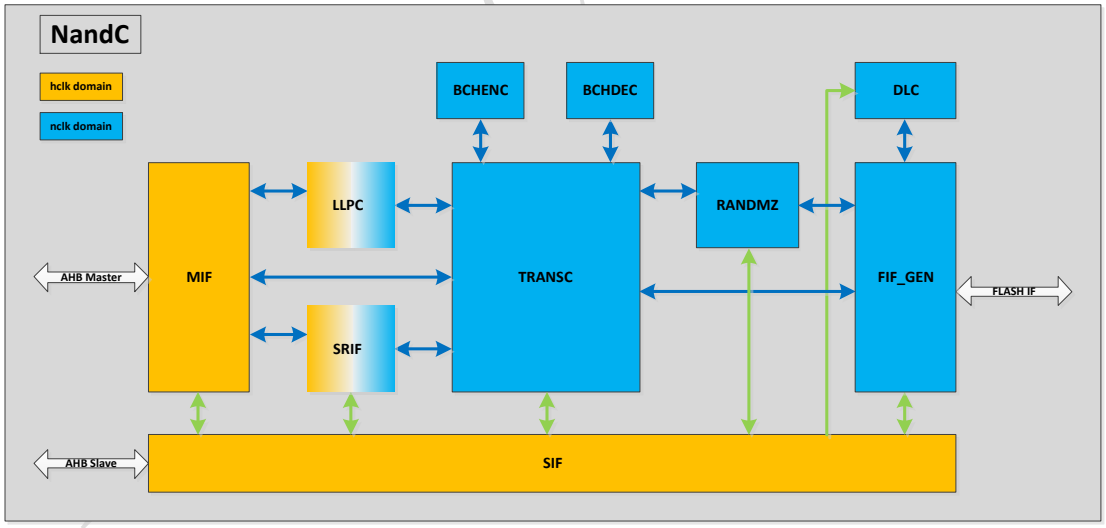

Fig. 9-1 NandC Block Diagram

9.3 Function Description

9.3.1 AHB Interface

There is an AHB master interface in NandC, which is selectable and configurable. It is responsible for transferring data from external memory to internal memory when flash program, or inverse when flash read; and transferring LLP data from external memory to internal register file when LLP is active.

There is an AHB slave interface in NandC. It is responsible for accessing registers and internal

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memories. The addresses of these registers and memories are listed in "Internal Address Mapping" section.

9.3.2 Flash Type/Flash Interface

Flash device with different types of interfaces is supported. These interfaces include: asynchronous 8bits flash interface, asynchronous 16bits flash interface, ONFI synchronous flash interface, toggle flash interface, and so on. You can select one of them by software (configure FMCTL) to suit for these devices. Also you can configure their timing parameters by software (configure FMWAIT_ASYN/FMWAIT_SYN) to have your desired rate.

9.3.3 Linked List Pointer Mode (LLP)

To save the software resource and improve the performance, a LLP is add, which is selectable. When LLP is selected, the flash operation instructions stored in external memory with specific format should be loaded for flash working. The detailed format and working flow are referred to "LLP Application" section.

9.3.4 BCH Encoder/BCH Decoder

The BCH Encoder is responsible for encoding data to be written into flash device. The max encoded length is 1133bytes, in which the data length is 1024bytes, system information is 4bytes, BCH code is 105bytes.

The BCH Decoder is responsible for decoding data read from flash device. The max decoded length is 1133bytes, in which the data length is 1024bytes, spare length is 109bytes.

9.3.5 Randomizer

To improve device lifetime, a randomizer is added in NandC. It includes two parts: Scrambler and Descrambler, which is responsible for scrambling data to be written into flash after bch encoding, and descramblingdata read from flash before bch decoding.

9.3.6 Delay Line Controller

For ONFI Synchronous Flash or Toggle Flash, the data read from flash follows with a strobe signal: DQS, where a skew between them exists. To remove the skew and improve the timing between data and DQS, a Delay Line Controller is needed. It is responsible for detecting the phase of the signal similar to DQS, determining the element number to be shifted, and then shifting the DQS with the determined number.

9.4 Register Description

9.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 9-1 NandC Address Mapping

Base Address[12:8]	Device	Address Length	Offset Address Range
5'b00_00x(x=0, 1)	FLR	512 BYTE	0x0000 ~ 0x01ff
5'b00_01x(x=0, 1)	SPR	512 BYTE	0x0200 ~ 0x03ff
5'b00_10x(x=0, 1)	FLR1	512 BYTE	0x0400 ~ 0x05ff
5'b00_11x(x=0,1)	FLR2	512 BYTE	0x0600 ~ 0x07ff
5'b01_000	Flash0	256 BYTE	0x0800 ~ 0x08ff
5'b01_001	Flash1	256 BYTE	0x0900 ~ 0x09ff

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Base Address[12:8]	Device	Address Length	Offset Address Range
5'b01_010	Flash2	256 BYTE	0x0a00 ~ 0x0aff
5'b01_011	Flash3	256 BYTE	0x0b00 ~ 0x0bff
5'b01_100	Flash4	256 BYTE	0x0c00 ~ 0x0cff
5'b01_101	Flash5	256 BYTE	0x0d00 ~ 0x0dff
5'b01_110	Flash6	256 BYTE	0x0e00 ~ 0x0eff
5'b01_111	Flash7	256 BYTE	0x0f00 ~ 0x0fff
5'b10_0xx(x=0, 1)	Sram0	1K BYTE	0x1000 ~ 0x13ff
5'b10_1xx(x=0, 1)	Sram1	1K BYTE	0x1400 ~ 0x17ff

9.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
NANDC_FMCTL	0x0000	W	0x00000200	Flash Interface Control Register
NANDC_FMWAIT_ASYN	0x0004	W	0x3f03f7ff	Flash Timing Control Register For Asynchronous Timing
NANDC_FLCTL	0x0008	W	0x00100000	Internal Transfer Control Register
NANDC_BCHCTL	0x000c	W	0x00000008	BCH Control Register
NANDC_MTRANS_CFG	0x0010	W	0x000001d0	Bus Transfer Configuration Register
NANDC_MTRANS_SADDR0	0x0014	W	0x00000000	Start Address Register For Page Data Transmission
NANDC_MTRANS_SADDR1	0x0018	W	0x00000000	Start Address Register For Spare Data Transmission
NANDC_MTRANS_STAT	0x001c	W	0x00000000	Bus Transfer Status Register
NANDC_BCHST0	0x0020	W	0x04000000	BCH Status Register For Codeword 0~1
NANDC_BCHST1	0x0024	W	0x00000000	BCH Status Register For Codeword 2~3
NANDC_BCHST2	0x0028	W	0x00000000	BCH Status Register For Codeword 4~5
NANDC_BCHST3	0x002c	W	0x00000000	BCH Status Register For Codeword 6~7
NANDC_BCHST4	0x0030	W	0x00000000	BCH Status Register For Codeword 8~9
NANDC_BCHST5	0x0034	W	0x00000000	BCH Status Register For Codeword 10~11
NANDC_BCHST6	0x0038	W	0x00000000	BCH Status Register For Codeword 12~13
NANDC_BCHST7	0x003c	W	0x00000000	BCH Status Register For Codeword 14~15
NANDC_BCHLOC0	0x0040	W	0x00000000	BCH Error Bit Location Number Register For Codeword 0~5
NANDC_BCHLOC1	0x0044	W	0x00000000	BCH Error Bit Location Number Register For Codeword 6~11
NANDC_BCHLOC2	0x0048	W	0x00000000	BCH Error Bit Location Number Register For Codeword 12~17
NANDC_BCHLOC3	0x004c	W	0x00000000	BCH Error Bit Location Number Register For Codeword 24~29
NANDC_BCHLOC4	0x0050	W	0x00000000	BCH Error Bit Location Number Register For Codeword 24~29

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Name	Offset	Size	Reset Value	Description
NANDC_BCHLOC5	0x0054	W	0x00000000	BCH Error Bit Location Number Register For Codeword 30~31
NANDC_BCHLOC6	0x0058	W	0x00000000	Highest Bit For BCH Error Bit Location Number Register
NANDC_BCHDE0_0	0x0070	W	0x00000000	BCH decode result of 0th error bit for codeword 0
NANDC_BCHDE0_1	0x0074	W	0x00000000	BCH decode result of 1th error bit for codeword 0
NANDC_BCHDE0_2	0x0078	W	0x00000000	BCH decode result of 2th error bit for codeword 0
NANDC_BCHDE0_3	0x007c	W	0x00000000	BCH decode result of 3th error bit for codeword 0
NANDC_BCHDE0_4	0x0080	W	0x00000000	BCH decode result of 4th error bit for codeword 0
NANDC_BCHDE0_5	0x0084	W	0x00000000	BCH decode result of 5th error bit for codeword 0
NANDC_BCHDE0_6	0x0088	W	0x00000000	BCH decode result of 6th error bit for codeword 0
NANDC_BCHDE0_7	0x008c	W	0x00000000	BCH decode result of 7th error bit for codeword 0
NANDC_BCHDE0_8	0x0090	W	0x00000000	BCH decode result of 8th error bit for codeword 0
NANDC_BCHDE0_9	0x0094	W	0x00000000	BCH decode result of 9th error bit for codeword 0
NANDC_BCHDE0_10	0x0098	W	0x00000000	BCH decode result of 10th error bit for codeword 0
NANDC_BCHDE0_11	0x009c	W	0x00000000	BCH decode result of 11th error bit for codeword 0
NANDC_BCHDE0_12	0x00a0	W	0x00000000	BCH decode result of 12th error bit for codeword 0
NANDC_BCHDE0_13	0x00a4	W	0x00000000	BCH decode result of 13th error bit for codeword 0
NANDC_BCHDE0_14	0x00a8	W	0x00000000	BCH decode result of 14th error bit for codeword 0
NANDC_BCHDE0_15	0x00ac	W	0x00000000	BCH decode result of 15th error bit for codeword 0
NANDC_BCHDE0_16	0x00b0	W	0x00000000	BCH decode result of 16th error bit for codeword 0
NANDC_BCHDE0_17	0x00b4	W	0x00000000	BCH decode result of 17th error bit for codeword 0
NANDC_BCHDE0_18	0x00b8	W	0x00000000	BCH decode result of 18th error bit for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_19	0x00bc	W	0x00000000	BCH decode result of 19th error bit for codeword 0
NANDC_BCHDE0_20	0x00c0	W	0x00000000	BCH decode result of 20th error bit for codeword 0
NANDC_BCHDE0_21	0x00c4	W	0x00000000	BCH decode result of 21th error bit for codeword 0
NANDC_BCHDE0_22	0x00c8	W	0x00000000	BCH decode result of 22th error bit for codeword 0
NANDC_BCHDE0_23	0x00cc	W	0x00000000	BCH decode result of 23th error bit for codeword 0
NANDC_BCHDE1_0	0x00d0	W	0x00000000	BCH decode result of 0th error bit for codeword 1
NANDC_BCHDE1_1	0x00d4	W	0x00000000	BCH decode result of 1th error bit for codeword 1
NANDC_BCHDE1_2	0x00d8	W	0x00000000	BCH decode result of 2th error bit for codeword 1
NANDC_BCHDE1_3	0x00dc	W	0x00000000	BCH decode result of 3th error bit for codeword 1
NANDC_BCHDE1_4	0x00e0	W	0x00000000	BCH decode result of 4th error bit for codeword 1
NANDC_BCHDE1_5	0x00e4	W	0x00000000	BCH decode result of 5th error bit for codeword 1
NANDC_BCHDE1_6	0x00e8	W	0x00000000	BCH decode result of 6th error bit for codeword 1
NANDC_BCHDE1_7	0x00ec	W	0x00000000	BCH decode result of 7th error bit for codeword 1
NANDC_BCHDE1_8	0x00f0	W	0x00000000	BCH decode result of 8th error bit for codeword 1
NANDC_BCHDE1_9	0x00f4	W	0x00000000	BCH decode result of 9th error bit for codeword 1
NANDC_BCHDE1_10	0x00f8	W	0x00000000	BCH decode result of 10th error bit for codeword 1
NANDC_BCHDE1_11	0x00fc	W	0x00000000	BCH decode result of 11th error bit for codeword 1
NANDC_BCHDE1_12	0x0100	W	0x00000000	BCH decode result of 12th error bit for codeword 1
NANDC_BCHDE1_13	0x0104	W	0x00000000	BCH decode result of 13th error bit for codeword 1
NANDC_BCHDE1_14	0x0108	W	0x00000000	BCH decode result of 14th error bit for codeword 1
NANDC_BCHDE1_15	0x010c	W	0x00000000	BCH decode result of 15th error bit for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE1_16	0x0110	W	0x00000000	BCH decode result of 16th error bit for codeword 1
NANDC_BCHDE1_17	0x0114	W	0x00000000	BCH decode result of 17th error bit for codeword 1
NANDC_BCHDE1_18	0x0118	W	0x00000000	BCH decode result of 1th error bit for codeword 1
NANDC_BCHDE1_19	0x011c	W	0x00000000	BCH decode result of 19th error bit for codeword 1
NANDC_BCHDE1_20	0x0120	W	0x00000000	BCH decode result of 20th error bit for codeword 1
NANDC_BCHDE1_21	0x0124	W	0x00000000	BCH decode result of 21th error bit for codeword 1
NANDC_BCHDE1_22	0x0128	W	0x00000000	BCH decode result of 22th error bit for codeword 1
NANDC_BCHDE1_23	0x012c	W	0x00000000	BCH decode result of 23th error bit for codeword 1
NANDC_DLL_CTL_REG 0	0x0130	W	0x007f7f05	DLL Control Register 0
NANDC_DLL_CTL_REG 1	0x0134	W	0x00000022	DLL Control Register 1
NANDC_DLL_OBS_REG 0	0x0138	W	0x00000200	DLL Status Register
NANDC_RANDMZ_CFG	0x0150	W	0x00000000	Randomizer Configure Register
NANDC_FMWAIT_SYN	0x0158	W	0x00000000	Flash Timing Control Register For Synchronous Timing
NANDC_MTRANS_STAT 2	0x015c	W	0x00000000	Bus Transfer Status Register2
NANDC_NANDC_VER	0x0160	W	0x56363232	Nandc Version Register
NANDC_LLP_CTL	0x0164	W	0x00000000	LLP Control Register
NANDC_LLP_STAT	0x0168	W	0x00000001	LLP Status Register
NANDC_INTEN	0x016c	W	0x00000000	NandC Interrupt Enable Register
NANDC_INTCLR	0x0170	W	0x00000000	NandC Interrupt Clear Register
NANDC_INTST	0x0174	W	0x00000000	NandC Interrupt Status Register
NANDC_SPARE0_0	0x0200	W	0xffffffff	System Information for codeword 0
NANDC_SPARE0_1	0x0204	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_2	0x0208	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_3	0x020c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_4	0x0210	W	0x00000000	Spare Data and BCH Encode Information for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_SPARE0_5	0x0214	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_6	0x0218	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_7	0x021c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_8	0x0220	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_9	0x0224	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_10	0x0228	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_11	0x022c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE1_0	0x0230	W	0xffffffff	System Information for codeword 1
NANDC_SPARE1_1	0x0234	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_2	0x0238	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_3	0x023c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_4	0x0240	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_5	0x0244	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_6	0x0248	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_7	0x024c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_8	0x0250	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_9	0x0254	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_10	0x0258	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_11	0x025c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE0_12	0x0260	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_13	0x0264	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_14	0x0268	W	0x00000000	Spare Data and BCH Encode Information for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_SPARE0_15	0x026c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_16	0x0270	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_17	0x0274	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_18	0x0278	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_19	0x027c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_20	0x0280	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_21	0x0284	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_22	0x0288	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_23	0x028c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_24	0x0290	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_25	0x0294	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_26	0x0298	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_27	0x029c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE1_12	0x02a0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_13	0x02a4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_14	0x02a8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_15	0x02ac	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_16	0x02b0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_17	0x02b4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_18	0x02b8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_19	0x02bc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_SPARE1_20	0x02c0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_21	0x02c4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_22	0x02c8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_23	0x02cc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_24	0x02d0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_25	0x02d4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_26	0x02d8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_27	0x02dc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_BCHDE0_24	0x0400	W	0x00000000	BCH decode result of 24th error bit for codeword 0
NANDC_BCHDE0_25	0x0404	W	0x00000000	BCH decode result of 25th error bit for codeword 0
NANDC_BCHDE0_26	0x0408	W	0x00000000	BCH decode result of 26th error bit for codeword 0
NANDC_BCHDE0_27	0x040c	W	0x00000000	BCH decode result of 27th error bit for codeword 0
NANDC_BCHDE0_28	0x0410	W	0x00000000	BCH decode result of 28th error bit for codeword 0
NANDC_BCHDE0_29	0x0414	W	0x00000000	BCH decode result of 29th error bit for codeword 0
NANDC_BCHDE0_30	0x0418	W	0x00000000	BCH decode result of 30th error bit for codeword 0
NANDC_BCHDE0_31	0x041c	W	0x00000000	BCH decode result of 31th error bit for codeword 0
NANDC_BCHDE0_32	0x0420	W	0x00000000	BCH decode result of 32th error bit for codeword 0
NANDC_BCHDE0_33	0x0424	W	0x00000000	BCH decode result of 33th error bit for codeword 0
NANDC_BCHDE0_34	0x0428	W	0x00000000	BCH decode result of 3th error bit for codeword 0
NANDC_BCHDE0_35	0x042c	W	0x00000000	BCH decode result of 35th error bit for codeword 0
NANDC_BCHDE0_36	0x0430	W	0x00000000	BCH decode result of 36th error bit for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_37	0x0434	W	0x00000000	BCH decode result of 37th error bit for codeword 0
NANDC_BCHDE0_38	0x0438	W	0x00000000	BCH decode result of 38th error bit for codeword 0
NANDC_BCHDE0_39	0x043c	W	0x00000000	BCH decode result of 39th error bit for codeword 0
NANDC_BCHDE0_40	0x0440	W	0x00000000	BCH decode result of 40th error bit for codeword 0
NANDC_BCHDE0_41	0x0444	W	0x00000000	BCH decode result of 41th error bit for codeword 0
NANDC_BCHDE0_42	0x0448	W	0x00000000	BCH decode result of 42th error bit for codeword 0
NANDC_BCHDE0_43	0x044c	W	0x00000000	BCH decode result of 43th error bit for codeword 0
NANDC_BCHDE0_44	0x0450	W	0x00000000	BCH decode result of 44th error bit for codeword 0
NANDC_BCHDE0_45	0x0454	W	0x00000000	BCH decode result of 45th error bit for codeword 0
NANDC_BCHDE0_46	0x0458	W	0x00000000	BCH decode result of 46th error bit for codeword 0
NANDC_BCHDE0_47	0x045c	W	0x00000000	BCH decode result of 47th error bit for codeword 0
NANDC_BCHDE0_48	0x0460	W	0x00000000	BCH decode result of 48th error bit for codeword 0
NANDC_BCHDE0_49	0x0464	W	0x00000000	BCH decode result of 49th error bit for codeword 0
NANDC_BCHDE0_50	0x0468	W	0x00000000	BCH decode result of 50th error bit for codeword 0
NANDC_BCHDE0_51	0x046c	W	0x00000000	BCH decode result of 51th error bit for codeword 0
NANDC_BCHDE0_52	0x0470	W	0x00000000	BCH decode result of 52th error bit for codeword 0
NANDC_BCHDE0_53	0x0474	W	0x00000000	BCH decode result of 53th error bit for codeword 0
NANDC_BCHDE0_54	0x0478	W	0x00000000	BCH decode result of 54th error bit for codeword 0
NANDC_BCHDE0_55	0x047c	W	0x00000000	BCH decode result of 55th error bit for codeword 0
NANDC_BCHDE0_56	0x0480	W	0x00000000	BCH decode result of 56th error bit for codeword 0
NANDC_BCHDE0_57	0x0484	W	0x00000000	BCH decode result of 57th error bit for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_58	0x0488	W	0x00000000	BCH decode result of 58th error bit for codeword 0
NANDC_BCHDE0_59	0x048c	W	0x00000000	BCH decode result of 59th error bit for codeword 0
NANDC_BCHDE1_24	0x0490	W	0x00000000	BCH decode result of 24th error bit for codeword 1
NANDC_BCHDE1_25	0x0494	W	0x00000000	BCH decode result of 25th error bit for codeword 1
NANDC_BCHDE1_26	0x0498	W	0x00000000	BCH decode result of 26th error bit for codeword 1
NANDC_BCHDE1_27	0x049c	W	0x00000000	BCH decode result of 27th error bit for codeword 1
NANDC_BCHDE1_28	0x04a0	W	0x00000000	BCH decode result of 28th error bit for codeword 1
NANDC_BCHDE1_29	0x04a4	W	0x00000000	BCH decode result of 29th error bit for codeword 1
NANDC_BCHDE1_30	0x04a8	W	0x00000000	BCH decode result of 30th error bit for codeword 1
NANDC_BCHDE1_31	0x04ac	W	0x00000000	BCH decode result of 31th error bit for codeword 1
NANDC_BCHDE1_32	0x04b0	W	0x00000000	BCH decode result of 32th error bit for codeword 1
NANDC_BCHDE1_33	0x04b4	W	0x00000000	BCH decode result of 33th error bit for codeword 1
NANDC_BCHDE1_34	0x04b8	W	0x00000000	BCH decode result of 34th error bit for codeword 1
NANDC_BCHDE1_35	0x04bc	W	0x00000000	BCH decode result of 35th error bit for codeword 1
NANDC_BCHDE1_36	0x04c0	W	0x00000000	BCH decode result of 3th error bit for codeword 1
NANDC_BCHDE1_37	0x04c4	W	0x00000000	BCH decode result of 37th error bit for codeword 1
NANDC_BCHDE1_38	0x04c8	W	0x00000000	BCH decode result of 38th error bit for codeword 1
NANDC_BCHDE1_39	0x04cc	W	0x00000000	BCH decode result of 39th error bit for codeword 1
NANDC_BCHDE1_40	0x04d0	W	0x00000000	BCH decode result of 40th error bit for codeword 1
NANDC_BCHDE1_41	0x04d4	W	0x00000000	BCH decode result of 41th error bit for codeword 1
NANDC_BCHDE1_42	0x04d8	W	0x00000000	BCH decode result of 42th error bit for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE1_43	0x04dc	W	0x00000000	BCH decode result of 43th error bit for codeword 1
NANDC_BCHDE1_44	0x04e0	W	0x00000000	BCH decode result of 44th error bit for codeword 1
NANDC_BCHDE1_45	0x04e4	W	0x00000000	BCH decode result of 45th error bit for codeword 1
NANDC_BCHDE1_46	0x04e8	W	0x00000000	BCH decode result of 46th error bit for codeword 1
NANDC_BCHDE1_47	0x04ec	W	0x00000000	BCH decode result of 47th error bit for codeword 1
NANDC_BCHDE1_48	0x04f0	W	0x00000000	BCH decode result of 48th error bit for codeword 1
NANDC_BCHDE1_49	0x04f4	W	0x00000000	BCH decode result of 49th error bit for codeword 1
NANDC_BCHDE1_50	0x04f8	W	0x00000000	BCH decode result of 50th error bit for codeword 1
NANDC_BCHDE1_51	0x04fc	W	0x00000000	BCH decode result of 51th error bit for codeword 1
NANDC_BCHDE1_52	0x0500	W	0x00000000	BCH decode result of 52th error bit for codeword 1
NANDC_BCHDE1_53	0x0504	W	0x00000000	BCH decode result of 53th error bit for codeword 1
NANDC_BCHDE1_54	0x0508	W	0x00000000	BCH decode result of 54th error bit for codeword 1
NANDC_BCHDE1_55	0x050c	W	0x00000000	BCH decode result of 55th error bit for codeword 1
NANDC_BCHDE1_56	0x0510	W	0x00000000	BCH decode result of 56th error bit for codeword 1
NANDC_BCHDE1_57	0x0514	W	0x00000000	BCH decode result of 57th error bit for codeword 1
NANDC_BCHDE1_58	0x0518	W	0x00000000	BCH decode result of 58th error bit for codeword 1
NANDC_BCHDE1_59	0x051c	W	0x00000000	BCH decode result of 59th error bit for codeword 1
NANDC_BCHST8	0x0520	W	0x00000000	BCH Status Register For Codeword 16~17
NANDC_BCHST9	0x0524	W	0x00000000	BCH Status Register For Codeword 18~19
NANDC_BCHST10	0x0528	W	0x00000000	BCH Status Register For Codeword 20~21
NANDC_BCHST11	0x052c	W	0x00000000	BCH Status Register For Codeword 22~23

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Name	Offset	Size	Reset Value	Description
NANDC_BCHST12	0x0530	W	0x00000000	BCH Status Register For Codeword 24~25
NANDC_BCHST13	0x0534	W	0x00000000	BCH Status Register For Codeword 26~27
NANDC_BCHST14	0x0538	W	0x00000000	BCH Status Register For Codeword 28~29
NANDC_BCHST15	0x053c	W	0x00000000	BCH Status Register For Codeword 30~31
NANDC_RANDMZ_SEED13_0	0x0600	W	0x00000000	Seed 0 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_1	0x0604	W	0x00000000	Seed 1 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_2	0x0608	W	0x00000000	Seed 2 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_3	0x060c	W	0x00000000	Seed 3 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_4	0x0610	W	0x00000000	Seed 4 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_5	0x0614	W	0x00000000	Seed 5 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_6	0x0618	W	0x00000000	Seed 6 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_7	0x061c	W	0x00000000	Seed 7 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_8	0x0620	W	0x00000000	Seed 8 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_9	0x0624	W	0x00000000	Seed 9 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_10	0x0628	W	0x00000000	Seed 10 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_11	0x062c	W	0x00000000	Seed 11 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_12	0x0630	W	0x00000000	Seed 12 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_13	0x0634	W	0x00000000	Seed 13 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_14	0x0638	W	0x00000000	Seed 14 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED13_15	0x063c	W	0x00000000	Seed 15 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_0	0x0640	W	0x00000000	Seed 0 for Toshiba 17 Power Polynomial Randomizer

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Name	Offset	Size	Reset Value	Description
NANDC_RANDMZ_SEED17_1	0x0644	W	0x00000000	Seed 1 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_2	0x0648	W	0x00000000	Seed 2 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_3	0x064c	W	0x00000000	Seed 3 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_4	0x0650	W	0x00000000	Seed 4 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_5	0x0654	W	0x00000000	Seed 5 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_6	0x0658	W	0x00000000	Seed 6 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_7	0x065c	W	0x00000000	Seed 7 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_8	0x0660	W	0x00000000	Seed 8 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_9	0x0664	W	0x00000000	Seed 9 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_10	0x0668	W	0x00000000	Seed 10 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_11	0x066c	W	0x00000000	Seed 11 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_12	0x0670	W	0x00000000	Seed 12 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_13	0x0674	W	0x00000000	Seed 13 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_14	0x0678	W	0x00000000	Seed 14 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED17_15	0x067c	W	0x00000000	Seed 15 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_0	0x0680	W	0x00000000	Seed 0 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_1	0x0684	W	0x00000000	Seed 1 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_2	0x0688	W	0x00000000	Seed 2 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_3	0x068c	W	0x00000000	Seed 3 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_4	0x0690	W	0x00000000	Seed 4 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_5	0x0694	W	0x00000000	Seed 5 for Toshiba 19 Power Polynomial Randomizer

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Name	Offset	Size	Reset Value	Description
NANDC_RANDMZ_SEED19_6	0x0698	W	0x00000000	Seed 6 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_7	0x069c	W	0x00000000	Seed 7 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_8	0x06a0	W	0x00000000	Seed 8 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_9	0x06a4	W	0x00000000	Seed 9 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_10	0x06a8	W	0x00000000	Seed 10 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_11	0x06ac	W	0x00000000	Seed 11 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_12	0x06b0	W	0x00000000	Seed 12 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_13	0x06b4	W	0x00000000	Seed 13 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_14	0x06b8	W	0x00000000	Seed 14 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED19_15	0x06bc	W	0x00000000	Seed 15 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_0	0x06c0	W	0x00000000	Seed 0 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_1	0x06c4	W	0x00000000	Seed 1 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_2	0x06c8	W	0x00000000	Seed 2 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_3	0x06cc	W	0x00000000	Seed 3 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_4	0x06d0	W	0x00000000	Seed 4 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_5	0x06d4	W	0x00000000	Seed 5 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_6	0x06d8	W	0x00000000	Seed 6 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_7	0x06dc	W	0x00000000	Seed 7 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_8	0x06e0	W	0x00000000	Seed 8 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_9	0x06e4	W	0x00000000	Seed 9 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_10	0x06e8	W	0x00000000	Seed 10 for Toshiba 23 Power Polynomial Randomizer

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Name	Offset	Size	Reset Value	Description
NANDC_RANDMZ_SEED23_11	0x06ec	W	0x00000000	Seed 11 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_12	0x06f0	W	0x00000000	Seed 12 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_13	0x06f4	W	0x00000000	Seed 13 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_14	0x06f8	W	0x00000000	Seed 14 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEED23_15	0x06fc	W	0x00000000	Seed 15 for Toshiba 23 Power Polynomial Randomizer

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

9.4.3 Detail Register Description

NANDC_FMCTL
Address: Operational Base + offset (0x0000)
Flash Interface Control Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	syn_mode Toggle enable signal, 1 active. 0: ONFI synchronous flash. 1: Toggle synchronous flash.
14	RW	0x0	syn_clken Synchronous flash clock enable signal, 1 active. Only available in Synchronous Mode. 0: flash clock is disabled. 1: flash clock is enabled.
13	RW	0x0	tm Timing mode indication. 0: Asynchronous Mode. 1: Synchronous Mode (Toggle or ONFI Synchronous).
12	RW	0x0	dwidth Flash data bus width indication. 0: 8bits, active in both Asynchronous Mode flash and Synchronous Mode flash. 1: 16bits, active only in Asynchronous Mode flash.
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RO	0x1	frdy Flash ready/busy indicate signal. 0: flash is busy. 1: flash is ready. This bit is the sample of the pin of R/Bn.
8	RW	0x0	wp Flash write protect. 0: flash program/erase disabled. 1: flash program/erase enabled. This bit is output to the pin of WPn.
7	RW	0x0	fcs7 Flash memory chip 7 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
6	RW	0x0	fcs6 Flash memory chip 6 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
5	RW	0x0	fcs5 Flash memory chip 5 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
4	RW	0x0	fcs4 Flash memory chip 4 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
3	RW	0x0	fcs3 Flash memory chip 3 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
2	RW	0x0	fcs2 Flash memory chip 2 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
1	RW	0x0	fcs1 Flash memory chip 1 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
0	RW	0x0	fcs0 Flash memory chip 0 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.

NANDC_FMWAIT_ASYN
Address: Operational Base + offset (0x0004)

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Flash Timing Control Register For Asynchronous Timing

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	fmw_dly_en fmw_dly enable signal,1 active.
29:24	RW	0x3f	fmw_dly The number of delay cycle between two codeword transmission.
23:18	RO	0x0	reserved
17:12	RW	0x3f	csrw When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the falling edge of CSn to the falling edge of RDn or WRn. The min value of csrw is 0.
11	RO	0x0	reserved
10:5	RW	0x3f	rwpw When in Asynchronous mode or Toggle address/command mode, this field specifies the width of RDn or WRn in processor clock cycles, 0x0<=rwpw<=0x3f.
4:0	RW	0x1f	rwcs When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the rising edge of RDn or WRn to the rising edge of CSn, 0x0<=rwcs<=0x1f.

NANDC_FLCTL

Address: Operational Base + offset (0x0008)

Internal Transfer Control Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	low_power Nandc low power control 0: normal mode 1: low power mode
27:22	RW	0x00	page_num Transmission codeword number in internal DMA mode when bus-mode is master-mode 1~32: 1~32 codeword. default: not support. Notes: a. Only active in internal DMA mode b. Only active when bus-mode is master-mode

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Bit	Attr	Reset Value	Description
21	RW	0x0	page_size Transmission codeword size in internal DMA mode 0: 1024bytes/codeword 1: 512bytes/codeword
20	RO	0x1	tr_rdy Internal DMA transmission ready indication. 0: internal DMA transmission is busy 1: internal DMA transmission is ready When reading flash, tr_rdy should not be set to 1 until all data transmission and correct finished. When programing flash, tr_rdy should not be set to 1 until all data transmission finished. Notes: Only active in internal DMA mode.
19	RO	0x0	reserved
18:12	RW	0x00	spare_size Spare byte number when lba_en=1. 0<= spare_size<=109. When spare_size>=109, it is treated as 0. Notes: The spare_size must be even number when flash is ONFI Synchronous Flash or Aynchronous Flash with 16bits data width.
11	RW	0x0	lba_en LBA mode indication, 1 active. 0: NO-LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by BCHCTL[16](bchpage), spare size is 32/46/74 bytes or 109 bytes determined by BCHCTL[4] and BCHCTL[18]. 1: LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by FLCTL[21](page_size), spare size is determined by FLCTL[17:12](spare_size). Notes: a. When lba_en is active, BCH CODEC should be disabled, spare_size and page_size are configurable. b. When lba_en is active, cor_able is inactive.

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Bit	Attr	Reset Value	Description
10	RW	0x0	cor_able Auto correct enable indication, 1 active. 0: auto correct disable 1: auto correct enable Notes: a. Only active in internal DMA mode. b. lba_en is prior to cor_able. When lba_en=1, cor_able is ignored.
9:8	RO	0x0	reserved
7	RW	0x0	flash_st_mod Mode for NandC to start internal data transmission in internal DMA mode. 0: busy mode: hardware should not start internal data transmission until flash is ready even flash_st is asserted. 1: ready mode: hardware should start internal data transmission directly when flash_st is asserted. Notes: Only active in internal DMA mode.
6:5	RW	0x0	tr_count Transmission codeword number in internal DMA mode when bus-mode is slave-mode 00: 0 codeword need transferred 01: 1 codeword need transferred 10: 2 codeword need transferred 11: not supported Notes: a. Only active in internal DMA mode. b. Only active when bus-mode is slave-mode.
4	RW	0x0	st_addr Start buffer address. 0: start transfer from sram0 1: start transfer from sram1 Notes: Only active in internal DMA mode.
3	RW	0x0	bypass NandC internal DMA bypass indication. 0: bypass the internal DMA, data are transferred to/from flash by direct path. 1: internal DMA active, data are transferred to/from flash by internal DMA.

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Bit	Attr	Reset Value	Description
2	RW	0x0	flash_st Start signal for NandC to transfer data between flash and internal buffer in internal DMA mode. When asserted, it will auto cleared. 0: not start transmission 1: start transmission Notes: Only active in internal DMA mode
1	RW	0x0	flash_rdn Indicate data flow direction. 0: NandC read data from flash. 1: NandC write data to flash
0	RW	0x0	flash_rst NandC software reset indication. When asserted, it will auto cleared. 0: not software reset 1: software reset Notes: flash_rst is prior to flash_st

NANDC_BCHCTL
Address: Operational Base + offset (0x000c)
BCH Control Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:19	RW	0x00	bchthres BCH error number threshold
18	RW	0x0	bchmode1 High bit of BCH mode selection for 40bitBCH or 60bitBCH. BchMode=bchmode1, bchmode0: 00: 16bitBCH 01: 24bitBCH 10: 40bitBCH 11: 60bitBCH
17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	bchpage The data size indication when BCH is active. 0: 1024 bytes, all the 1024 bytes data in codeword are valid data to be transferred. 1: 512 bytes, higher 512bytes are valid, and lower 512bytes are invalid and stuffed with 0xff. Notes: a. Only active when data transferred in internal DMA mode. b. Only active for asynchronous flash.
15:8	RW	0x00	addr BCH active range selection. BCH should be active when access in range address.
7:5	RW	0x0	region BCH active region selection indication. 000: Flash memory 0 region (flash 0) 001: Flash memory 1 region (flash 1) 010: Flash memory 2 region (flash 2) 011: Flash memory 3 region (flash 3) 100: Flash memory 4 region (flash 4) 101: Flash memory 5 region (flash 5) 110: Flash memory 6 region (flash 6) 111: Flash memory 7 region (flash 7)
4	RW	0x0	bchmode0 BCH mode selection indication. BCH mode is determined by both bchmode0 and bchmode1,detailed information is showed in BCHCTL[18].
3	RW	0x1	bchepd BCH encoder/decoder power down indication. 0: BCH encoder/decoder working. 1: BCH encoder/decoder not working.
2	RW	0x0	mode_addrcare BCH address care mode selection indication. 0: address care. 1: address not care. Notes: This bit is just active for data transmission in bypass mode, but not for command and address transmission.
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	bchrst BCH software reset indication, When asserted, it will auto cleared. 0: not software reset 1: software reset Notes: a. BCH Decoder should be software reset before decode begin. b. bch software reset should be used with nandc software reset at the same time.

NANDC_MTRANS_CFG
Address: Operational Base + offset (0x0010)
Bus Transfer Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	W1C	0x0	ahb_rst ahb master interface software reset, auto cleared
14	RW	0x0	fl_pwd Flash power down indication, 1 active. 0: Flash power on, data transferred through master interface is data that to be written into or read from flash. 1: Flash power down, data transferred through master interface is not data that to be written into or read from flash. NandC is just used as DMA for external memory and internal memory.
13:9	RW	0x00	incr_num AHB Master incr num indication. incr_num=1~16. When burst=001, software should configure incr_num. Notes: Only active for master-mode.
8:6	RW	0x7	burst AHB Master burst type indication: 000 : Single transfer 011 : 4-beat burst 101 : 8-beat Burst 111 : 16-beat burst default : not supported Notes: Only active for master-mode.

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Bit	Attr	Reset Value	Description
5:3	RW	0x2	hsize AHB Master data size indication: 000 : 8 bits 001 : 16 bits 010 : 32 bits default : not supported Notes: Only active for master-mode.
2	RW	0x0	bus_mode Bus interface selection. 0: Slave interface, flash data is transferred through slave interface 1: Master interface, flash data is transferred through master interface
1	RW	0x0	ahb_wr Data transfer direction through master interface. 0: read direction(internal memory ->external memory) 1: write direction (internal memory->external memory) Notes: a. Only active for master-mode. b. When read flash(flash_rdn=0), ahb_wr=1; when program flash(flash_rdn=1), ahb_wr=0.
0	W1C	0x0	ahb_wr_st Start indication for loading data from external memory to internal memory or storing data from internal memory to external memory through master. When asserted, it will auto cleared. Notes: a. Only active for master-mode and fl_pwd=1. b. When fl_pwd=0, flash is active, NandC start to transfer data through master interface if flash_st=1 c. When fl_pwd=1, flash is not active, NandC start to transfer data through master interface if ahb_wr_st=1

NANDC_MTRANS_SADDR0

Address: Operational Base + offset (0x0014)

Start Address Register For Page Data Transmission

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr0 Start address for page data transmision. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_SADDR1
Address: Operational Base + offset (0x0018)
Start Address Register For Spare Data Transmission

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr1 Start address for spare data. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_STAT
Address: Operational Base + offset (0x001c)
Bus Transfer Status Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RO	0x00	mtrans_cnt finished counter for codeword transmission through Master interface Notes: Only active for master-mode.
15:0	RO	0x0000	bus_err Bus error indication for codeword0~15. [0] : bus error for codeword 0 …… [15] : bus error for codeword 15 Notes: Only active for master-mode.

NANDC_BCHST0
Address: Operational Base + offset (0x0020)
BCH Status Register For Codeword 0~1

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum1_h1 Highest bit of err_hnum1
29	RO	0x0	err_tnum1_h1 Highest bit of err_tnum1

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Bit	Attr	Reset Value	Description
28	RO	0x0	err_hnum0_h1 Highest bit of err_hnum0
27	RO	0x0	err_tnum0_h1 Highest bit of err_tnum0
26	RO	0x1	bchrdy Ready indication for bch encoder/decoder, 1 active. 0: bch encoder/decoder is busy 1: bch encoder/decoder is ready
25:21	RO	0x00	err_hnum1_l5 Lower 5 bits of number of error bits found in first 512bytes of 1st backup codeword
20:16	RO	0x00	err_tnum1_l5 Lower 5 bits of number of error bits found in 1st backup codeword
15	RO	0x0	fail1 Indication for the 1st backup codeword decoded failed or not. 0: decode successfully 1: decode fail
14	RO	0x0	done1 Indication for finishing decoding the 1st backup codeword 0: not finished 1: finished
13	RO	0x0	errf1 Indication for error found in 1st backup codeword. 0: no error 1: error found
12:8	RO	0x00	err_hnum0_l5 Lower 5 bits of number of error bits found in first 512bytes of current backup codeword
7:3	RO	0x00	err_tnum0_l5 Lower 5 bits of number of error bits found in current backup codeword
2	RO	0x0	fail0 Indication for current backup codeword decode failed or not 0: decode successfully 1: decode fail

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Bit	Attr	Reset Value	Description
1	RO	0x0	done0 Indication for finishing decoding the current backup codeword. 0: not finished 1: finished
0	RO	0x0	errf0 Indication for error found in current backup codeword. 0: no error 1: error found

NANDC_BCHST1
Address: Operational Base + offset (0x0024)
BCH Status Register For Codeword 2~3

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum3_h1 Highest bit of err_hnum3
29	RO	0x0	err_tnum3_h1 Highest bit of err_tnum3
28	RO	0x0	err_hnum2_h1 Highest bit of err_hnum2
27	RO	0x0	err_tnum2_h1 Highest bit of err_tnum2
26	RO	0x0	reserved
25:21	RO	0x00	err_hnum3_l5 Lower 5 bits of number of error bits found in first 512bytes of 3th backup codeword
20:16	RO	0x00	err_tnum3_l5 Lower 5 bits of number of error bits found in 3th backup codeword
15	RO	0x0	fail3 Indication for the 3th backup codeword decoded failed or not. 0: decode successfully 1: decode fail
14	RO	0x0	done3 Indication for finishing decoding the 3th backup codeword 0: not finished 1: finished

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Bit	Attr	Reset Value	Description
13	RO	0x0	errf3 Indication for error found in 3th backup codeword. 0: no error 1: error found
12:8	RO	0x00	err_hnum2_l5 Lower 5 bits of number of error bits found in first 512bytes of 2th backup codeword
7:3	RO	0x00	err_tnum2_l5 Lower 5 bits of number of error bits found in 2th backup codeword
2	RO	0x0	fail2 Indication for 2th backup codeword decode failed or not 0: decode successfully 1: decode fail
1	RO	0x0	done2 Indication for finishing decoding the 2th backup codeword. 0: not finished 1: finished
0	RO	0x0	errf2 Indication for error found in 2th backup codeword. 0: no error 1: error found

NANDC_BCHST2
Address: Operational Base + offset (0x0028)
BCH Status Register For Codeword 4~5

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd4_cwd5 BCHST information for 4th and 5th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST3
Address: Operational Base + offset (0x002c)
BCH Status Register For Codeword 6~7

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd6_cwd7 BCHST information for 6th and 7th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST4
Address: Operational Base + offset (0x0030)
BCH Status Register For Codeword 8~9

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd8_cwd9 BCHST information for 8th and 9th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST5
Address: Operational Base + offset (0x0034)
BCH Status Register For Codeword 10~11

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd10_cwd11 BCHST information for 10th and 11th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST6
Address: Operational Base + offset (0x0038)
BCH Status Register For Codeword 12~13

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd12_cwd13 BCHST information for 12th and 13th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST7
Address: Operational Base + offset (0x003c)
BCH Status Register For Codeword 14~15

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd14_cwd15 BCHST information for 14th and 15th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHLOC0
Address: Operational Base + offset (0x0040)
BCH Error Bit Location Number Register For Codeword 0~5

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc5_l5 Lower 5 bits of number of 8bit error location in 5th backup codeword
24:20	RO	0x00	err_loc4_l5 Lower 5 bits of number of 8bit error location in 4th backup codeword
19:15	RO	0x00	err_loc3_l5 Lower 5 bits of number of 8bit error location in 3rd backup codeword
14:10	RO	0x00	err_loc2_l5 Lower 5 bits of number of 8bit error location in 2nd backup codeword
9:5	RO	0x00	err_loc1_l5 Lower 5 bits of number of 8bit error location in 1st backup codeword
4:0	RO	0x00	err_loc0_l5 Lower 5 bits of number of 8bit error location in current backup codeword

NANDC_BCHLOC1
Address: Operational Base + offset (0x0044)
BCH Error Bit Location Number Register For Codeword 6~11

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc11_l5 Lower 5 bits of number of 8bit error location in 11th backup codeword
24:20	RO	0x00	err_loc10_l5 Lower 5 bits of number of 8bit error location in 10th backup codeword
19:15	RO	0x00	err_loc9_l5 Lower 5 bits of number of 8bit error location in 9th backup codeword

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Bit	Attr	Reset Value	Description
14:10	RO	0x00	err_loc8_l5 Lower 5 bits of number of 8bit error location in 8th backup codeword
9:5	RO	0x00	err_loc7_l5 Lower 5 bits of number of 8bit error location in 7th backup codeword
4:0	RO	0x00	err_loc6_l5 Lower 5 bits of number of 8bit error location in 6th backup codeword

NANDC_BCHLOC2
Address: Operational Base + offset (0x0048)
BCH Error Bit Location Number Register For Codeword 12~17

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc17_l5 Lower 5 bits of number of 8bit error location in 17th backup codeword
24:20	RO	0x00	err_loc16_l5 Lower 5 bits of number of 8bit error location in 16th backup codeword
19:15	RO	0x00	err_loc15_l5 Lower 5 bits of number of 8bit error location in 15th backup codeword
14:10	RO	0x00	err_loc14_l5 Lower 5 bits of number of 8bit error location in 14th backup codeword
9:5	RO	0x00	err_loc13_l5 Lower 5 bits of number of 8bit error location in 13th backup codeword
4:0	RO	0x00	err_loc12_l5 Lower 5 bits of number of 8bit error location in 12th backup codeword

NANDC_BCHLOC3
Address: Operational Base + offset (0x004c)
BCH Error Bit Location Number Register For Codeword 24~29

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc23_l5 Lower 5 bits of number of 8bit error location in 23th backup codeword

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Bit	Attr	Reset Value	Description
24:20	RO	0x00	err_loc22_l5 Lower 5 bits of number of 8bit error location in 22th backup codeword
19:15	RO	0x00	err_loc21_l5 Lower 5 bits of number of 8bit error location in 21th backup codeword
14:10	RO	0x00	err_loc20_l5 Lower 5 bits of number of 8bit error location in 20th backup codeword
9:5	RO	0x00	err_loc19_l5 Lower 5 bits of number of 8bit error location in 19th backup codeword
4:0	RO	0x00	err_loc18_l5 Lower 5 bits of number of 8bit error location in 18th backup codeword

NANDC_BCHLOC4
Address: Operational Base + offset (0x0050)
BCH Error Bit Location Number Register For Codeword 24~29

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc29_l5 Lower 5 bits of number of 8bit error location in 23th backup codeword
24:20	RO	0x00	err_loc28_l5 Lower 5 bits of number of 8bit error location in 22th backup codeword
19:15	RO	0x00	err_loc27_l5 Lower 5 bits of number of 8bit error location in 21th backup codeword
14:10	RO	0x00	err_loc26_l5 Lower 5 bits of number of 8bit error location in 20th backup codeword
9:5	RO	0x00	err_loc25_l5 Lower 5 bits of number of 8bit error location in 19th backup codeword
4:0	RO	0x00	err_loc24_l5 Lower 5 bits of number of 8bit error location in 18th backup codeword

NANDC_BCHLOC5
Address: Operational Base + offset (0x0054)
BCH Error Bit Location Number Register For Codeword 30~31

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:5	RO	0x00	err_loc31_l5 Lower 5 bits of number of 8bit error location in 31th backup codeword
4:0	RO	0x00	err_loc30_l5 Lower 5 bits of number of 8bit error location in 30th backup codeword

NANDC_BCHLOC6
Address: Operational Base + offset (0x0058)
Highest Bit For BCH Error Bit Location Number Register

Bit	Attr	Reset Value	Description
31	RO	0x0	err_loc31_h1 High bit for numbers of 8bit error location in 31th codeword
30	RO	0x0	err_loc30_h1 High bit for numbers of 8bit error location in 30th codeword
29	RO	0x0	err_loc29_h1 High bit for numbers of 8bit error location in 29th codeword
28	RO	0x0	err_loc28_h1 High bit for numbers of 8bit error location in 28th codeword
27	RO	0x0	err_loc27_h1 High bit for numbers of 8bit error location in 27th codeword
26	RO	0x0	err_loc26_h1 High bit for numbers of 8bit error location in 26th codeword
25	RO	0x0	err_loc25_h1 High bit for numbers of 8bit error location in 25th codeword
24	RO	0x0	err_loc24_h1 High bit for numbers of 8bit error location in 24th codeword
23	RO	0x0	err_loc23_h1 High bit for numbers of 8bit error location in 23th codeword
22	RO	0x0	err_loc22_h1 High bit for numbers of 8bit error location in 22th codeword
21	RO	0x0	err_loc21_h1 High bit for numbers of 8bit error location in 21th codeword

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Bit	Attr	Reset Value	Description
20	RO	0x0	err_loc20_h1 High bit for numbers of 8bit error location in 20th codeword
19	RO	0x0	err_loc19_h1 High bit for numbers of 8bit error location in 19th codeword
18	RO	0x0	err_loc18_h1 High bit for numbers of 8bit error location in 18th codeword
17	RO	0x0	err_loc17_h1 High bit for numbers of 8bit error location in 17th codeword
16	RO	0x0	err_loc16_h1 High bit for numbers of 8bit error location in 16th codeword
15	RO	0x0	err_loc15_h1 High bit for numbers of 8bit error location in 15th codeword
14	RO	0x0	err_loc14_h1 High bit for numbers of 8bit error location in 14th codeword
13	RO	0x0	err_loc13_h1 High bit for numbers of 8bit error location in 13th codeword
12	RO	0x0	err_loc12_h1 High bit for numbers of 8bit error location in 12th codeword
11	RO	0x0	err_loc11_h1 High bit for numbers of 8bit error location in 11th codeword
10	RO	0x0	err_loc10_h1 High bit for numbers of 8bit error location in 10th codeword
9	RO	0x0	err_loc9_h1 High bit for numbers of 8bit error location in 9th codeword
8	RO	0x0	err_loc8_h1 High bit for numbers of 8bit error location in 8th codeword
7	RO	0x0	err_loc7_h1 High bit for numbers of 8bit error location in 7th codeword
6	RO	0x0	err_loc6_h1 High bit for numbers of 8bit error location in 6th codeword

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Bit	Attr	Reset Value	Description
5	RO	0x0	err_loc5_h1 High bit for numbers of 8bit error location in 5th codeword
4	RO	0x0	err_loc4_h1 High bit for numbers of 8bit error location in 4th codeword
3	RO	0x0	err_loc3_h1 High bit for numbers of 8bit error location in 3th codeword
2	RO	0x0	err_loc2_h1 High bit for numbers of 8bit error location in 2th codeword
1	RO	0x0	err_loc1_h1 High bit for numbers of 8bit error location in 1th codeword
0	RO	0x0	err_loc0_h1 High bit for numbers of 8bit error location in 0th codeword

NANDC_BCHDE0_0
Address: Operational Base + offset (0x0070)
BCH decode result of 0th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:8	RO	0x000	offset The offset byte address of the error bit. The value is 11bit, which is the byte offset address in the codeword. The address can be divided into different part for different use, showed as follows. 0 ~1023: page data 1024~1027: system information 1028~1055: bch information for 16bitBCH 1028~1069: bch information for 24bitBCH 1028~1097: bch information for 40bitBCH 1028~1132: bch information for 60bitBCH
7:0	RO	0x00	err_val The error value of corresponding error byte

NANDC_BCHDE0_1
Address: Operational Base + offset (0x0074)
BCH decode result of 1th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_1 decode result of 1th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_2
Address: Operational Base + offset (0x0078)
BCH decode result of 2th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_2 decode result of 2th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_3
Address: Operational Base + offset (0x007c)
BCH decode result of 3th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_3 decode result of 3th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_4
Address: Operational Base + offset (0x0080)
BCH decode result of 4th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_4 decode result of 4th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_5

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Address: Operational Base + offset (0x0084)
BCH decode result of 5th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_5 decode result of 5th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_6
Address: Operational Base + offset (0x0088)
BCH decode result of 6th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_6 decode result of 6th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_7
Address: Operational Base + offset (0x008c)
BCH decode result of 7th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_7 decode result of 7th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_8
Address: Operational Base + offset (0x0090)
BCH decode result of 8th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_8 decode result of 8th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_9
Address: Operational Base + offset (0x0094)
BCH decode result of 9th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_9 decode result of 9th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_10
Address: Operational Base + offset (0x0098)
BCH decode result of 10th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_10 decode result of 10th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_11
Address: Operational Base + offset (0x009c)
BCH decode result of 11th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_11 decode result of 11th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_12
Address: Operational Base + offset (0x00a0)
BCH decode result of 12th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_12 decode result of 12th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_13
Address: Operational Base + offset (0x00a4)
BCH decode result of 13th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_13 decode result of 13th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_14
Address: Operational Base + offset (0x00a8)
BCH decode result of 14th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_14 decode result of 14th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_15
Address: Operational Base + offset (0x00ac)
BCH decode result of 15th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_15 decode result of 15th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_16

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Address: Operational Base + offset (0x00b0)
BCH decode result of 16th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_16 decode result of 16th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_17
Address: Operational Base + offset (0x00b4)
BCH decode result of 17th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_17 decode result of 17th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_18
Address: Operational Base + offset (0x00b8)
BCH decode result of 18th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_18 decode result of 18th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_19
Address: Operational Base + offset (0x00bc)
BCH decode result of 19th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_19 decode result of 1th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_20
Address: Operational Base + offset (0x00c0)
BCH decode result of 20th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_20 decode result of 20th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_21
Address: Operational Base + offset (0x00c4)
BCH decode result of 21th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_21 decode result of 21th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_22
Address: Operational Base + offset (0x00c8)
BCH decode result of 22th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_22 decode result of 22th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_23
Address: Operational Base + offset (0x00cc)
BCH decode result of 23th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_23 decode result of 23th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE1_0
Address: Operational Base + offset (0x00d0)
BCH decode result of 0th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:8	RO	0x000	offset The offset byte address of the error bit. The value is 11bit, which is the byte offset address in the codeword. The address can be divided into different part for different use, showed as follows. 0 ~1023: page data 1024~1027: system information 1028~1055: bch information for 16bitBCH 1028~1069: bch information for 24bitBCH 1028~1097: bch information for 40bitBCH 1028~1132: bch information for 60bitBCH
7:0	RO	0x00	err_val The error value of corresponding error byte

NANDC_BCHDE1_1
Address: Operational Base + offset (0x00d4)
BCH decode result of 1th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_1 decode result of 1th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_2
Address: Operational Base + offset (0x00d8)
BCH decode result of 2th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_2 decode result of 2th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_3
Address: Operational Base + offset (0x00dc)
BCH decode result of 3th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_3 decode result of 3th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_4
Address: Operational Base + offset (0x00e0)
BCH decode result of 4th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_4 decode result of 4th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_5
Address: Operational Base + offset (0x00e4)
BCH decode result of 5th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_5 decode result of 5th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_6

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Address: Operational Base + offset (0x00e8)
BCH decode result of 6th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_6 decode result of 6th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_7
Address: Operational Base + offset (0x00ec)
BCH decode result of 7th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_7 decode result of 7th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_8
Address: Operational Base + offset (0x00f0)
BCH decode result of 8th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_8 decode result of 8th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_9
Address: Operational Base + offset (0x00f4)
BCH decode result of 9th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_9 decode result of 9th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_10
Address: Operational Base + offset (0x00f8)
BCH decode result of 10th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_10 decode result of 10th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_11
Address: Operational Base + offset (0x00fc)
BCH decode result of 11th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_11 decode result of 11th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_12
Address: Operational Base + offset (0x0100)
BCH decode result of 12th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_12 decode result of 12th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_13
Address: Operational Base + offset (0x0104)
BCH decode result of 13th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_13 decode result of 13th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_14
Address: Operational Base + offset (0x0108)
BCH decode result of 14th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_14 decode result of 14th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_15
Address: Operational Base + offset (0x010c)
BCH decode result of 15th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_15 decode result of 15th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_16
Address: Operational Base + offset (0x0110)
BCH decode result of 16th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_16 decode result of 16th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_17

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Address: Operational Base + offset (0x0114)
BCH decode result of 17th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_17 decode result of 17th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_18
Address: Operational Base + offset (0x0118)
BCH decode result of 1th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_18 decode result of 18th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_19
Address: Operational Base + offset (0x011c)
BCH decode result of 19th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_19 decode result of 19th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_20
Address: Operational Base + offset (0x0120)
BCH decode result of 20th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_20 decode result of 20th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_21
Address: Operational Base + offset (0x0124)
BCH decode result of 21th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_21 decode result of 21th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_22
Address: Operational Base + offset (0x0128)
BCH decode result of 22th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_22 decode result of 22th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_23
Address: Operational Base + offset (0x012c)
BCH decode result of 23th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_23 decode result of 23th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_DLL_CTL_REG0
Address: Operational Base + offset (0x0130)
DLL Control Register 0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x7f	dll_dqs_dly_bypass Holds the read DQS delay setting when the DLL is operating in bypass mode.

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Bit	Attr	Reset Value	Description
15:8	RW	0x7f	dll_dqs_dly Holds the read DQS delay setting when the DLL is operating in normal mode. Typically, this value is 1/4 of a clock cycle. Each increment of this field represents 1/128th of a clock cycle.
7:0	RW	0x05	dll_start_point DLL Start Point Control. This value is loaded into the DLL at initialization and is the value at which the DLL will begin searching for a lock. Each increment of this field represents 1/128th of a clock cycle.

NANDC_DLL_CTL_REG1
Address: Operational Base + offset (0x0134)
DLL Control Register 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x02	dll_incr DLL Increment Value. This sets the increment used by the DLL when searching for a lock. It is recommended keeping this field small (around 0x4) to keep the steps gradual
3:2	RW	0x0	dll_qtren Quarter flag of DLL, active in no-bypass mode. 01:1/4 fclk, dqs_dly=128. 10:1/8 fclk, dqs_dly=64. Default: dqs_dly=dll_dqs_dly(DLL_CTL_REG0[15:8]). When dll_qtr='b01 or 'b10, software not need to configure dll_dqs_dly , and hardware should delay the input signal for 1/4 or 1/8 fclk cycle time; When dll_qtr=0, software need to configure dll_dqs_dly.
1	RW	0x1	dll_bypass DLL Bypass Control, 1active 0: dll not bypass, dll_dqs_dleay= dqs_dly 1: dll bypass, dll_dqs_dleay= dll_dqs_dly_bypass
0	RW	0x0	dll_start Start signal for DLL, 1 active. Notes: It will keep high until dll disabled.

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NANDC_DLL_OBS_REG0
Address: Operational Base + offset (0x0138)
DLL Status Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:9	RO	0x01	dll_dqs_delay_value Report the delay value for the read DQS signal
8:1	RO	0x00	dll_lock_value Reports the DLL encoder value from the master DLL to the slave DLL's. The slaves use this value to set up their delays for the clk_wr and read DQS signals.
0	RO	0x0	dll_lock DLL Lock indication: 0: DLL has not locked 1: DLL is locked.

NANDC_RANDMZ_CFG
Address: Operational Base + offset (0x0150)
Randomizer Configure Register

Bit	Attr	Reset Value	Description
31	RW	0x0	randmz_en Randomizer enable indication, 1 active. 0: Randomizer active 1: Randomizer not active Notes: a. Not active when data transmission in bypass mode. b. Just active for data, but not for address and command. c. Not active when BchPage=1.
30:29	RW	0x0	randmz_mode Randomizer mode: 00- Samsung randomizer Polynomial=1+x+x^15 10- Samsung randomizer Polynomial=1+x^14+x^15 01-TOSHIBA randomizer
28:24	RW	0x00	page_offset basic seed rotation bits for every 16page
23:20	RW	0x0	cwd_offset basic seed start point for every page

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Bit	Attr	Reset Value	Description
19:0	RW	0x00000	randmz_seed when Samsung randomizer: The seed for randomizer(initial value); when Toshiba randomizer: Seed Agitation Register.

NANDC_FMWAIT_SYN
Address: Operational Base + offset (0x0158)
Flash Timing Control Register For Synchronous Timing

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:9	RW	0x00	pst Write/Read Postamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycle for Postamb- le time.
8:3	RW	0x00	pre Write/Read Preamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycle for preamble time.
2:0	RW	0x0	fclk Half hclk cycle number for flash clock for ONFI synchronous mode or Toggle data mode

NANDC_MTRANS_STAT2
Address: Operational Base + offset (0x015c)
Bus Transfer Status Register2

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	bus_err2 Bus error indication for codeword16~31. [0] : bus error for codeword 16 …… [15] : bus error for codeword 31 Notes: Only active for master-mode.

NANDC_NANDC_VER
Address: Operational Base + offset (0x0160)
Nandc Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x56363232	version Version indication for NANDC

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NANDC_LLP_CTL
Address: Operational Base + offset (0x0164)
LLP Control Register

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	llp_loc Starting address for LLI0, 64byte align
5	RW	0x0	llp_frdy Working time for FOP_WAIT_FRDY for all FOP in first LLP group: 0: FOP_WAIT_FRDY begin working when started 1: FOP_WAIT_FRDY not begin working until 16 cycles later after started
4:3	RO	0x0	reserved
2	RW	0x0	llp_rst Reset signal for LLP. When asserted, it will auto cleared.
1	RW	0x0	llp_mode 0- current LLI only has FOP 1-current LLI has both CFG and FOP
0	RW	0x0	llp_en Enable signal for LLP 0-LLP disable 1-LLP enable

NANDC_LLP_STAT
Address: Operational Base + offset (0x0168)
LLP Status Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	llp_stat latest LLI_LOC finished, 64byte align
5:2	RO	0x0	reserved
1	RO	0x0	llp_err error status for llp load or execute 0-llp is correct 1-llp is error
0	RO	0x1	llp_rdy ready status for all llp load 0-llp load is busy 1-llp load is ready

NANDC_INTEN
Address: Operational Base + offset (0x016c)
NandC Interrupt Enable Register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	llp_int_en Enable for LLP finished interrupt. 0: interrupt disable 1: interrupt enable When llp_en_en is active, an interrupt is generated if LLP operation is finished
3	RW	0x0	bchfail_int_en Enable for bch fail interrupt. 0-interrupt disable 1-interrupt enable When bchfail_int_en is active, an interrupt is generated if bch decode failed
2	RW	0x0	bcherr_int_en Enable for bch error interrupt. 0-interrupt disable 1-interrupt enable When bcherr_int_en is active, an interrupt is generated if bch decode error bit is larger than bchthres(BCHCTL[26:19])
1	RW	0x0	frdy_int_en Enable for flash_rdy interrupt 0-interrupt disable 1-interrupt enable When frdy_int_en is active, an interrupt is generated if flash R/B# changes from 0 to 1
0	RW	0x0	dma_int_en Enable for internal DMA transfer finished interrupt 0-interrupt disable 1-interrupt enable When dma_int_en is active, an interrupt is generated if page_num(FLCTL[27:22]) of flash data transfer in DMA mode is finished

NANDC_INTCLR
Address: Operational Base + offset (0x0170)
NandC Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	llp_int_clr Clear for LLP finished interrupt. When asserted, this bit will be auto cleared. 0: interrupt not cleared 1: interrupt cleared

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Bit	Attr	Reset Value	Description
3	RW	0x0	bchfail_int_clr Clear for bch decode fail interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
2	RW	0x0	bcherr_int_clr Clear for bch error interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
1	RW	0x0	frdy_int_clr Clear for flash_rdy interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
0	RW	0x0	dma_int_clr Clear for internal DMA transfer finished interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared

NANDC_INTST
Address: Operational Base + offset (0x0174)
NandC Interrupt Status Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	llp_int_stat Status for LLP finished interrupt, high active
3	RO	0x0	bchfail_int_stat Status for bch decode fail interrupt, high active
2	RO	0x0	bcherr_int_stat Status for bch error interrupt, high active
1	RO	0x0	frdy_int_stat Status for flash_rdy interrupt, high active
0	RO	0x0	dma_int_stat Status for internal DMA transfer finished interrupt, high active

NANDC_SPARE0_0
Address: Operational Base + offset (0x0200)
System Information for codeword 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 the 4th system byte of codeword 0
23:16	RW	0xff	system_2 the 3rd system byte of codeword 0
15:8	RW	0xff	system_1 the 2nd system byte of codeword 0
7:0	RW	0xff	system_0 the 1st system byte of codeword 0

NANDC_SPARE0_1
Address: Operational Base + offset (0x0204)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_2
Address: Operational Base + offset (0x0208)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_3
Address: Operational Base + offset (0x020c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_4
Address: Operational Base + offset (0x0210)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_5
Address: Operational Base + offset (0x0214)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_6
Address: Operational Base + offset (0x0218)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_7
Address: Operational Base + offset (0x021c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_8
Address: Operational Base + offset (0x0220)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_9
Address: Operational Base + offset (0x0224)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_10
Address: Operational Base + offset (0x0228)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_11
Address: Operational Base + offset (0x022c)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_0
Address: Operational Base + offset (0x0230)
System Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 the 4th system byte of codeword 1
23:16	RW	0xff	system_2 the 3rd system byte of codeword 1
15:8	RW	0xff	system_1 the 2nd system byte of codeword 1
7:0	RW	0xff	system_0 the 1st system byte of codeword 1

NANDC_SPARE1_1
Address: Operational Base + offset (0x0234)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_2
Address: Operational Base + offset (0x0238)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_3
Address: Operational Base + offset (0x023c)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_4
Address: Operational Base + offset (0x0240)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_5
Address: Operational Base + offset (0x0244)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_6
Address: Operational Base + offset (0x0248)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_7
Address: Operational Base + offset (0x024c)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_8
Address: Operational Base + offset (0x0250)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_9
Address: Operational Base + offset (0x0254)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_10
Address: Operational Base + offset (0x0258)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_11
Address: Operational Base + offset (0x025c)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_12
Address: Operational Base + offset (0x0260)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_13
Address: Operational Base + offset (0x0264)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_14
Address: Operational Base + offset (0x0268)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_15
Address: Operational Base + offset (0x026c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_16
Address: Operational Base + offset (0x0270)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_17
Address: Operational Base + offset (0x0274)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_18
Address: Operational Base + offset (0x0278)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_19
Address: Operational Base + offset (0x027c)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_20

Address: Operational Base + offset (0x0280)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_21
Address: Operational Base + offset (0x0284)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_22
Address: Operational Base + offset (0x0288)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_23
Address: Operational Base + offset (0x028c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_24
Address: Operational Base + offset (0x0290)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_25
Address: Operational Base + offset (0x0294)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_26
Address: Operational Base + offset (0x0298)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_27
Address: Operational Base + offset (0x029c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_12
Address: Operational Base + offset (0x02a0)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_13
Address: Operational Base + offset (0x02a4)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_14
Address: Operational Base + offset (0x02a8)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_15
Address: Operational Base + offset (0x02ac)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_16
Address: Operational Base + offset (0x02b0)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_17
Address: Operational Base + offset (0x02b4)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_18
Address: Operational Base + offset (0x02b8)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_19
Address: Operational Base + offset (0x02bc)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_20
Address: Operational Base + offset (0x02c0)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_21
Address: Operational Base + offset (0x02c4)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_22
Address: Operational Base + offset (0x02c8)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_23
Address: Operational Base + offset (0x02cc)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_24
Address: Operational Base + offset (0x02d0)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_25
Address: Operational Base + offset (0x02d4)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_26
Address: Operational Base + offset (0x02d8)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_27
Address: Operational Base + offset (0x02dc)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_BCHDE0_24
Address: Operational Base + offset (0x0400)
BCH decode result of 24th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_24 decode result of 24th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_25
Address: Operational Base + offset (0x0404)
BCH decode result of 25th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_25 decode result of 25th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_26
Address: Operational Base + offset (0x0408)
BCH decode result of 26th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_26 decode result of 26th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_27
Address: Operational Base + offset (0x040c)
BCH decode result of 27th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_27 decode result of 27th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_28
Address: Operational Base + offset (0x0410)
BCH decode result of 28th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_28 decode result of 28th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_29

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Address: Operational Base + offset (0x0414)
BCH decode result of 29th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_29 decode result of 29th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_30
Address: Operational Base + offset (0x0418)
BCH decode result of 30th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_30 decode result of 30th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_31
Address: Operational Base + offset (0x041c)
BCH decode result of 31th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_31 decode result of 31th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_32
Address: Operational Base + offset (0x0420)
BCH decode result of 32th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_3 decode result of 3th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_33
Address: Operational Base + offset (0x0424)
BCH decode result of 33th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_33 decode result of 33th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_34
Address: Operational Base + offset (0x0428)
BCH decode result of 3th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_34 decode result of 34th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_35
Address: Operational Base + offset (0x042c)
BCH decode result of 35th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_35 decode result of 35th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_36
Address: Operational Base + offset (0x0430)
BCH decode result of 36th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_36 decode result of 36th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_37
Address: Operational Base + offset (0x0434)
BCH decode result of 37th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_37 decode result of 37th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_38
Address: Operational Base + offset (0x0438)
BCH decode result of 38th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_38 decode result of 38th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_39
Address: Operational Base + offset (0x043c)
BCH decode result of 39th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_39 decode result of 39th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_40

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Address: Operational Base + offset (0x0440)
BCH decode result of 40th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_40 decode result of 40th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_41
Address: Operational Base + offset (0x0444)
BCH decode result of 41th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_41 decode result of 41th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_42
Address: Operational Base + offset (0x0448)
BCH decode result of 42th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_42 decode result of 4th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_43
Address: Operational Base + offset (0x044c)
BCH decode result of 43th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_43 decode result of 43th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_44
Address: Operational Base + offset (0x0450)
BCH decode result of 44th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_44 decode result of 44th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_45
Address: Operational Base + offset (0x0454)
BCH decode result of 45th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_45 decode result of 45th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_46
Address: Operational Base + offset (0x0458)
BCH decode result of 46th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_46 decode result of 46th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_47
Address: Operational Base + offset (0x045c)
BCH decode result of 47th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_47 decode result of 47th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_48
Address: Operational Base + offset (0x0460)
BCH decode result of 48th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_48 decode result of 48th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_49
Address: Operational Base + offset (0x0464)
BCH decode result of 49th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_49 decode result of 49th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_50
Address: Operational Base + offset (0x0468)
BCH decode result of 50th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_50 decode result of 50th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_51

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Address: Operational Base + offset (0x046c)
BCH decode result of 51th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_51 decode result of 51th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_52
Address: Operational Base + offset (0x0470)
BCH decode result of 52th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_52 decode result of 52th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_53
Address: Operational Base + offset (0x0474)
BCH decode result of 53th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_53 decode result of 53th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_54
Address: Operational Base + offset (0x0478)
BCH decode result of 54th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_54 decode result of 54th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_55
Address: Operational Base + offset (0x047c)
BCH decode result of 55th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_55 decode result of 55th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_56
Address: Operational Base + offset (0x0480)
BCH decode result of 56th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_56 decode result of 56th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_57
Address: Operational Base + offset (0x0484)
BCH decode result of 57th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_57 decode result of 57th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_58
Address: Operational Base + offset (0x0488)
BCH decode result of 58th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_58 decode result of 58th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_59
Address: Operational Base + offset (0x048c)
BCH decode result of 59th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_59 decode result of 59th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE1_24
Address: Operational Base + offset (0x0490)
BCH decode result of 24th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_24 decode result of 24th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_25
Address: Operational Base + offset (0x0494)
BCH decode result of 25th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_25 decode result of 25th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_26

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Address: Operational Base + offset (0x0498)
BCH decode result of 26th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_26 decode result of 26th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_27
Address: Operational Base + offset (0x049c)
BCH decode result of 27th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_27 decode result of 27th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_28
Address: Operational Base + offset (0x04a0)
BCH decode result of 28th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_28 decode result of 28th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_29
Address: Operational Base + offset (0x04a4)
BCH decode result of 29th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_29 decode result of 2th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_30
Address: Operational Base + offset (0x04a8)
BCH decode result of 30th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_30 decode result of 30th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_31
Address: Operational Base + offset (0x04ac)
BCH decode result of 31th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_31 decode result of 31th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_32
Address: Operational Base + offset (0x04b0)
BCH decode result of 32th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_32 decode result of 32th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_33
Address: Operational Base + offset (0x04b4)
BCH decode result of 33th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_33 decode result of 33th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_34
Address: Operational Base + offset (0x04b8)
BCH decode result of 34th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_34 decode result of 34th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_35
Address: Operational Base + offset (0x04bc)
BCH decode result of 35th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_35 decode result of 35th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_36
Address: Operational Base + offset (0x04c0)
BCH decode result of 3th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_36 decode result of 36th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_37

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Address: Operational Base + offset (0x04c4)
BCH decode result of 37th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_37 decode result of 37th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_38
Address: Operational Base + offset (0x04c8)
BCH decode result of 38th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_38 decode result of 38th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_39
Address: Operational Base + offset (0x04cc)
BCH decode result of 39th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_39 decode result of 39th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_40
Address: Operational Base + offset (0x04d0)
BCH decode result of 40th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_40 decode result of 40th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_41
Address: Operational Base + offset (0x04d4)
BCH decode result of 41th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_41 decode result of 41th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_42
Address: Operational Base + offset (0x04d8)
BCH decode result of 42th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_42 decode result of 42th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_43
Address: Operational Base + offset (0x04dc)
BCH decode result of 43th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_43 decode result of 43th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_44
Address: Operational Base + offset (0x04e0)
BCH decode result of 44th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_44 decode result of 44th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_45
Address: Operational Base + offset (0x04e4)
BCH decode result of 45th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_45 decode result of 45th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_46
Address: Operational Base + offset (0x04e8)
BCH decode result of 46th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_46 decode result of 46th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_47
Address: Operational Base + offset (0x04ec)
BCH decode result of 47th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_47 decode result of 47th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_48

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Address: Operational Base + offset (0x04f0)
BCH decode result of 48th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_48 decode result of 48th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_49
Address: Operational Base + offset (0x04f4)
BCH decode result of 49th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_49 decode result of 49th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_50
Address: Operational Base + offset (0x04f8)
BCH decode result of 50th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_50 decode result of 50th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_51
Address: Operational Base + offset (0x04fc)
BCH decode result of 51th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_51 decode result of 51th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_52
Address: Operational Base + offset (0x0500)
BCH decode result of 52th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_52 decode result of 52th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_53
Address: Operational Base + offset (0x0504)
BCH decode result of 53th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_53 decode result of 53th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_54
Address: Operational Base + offset (0x0508)
BCH decode result of 54th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_54 decode result of 54th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_55
Address: Operational Base + offset (0x050c)
BCH decode result of 55th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_55 decode result of 55th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_56
Address: Operational Base + offset (0x0510)
BCH decode result of 56th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_56 decode result of 56th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_57
Address: Operational Base + offset (0x0514)
BCH decode result of 57th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_57 decode result of 57th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_58
Address: Operational Base + offset (0x0518)
BCH decode result of 58th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_58 decode result of 58th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_59

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Address: Operational Base + offset (0x051c)
BCH decode result of 59th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_59 decode result of 59th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHST8
Address: Operational Base + offset (0x0520)
BCH Status Register For Codeword 16~17

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd16_cwd17 BCHST information for 16th and 17th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST9
Address: Operational Base + offset (0x0524)
BCH Status Register For Codeword 18~19

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd18_cwd19 BCHST information for 18th and 19th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST10
Address: Operational Base + offset (0x0528)
BCH Status Register For Codeword 20~21

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd20_cwd21 BCHST information for 20th and 21th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST11
Address: Operational Base + offset (0x052c)

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BCH Status Register For Codeword 22~23

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd22_cwd23 BCHST information for 22th and 23th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST12

Address: Operational Base + offset (0x0530)

BCH Status Register For Codeword 24~25

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd24_cwd25 BCHST information for 24th and 25th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST13

Address: Operational Base + offset (0x0534)

BCH Status Register For Codeword 26~27

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd26_cwd27 BCHST information for 26th and 27th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST14

Address: Operational Base + offset (0x0538)

BCH Status Register For Codeword 28~29

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd28_cwd29 BCHST information for 28th and 29th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST15

Address: Operational Base + offset (0x053c)

BCH Status Register For Codeword 30~31

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd30_cwd31 BCHST information for 30th and 31th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_RANDMZ_SEED13_0
Address: Operational Base + offset (0x0600)
Seed 0 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_1
Address: Operational Base + offset (0x0604)
Seed 1 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_2
Address: Operational Base + offset (0x0608)
Seed 2 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_3
Address: Operational Base + offset (0x060c)
Seed 3 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_4
Address: Operational Base + offset (0x0610)
Seed 4 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	randmz_seed13_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_5
Address: Operational Base + offset (0x0614)
Seed 5 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_6
Address: Operational Base + offset (0x0618)
Seed 6 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_7
Address: Operational Base + offset (0x061c)
Seed 7 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_8
Address: Operational Base + offset (0x0620)
Seed 8 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_9
Address: Operational Base + offset (0x0624)
Seed 9 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_10

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Address: Operational Base + offset (0x0628)
Seed 10 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_11
Address: Operational Base + offset (0x062c)
Seed 11 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_12
Address: Operational Base + offset (0x0630)
Seed 12 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_13
Address: Operational Base + offset (0x0634)
Seed 13 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_14
Address: Operational Base + offset (0x0638)
Seed 14 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_15
Address: Operational Base + offset (0x063c)
Seed 15 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	randmz_seed13_15 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_0
Address: Operational Base + offset (0x0640)
Seed 0 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_1
Address: Operational Base + offset (0x0644)
Seed 1 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_2
Address: Operational Base + offset (0x0648)
Seed 2 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_3
Address: Operational Base + offset (0x064c)
Seed 3 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_4
Address: Operational Base + offset (0x0650)
Seed 4 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_5

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Address: Operational Base + offset (0x0654)
Seed 5 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_6
Address: Operational Base + offset (0x0658)
Seed 6 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_7
Address: Operational Base + offset (0x065c)
Seed 7 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_8
Address: Operational Base + offset (0x0660)
Seed 8 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_9
Address: Operational Base + offset (0x0664)
Seed 9 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_10
Address: Operational Base + offset (0x0668)
Seed 10 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:0	RW	0x00000	randmz_seed17_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_11
Address: Operational Base + offset (0x066c)
Seed 11 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_12
Address: Operational Base + offset (0x0670)
Seed 12 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_13
Address: Operational Base + offset (0x0674)
Seed 13 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_14
Address: Operational Base + offset (0x0678)
Seed 14 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_15
Address: Operational Base + offset (0x067c)
Seed 15 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_15 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_0

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Address: Operational Base + offset (0x0680)
Seed 0 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_1
Address: Operational Base + offset (0x0684)
Seed 1 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_2
Address: Operational Base + offset (0x0688)
Seed 2 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_3
Address: Operational Base + offset (0x068c)
Seed 3 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_4
Address: Operational Base + offset (0x0690)
Seed 4 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_5
Address: Operational Base + offset (0x0694)
Seed 5 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RW	0x00000	randmz_seed19_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_6
Address: Operational Base + offset (0x0698)
Seed 6 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_7
Address: Operational Base + offset (0x069c)
Seed 7 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_8
Address: Operational Base + offset (0x06a0)
Seed 8 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_9
Address: Operational Base + offset (0x06a4)
Seed 9 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_10
Address: Operational Base + offset (0x06a8)
Seed 10 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_11

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Address: Operational Base + offset (0x06ac)
Seed 11 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_12
Address: Operational Base + offset (0x06b0)
Seed 12 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_13
Address: Operational Base + offset (0x06b4)
Seed 13 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_14
Address: Operational Base + offset (0x06b8)
Seed 14 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_15
Address: Operational Base + offset (0x06bc)
Seed 15 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_15 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_0
Address: Operational Base + offset (0x06c0)
Seed 0 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:0	RW	0x000000	randmz_seed23_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_1
Address: Operational Base + offset (0x06c4)
Seed 1 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_2
Address: Operational Base + offset (0x06c8)
Seed 2 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_3
Address: Operational Base + offset (0x06cc)
Seed 3 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_4
Address: Operational Base + offset (0x06d0)
Seed 4 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_5
Address: Operational Base + offset (0x06d4)
Seed 5 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_6

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Address: Operational Base + offset (0x06d8)
Seed 6 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_7
Address: Operational Base + offset (0x06dc)
Seed 7 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_8
Address: Operational Base + offset (0x06e0)
Seed 8 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_9
Address: Operational Base + offset (0x06e4)
Seed 9 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_10
Address: Operational Base + offset (0x06e8)
Seed 10 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_11
Address: Operational Base + offset (0x06ec)
Seed 11 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:0	RW	0x000000	randmz_seed23_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_12
Address: Operational Base + offset (0x06f0)
Seed 12 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_13
Address: Operational Base + offset (0x06f4)
Seed 13 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_14
Address: Operational Base + offset (0x06f8)
Seed 14 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_15
Address: Operational Base + offset (0x06fc)
Seed 15 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_15 The seed for randomizer(initial value);

9.5 Interface Description

Table 9-2 NandC0 Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
flash_wp	O	IO_FLASH0wp_EMMCpwren_FLASH0gpio3b1	GPIO3B_IOMUX[3:2] = 2'b01
flash_ale	O	IO_FLASH0ale_FLASH0gpio3b3	GPIO3B_IOMUX[6]= 1'b1
flash_cle	O	IO_FLASH0cle_FLASH0gpio3b4	GPIO3B_IOMUX[8]= 1'b1

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Module Pin	IO	Pad Name	IOMUX Setting
flash_wrn	O	IO_FLASH0wrn_FLASH0gpio3b5	GPIO3B_IOMUX[10]= 1'b1
flash_rdn	O	IO_FLASH0rdn_FLASH0gpio3b2	GPIO3B_IOMUX[4]= 1'b1
flash_dqs	I/O	IO_FLASH0dqs_EMMCclkout_FLASH0gpio3c2	GPIO3C_IOMUX[5:4] = 2'b01
flash_rdy	I	IO_FLASH0rdy_FLASH0gpio3b0	GPIO3B_IOMUX[0]= 1'b1
flash_csn0	O	IO_FLASH0csn0_FLASH0gpio3b6	GPIO3B_IOMUX[12]= 1'b1
flash_csn1	O	IO_FLASH0csn1_FLASH0gpio3b7	GPIO3B_IOMUX[14]= 1'b1
flash_csn2	O	IO_FLASH0csn2_EMMCcmd_FLASH0gpio3c0	GPIO3C_IOMUX[1:0] = 2'b01
flash_csn3	O	IO_FLASH0csn3_EMMCrstnout_FLASH0gpio3c1	GPIO3C_IOMUX[3:2] = 2'b01
flash_csn4	O	IO_FLASH1wp_HOSTckoutn_MACrxdv_FLASH0csn4_FLASH1gpio4a1	GPIO4AL_IOMUX[6:4]= 3'b100
flash_csn5	O	IO_FLASH1rdn_HOSTdout8_MACrxer_FLASH0csn5_FLASH1gpio4a2	GPIO4AL_IOMUX[10: 8]= 3'b100
flash_csn6	O	IO_FLASH1ale_HOSTdout9_MACclk_FLASH0csn6_FLASH1gpio4a3	GPIO4AL_IOMUX[14: 12]= 3'b100
flash_csn7	O	IO_FLASH1cle_HOSTdout10_MACtxen_FLASH0csn7_FLASH1gpio4a4	GPIO4AH_IOMUX[2:0]= 3'b100
flash_data0	I/O	IO_FLASH0data0_EMMCdata0_FLASH0gpio3a0	GPIO3A_IOMUX[1:0] = 2'b01
flash_data1	I/O	IO_FLASH0data1_EMMCdata1_FLASH0gpio3a1	GPIO3A_IOMUX[3:2] = 2'b01
flash_data2	I/O	IO_FLASH0data2_EMMCdata2_FLASH0gpio3a2	GPIO3A_IOMUX[5:4] = 2'b01
flash_data3	I/O	IO_FLASH0data3_EMMCdata3_FLASH0gpio3a3	GPIO3A_IOMUX[7:6] = 2'b01
flash_data4	I/O	IO_FLASH0data4_EMMCdata4_FLASH0gpio3a4	GPIO3A_IOMUX[9:8] = 2'b01
flash_data5	I/O	IO_FLASH0data5_EMMCdata5_FLASH0gpio3a5	GPIO3A_IOMUX[11:1 0]= 2'b01
flash_data6	I/O	IO_FLASH0data6_EMMCdata6_FLASH0gpio3a6	GPIO3A_IOMUX[13:1 2]= 2'b01
flash_data7	I/O	IO_FLASH0data7_EMMCdata7_FLASH0gpio3a7	GPIO3A_IOMUX[15:1 4]= 2'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 9-3 NandC1 Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
flash_wp	O	IO_FLASH1wp_HOSTckoutn_MACrxdv_FLASH0csn4_FLASH1gpio4a1	GPIO4AL_IOMUX[2:0]= 3'b001
flash_ale	O	IO_FLASH1ale_HOSTdout9_MACclk_FLASH0csn6_FLASH1gpio4a3	GPIO4AL_IOMUX[14: 12]= 3'b001
flash_cle	O	IO_FLASH1cle_HOSTdout10_MACtxen_FLASH0csn7_FLASH1gpio4a4	GPIO4AH_IOMUX[2:0]= 3'b001
flash_wrn	O	IO_FLASH1wrn_HOSTdout11_MACmdio_FLASH1gpio4a5	GPIO4AH_IOMUX[5:4]= 2'b01
flash_rdn	O	IO_FLASH1rdn_HOSTdout8_MACrxer_FLASH0csn5_FLASH1gpio4a2	GPIO4AL_IOMUX[10: 8]= 3'b001
flash_dqs	I/O	IO_FLASH1dqs_HOSTdout14_MAC	GPIO4BL_IOMUX[2:0

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Module Pin	IO	Pad Name	IOMUX Setting
		col_FLASH1csn3_FLASH1gpio4b0	]= 3'b001
flash_rdy	I	IO_FLASH1rdy_HOSTckoutp_MACmdc_FLASH1gpio4a0	GPIO4AL_IOMUX[1:0]= 2'b01
flash_csn0	O	IO_FLASH1csn0_HOSTdout12_MACrxclk_SDIO1cmd_FLASH1gpio4a6	GPIO4AH_IOMUX[10:8]= 3'b001
flash_csn1	O	IO_FLASH1csn1_HOSTdout13_MACcrs_SDIO1clkout_FLASH1gpio4a7	GPIO4AH_IOMUX[14:12]= 3'b001
flash_csn2	O	IO_FLASH1csn2_HOSTdout15_MACtxclk_SDIO1pwren_FLASH1gpio4b1	GPIO4BL_IOMUX[6:4]= 3'b001
flash_csn3	O	IO_FLASH1dqs_HOSTdout14_MACcol_FLASH1csn3_FLASH1gpio4b0	GPIO4BL_IOMUX[2:0]= 3'b100
flash_data0	I/O	IO_FLASH1data0_HOSTdout0_MACtxd2_SDIO1data0_FLASH1gpio3d0	GPIO3DL_IOMUX[2:0]= 3'b001
flash_data1	I/O	IO_FLASH1data1_HOSTdout1_MACtxd3_SDIO1data1_FLASH1gpio3d1	GPIO3DL_IOMUX[6:4]= 3'b001
flash_data2	I/O	IO_FLASH1data2_HOSTdout2_MACrxd2_SDIO1data2_FLASH1gpio3d2	GPIO3DL_IOMUX[10:8]= 3'b001
flash_data3	I/O	IO_FLASH1data3_HOSTdout3_MACrxd3_SDIO1data3_FLASH1gpio3d3	GPIO3DL_IOMUX[14:12]= 3'b001
flash_data4	I/O	IO_FLASH1data4_HOSTdout4_MACtxd0_SDIO1detectn_FLASH1gpio3d4	GPIO3DH_IOMUX[2:0]= 3'b001
flash_data5	I/O	IO_FLASH1data5_HOSTdout5_MACtxd1_SDIO1wrprt_FLASH1gpio3d5	GPIO3DH_IOMUX[6:4]= 3'b001
flash_data6	I/O	IO_FLASH1data6_HOSTdout6_MACrxd0_SDIO1bkpwr_FLASH1gpio3d6	GPIO3DH_IOMUX[10:8]= 3'b001
flash_data7	I/O	IO_FLASH1data7_HOSTdout7_MACrxd1_SDIO1intn_FLASH1gpio3d7	GPIO3DH_IOMUX[14:12]= 3'b001

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

Table 9-4 NandC Interface Connection

Module Pin	Direction	Flash Interface			
		Asyn8x	Asyn16x	ONFI	Toggle
flash_csni(i=0~7)	O	√	√	√	√
flash_wp	O	√	√	√	√
flash_ale	O	√	√	√	√
flash_cle	O	√	√	√	√
flash_wrn	O	√	√	√	√
flash_rdn	O	√	√	√	√
flash_data[7:0]	I/O	√	√	√	√
flash_data[15:8]	I/O	-	√	-	-
flash_dqs	I/O	-	-	√	√
flash_rdy	I	√	√	√	√

9.6 Application Notes

9.6.1 Clock Description

There are two clock domains in the NandC. One is hclk, and the other is nclk.

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- AHB slave bus uses the hclk to configure the NandC registers.
- AHB master bus uses the hclk to transmit the data between the external memory and internal sram.
- NandC use nclk to transmit the data between the nand flash and internal sram.
- All the flash interface timing configuration is relative to the nclk.

9.6.2 BCHST/BCHLOC/BCHDE/SPARE Application

1. BCHST

There are 16 BCHST-registers in NandC to store 32 codeword's BCH decode status(bchst) information. Every register stores 2 codeword's bchst information except BCHST0, which not only includes bchst information, but also includes one bit for *bchrdy*.

Let bchst_cwd0~bchst_cwd31 be the bchst information for 32 codewords. In BCHST-registers, the latest codeword's bchst is stored into bchst_cwd0, and the former is shifted into bchst_cwd1. That is, bchst_cwd0→ bchst_cwd1 →……→bchst_cwd31. Therefore, for example, if 32 codewords are decoded, then bchst_cwd0 is the bch decode status for codeword31, and bchst_cwd31 is the bch decode status for codeword0.

bchst_cwd0 = {BCHST0[28],BCHST0[12:8],BCHST0[27],BCHST0[7:3],BCHST0[2:0]}

bchst_cwd1 = {BCHST0[30],BCHST0[25:21],BCHST0[29],BCHST0[20:16],BCHST0[15:13]}
bchst_cwd2 = {BCHST1[28],BCHST1[12:8],BCHST1[27],BCHST1[7:3],BCHST1[2:0]}
bchst_cwd3 = {BCHST1[30],BCHST1[25:21],BCHST1[29],BCHST1[20:16],BCHST1[15:13]}
bchst_cwd4 = {BCHST2[28],BCHST2[12:8] ,BCHST2[27],BCHST2[7:3],BCHST2[2:0]}
bchst_cwd5 = {BCHST2[30],BCHST2[25:21],BCHST2[29],BCHST2[20:16],BCHST2[15:13]}
bchst_cwd6 = {BCHST3[28],BCHST3[12:8] ,BCHST3[27],BCHST3[7:3],BCHST3[2:0]}
bchst_cwd7 = {BCHST3[30],BCHST3[25:21],BCHST3[29],BCHST3[20:16],BCHST3[15:13]}
bchst_cwd8 = {BCHST4[28],BCHST4[12:8] ,BCHST4[27],BCHST4[7:3],BCHST4[2:0]}
bchst_cwd9 = {BCHST4[30],BCHST4[25:21],BCHST4[29],BCHST4[20:16],BCHST4[15:13]}
bchst_cwd10 = {BCHST5[28],BCHST5[12:8] ,BCHST5[27],BCHST5[7:3],BCHST5[2:0]}
bchst_cwd11 = {BCHST5[30],BCHST5[25:21],BCHST5[29],BCHST5[20:16],BCHST5[15:13]}
bchst_cwd12 = {BCHST6[28],BCHST6[12:8] ,BCHST6[27],BCHST6[7:3],BCHST6[2:0]}
bchst_cwd13 = {BCHST6[30],BCHST6[25:21],BCHST6[29],BCHST6[20:16],BCHST6[15:13]}
bchst_cwd14 = {BCHST7[28],BCHST7[12:8] ,BCHST7[27],BCHST7[7:3],BCHST7[2:0]}
bchst_cwd15 =
{BCHST7[30],BCHST7[25:21],BCHST7[29],BCHST7[20:16],BCHST7[15:13]}

bchst_cwd16 = {BCHST8[28],BCHST8[12:8],BCHST8[27],BCHST8[7:3],BCHST8[2:0]}

bchst_cwd17 = {BCHST8[30],BCHST8[25:21],BCHST8[29],BCHST8[20:16],BCHST8[15:13]}
bchst_cwd18 = {BCHST9[28],BCHST9[12:8],BCHST9[27],BCHST9[7:3],BCHST9[2:0]}
bchst_cwd19 = {BCHST9[30],BCHST9[25:21],BCHST9[29],BCHST9[20:16],BCHST9[15:13]}
bchst_cwd20 = {BCHST10[28],BCHST10[12:8] ,BCHST10[27],BCHST10[7:3],BCHST10[2:0]}
bchst_cwd21 =
{BCHST10[30],BCHST10[25:21],BCHST10[29],BCHST10[20:16],BCHST10[15:13]}

bchst_cwd22 = {BCHST11[28],BCHST11[12:8] ,BCHST11[27],BCHST11[7:3],BCHST11[2:0]}
bchst_cwd23 =
{BCHST11[30],BCHST11[25:21],BCHST11[29],BCHST11[20:16],BCHST11[15:13]}

bchst_cwd24 = {BCHST12[28],BCHST12[12:8] ,BCHST12[27],BCHST12[7:3],BCHST12[2:0]}
bchst_cwd25 =
{BCHST12[30],BCHST12[25:21],BCHST12[29],BCHST12[20:16],BCHST12[15:13]}

bchst_cwd26 = {BCHST13[28],BCHST13[12:8] ,BCHST13[27],BCHST13[7:3],BCHST13[2:0]}
bchst_cwd27 =
{BCHST13[30],BCHST13[25:21],BCHST13[29],BCHST13[20:16],BCHST13[15:13]}

bchst_cwd28 = {BCHST14[28],BCHST14[12:8] ,BCHST14[27],BCHST14[7:3],BCHST14[2:0]}

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bchst_cwd29 =
{BCHST14[30],BCHST14[25:21],BCHST14[29],BCHST14[20:16],BCHST14[15:13]}

bchst_cwd30 = {BCHST15[28],BCHST15[12:8] ,BCHST15[27],BCHST15[7:3],BCHST15[2:0]}
bchst_cwd31 =
{BCHST15[30],BCHST15[25:21],BCHST15[29],BCHST15[20:16],BCHST15[15:13]}

2. BCHLOC

There are 7 BCHLOC-registers in NandC to store 32 codeword's bch decode location(bchloc) information.

Let bchloc_cwd0~bchloc_cwd31 be the bchloc information for the 32 codeword. In BCHLOC registers, the latest codeword's bchloc is stored into bchloc_cwd0, and the former is shifted into bchloc_cwd1. That is, bchloc_cwd0→bchloc_cwd1→……→bchloc_cwd31. Therefore, for example, if 32 codeword are decoded, then bchloc_cwd0 is the bch decode status for codeword31, and bchloc_cwd31 is the bch decode status for codeword0.

bchloc_cwd0 = {BCHLOC6[0], BCHLOC0[4:0]}

bchloc_cwd1 = {BCHLOC6[1], BCHLOC0[9:5]}

bchloc_cwd2 = {BCHLOC6[2], BCHLOC0[14:10]}

bchloc_cwd3 = {BCHLOC6[3], BCHLOC0[19:15]}

bchloc_cwd4 = {BCHLOC6[4], BCHLOC0[24:20]}

bchloc_cwd5 = {BCHLOC6[5], BCHLOC0[29:25]}

bchloc_cwd6 = {BCHLOC6[6], BCHLOC1[4:0]}

bchloc_cwd7 = {BCHLOC6[7], BCHLOC1[9:5]}

bchloc_cwd8 = {BCHLOC6[8], BCHLOC1[14:10]}

bchloc_cwd9 = {BCHLOC6[9], BCHLOC1[19:15]}

bchloc_cwd10 = {BCHLOC6[10], BCHLOC1[24:20]}

bchloc_cwd11 = {BCHLOC6[11], BCHLOC1[29:25]}

bchloc_cwd12 = {BCHLOC6[12], BCHLOC2[4:0]}

bchloc_cwd13 = {BCHLOC6[13], BCHLOC2[9:5]}

bchloc_cwd14 = {BCHLOC6[14], BCHLOC2[14:10]}

bchloc_cwd15 = {BCHLOC6[15], BCHLOC2[19:15]}

bchloc_cwd16 = {BCHLOC6[16], BCHLOC2[24:20]}

bchloc_cwd17 = {BCHLOC6[17], BCHLOC2[29:25]}

bchloc_cwd18 = {BCHLOC6[18], BCHLOC3[4:0]}

bchloc_cwd19 = {BCHLOC6[19], BCHLOC3[9:5]}

bchloc_cwd20 = {BCHLOC6[20], BCHLOC3[14:10]}

bchloc_cwd21 = {BCHLOC6[21], BCHLOC3[19:15]}

bchloc_cwd22 = {BCHLOC6[22], BCHLOC3[24:20]}

bchloc_cwd23 = {BCHLOC6[23], BCHLOC3[29:25]}

bchloc_cwd24 = {BCHLOC6[24], BCHLOC4[4:0]}

bchloc_cwd25 = {BCHLOC6[25], BCHLOC4[9:5]}

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bchloc_cwd26 = {BCHLOC6[26], BCHLOC4[14:10]}

bchloc_cwd27 = {BCHLOC6[27], BCHLOC4[19:15]}

bchloc_cwd28 = {BCHLOC6[28], BCHLOC4[24:20]}

bchloc_cwd29 = {BCHLOC6[29], BCHLOC4[29:25]}

bchloc_cwd30 = {BCHLOC6[30], BCHLOC5[4:0]}

bchloc_cwd31 = {BCHLOC6[31], BCHLOC5[9:5]}

3. BCHDE

BCHDE includes two register-groups, BCHDE0 and BCHDE1. Each group has 60 registers: BCHDE0_0~BCHDE0_59 and BCHDE1_0~BCHDE1_59. BCHDE0_n(n=0~59) is the decode information of the nth error bit for codeword in sram0, and BCHDE1_n(n=0~59) is the decode information of the nth error bit for codeword in sram1.

The needed number of BCHDE registers is determined by bchmode. That is:

a. When 16bitBCH selected, BCHDEm_0 ~ BCHDEm_15 are available

b. When 24bitBCH selected, BCHDEm_0 ~ BCHDEm_23 are available

c. When 40bitBCH selected, BCHDEm_0 ~ BCHDEm_39 are available

d. When 60bitBCH selected, BCHDEm_0 ~ BCHDEm_59 are available

4. SPARE

SPARE includes two register-groups, SPARE0 and SPARE1. Each group has 28 registers: SPARE0_0~SPARE0_27 and SPARE1_0~SPARE1_27.

When in bch encoding, SPARE0_0 stores system information for codeword in sram0, SPARE0_n(n=1~27) stores encode information for codeword in sram0; SPARE1_0 stores system information for codeword in sram1, SPARE1_n(n=1~27) stores encode information for codeword in sram1.

When in bch decoding, SPARE0_n(n=0~27) stores the spare data read from flash for codeword in sram0; SPARE1_n(n=0~27) stores the spare data read from flash for codeword in sram1.

The needed number of BCHDE registers is determined by bchmode. That is:

a. When 16bitBCH selected, spare data=28bytes, SPAREm_0~SPAREm_7 are available

b. When 24bitBCH selected, spare data=42bytes, SPAREm_0~SPAREm_10 and SPAREm_11[15:0] are available

c. When 40bitBCH selected, spare data=70bytes, SPAREm_0~SPAREm_17 and SPAREm_18[15:0] are available

d. When 60bitBCH selected, spare data=105bytes, SPAREm_0~SPAREm_26 and SPAREm_27[7:0] are available

9.6.3 Bus Mode Application

MTRANS_CFG[2] determines whether the data load/store between internal memory and external memory is through slave interface or master interface.

1. Slave Mode

When MTRANS_CFG[2]=0, slave is selected. i. e. , flash data load/store between internal memory and external memory is through slave interface by cpu or external DMA.

In this mode, software should store page data into internal memory and spare data into SPARE

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registers before starting flash program operation; and should load page data from internal memory and spare data from SPARE registers after finishing flash read operation.

In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are unused. The transfer codeword number is determined by FLCTL[6:5], and the maximum number is 2.

The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transfer is finished.

2. Master Mode

When MTRANS_CFG[2]=1, master is selected. i. e. , flash data load/store between internal memory and external memory is through master interface.

In this mode, software should initialize page data and spare data into external memory, and set their addresses in MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash program operation. Similarly, software should configure MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash read operation and could read data from addresses in MTRANS_SADDR0 and MTRANS_SADDR1 after NandC transfer finish.

In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are used. The transfer codeword number is determined by FLCTL[26:22], and the maximum number is 16.

The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transmission is finished.

When MTRANS_CFG[2]=1, page data and spare data are stored in the continuous space of external memory respectively.

For page data, source address is named Saddr0, specified in MTRANS_SADDR0. The space can be divided into many continuous units, and the unit size(named PUnit) is 1024 bytes or 512 bytes determined by FLCTL[21] and FLCTL[11]:

a. when FLCTL[11]=0, PUnit is always equal to 1024 bytes
b. when FLCTL[11]=1 and FLCTL[21]=0, PUnit is equal to 1024 bytes
c. when FLCTL[11]=1 and FLCTL[21]=1, PUnit is equal to 512 bytes

For spare data, source address is named Saddr1, specified in MTRANS_SADDR1. The space can be divided into many continuous units, and the unit size(named SUnit) is 64 bytes or 128 bytes determined by BCHCTL[18], FLCTL[11] and FLCTL[21]:

a. When FLCTL[11]=0 and BCHCTL[18]=0, SUnit is equal to 64 bytes
b. When FLCTL[11]=0 and BCHCTL[18]=1, SUnit is equal to 128 bytes
c. When FLCTL[11]=1 and FLCTL[21]=0, SUnit is equal to 128 bytes
d. When FLCTL[11]=1 and FLCTL[21]=1, SUnit is equal to 64 bytes

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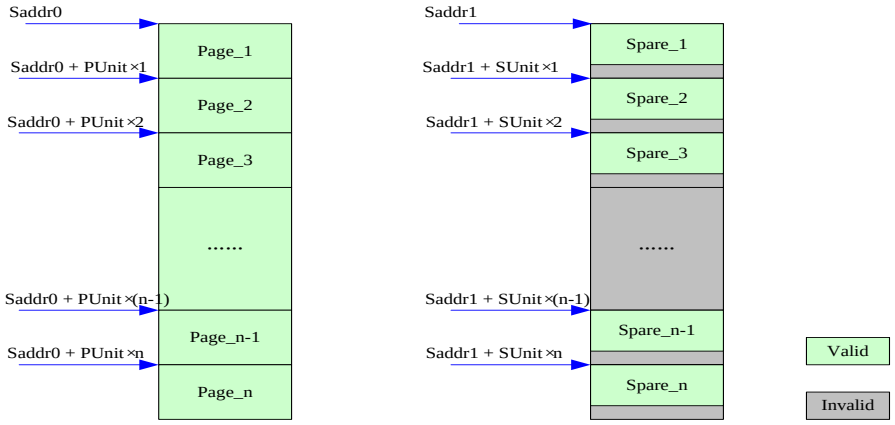

Fig. 9-2 NandC Address Assignment

The detailed format for page data and spare data in every unit is shown in following figures.

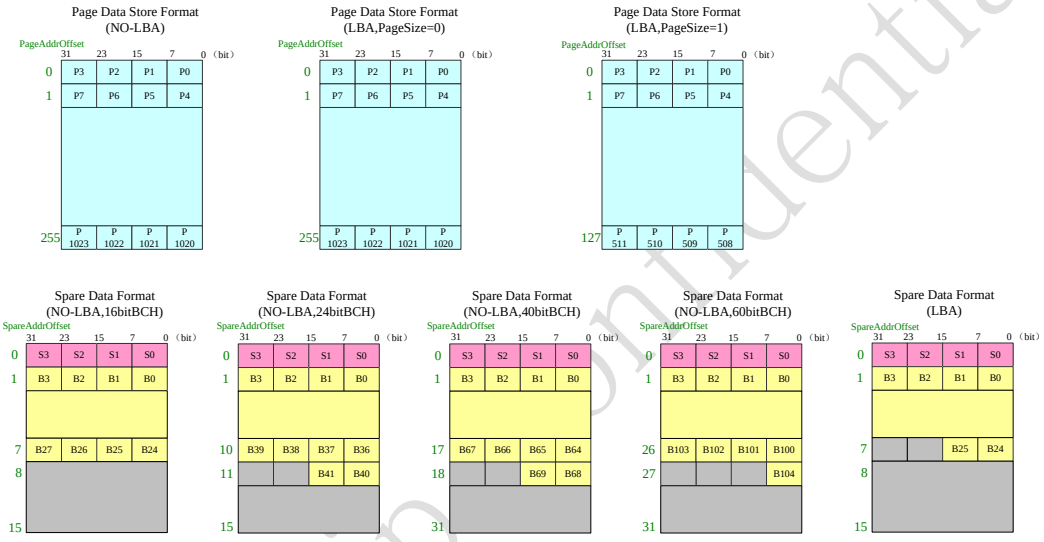

Fig. 9-3 NandC DataFormat

9.6.4 BchPage Application

BCHCTL[16] determines whether codeword size for page data is 1024 bytes or 512 bytes when FLCTL[11] is 0.

1. 1024bytes

When BCHCTL[16]=0, BchPage=0, hardware needs to write 1024 bytes page data and spare data into flash or read 1024 bytes page data and spare data from flash. All the 1024 bytes page data and spare data are encoded when writing or decoded when reading.

2. 512bytes

When BCHCTL[16]=1, BchPage=1, hardware needs to write 512 bytes page data and spare data into flash or read 512 bytes page data and spare data from flash.

In this mode, the page data unit size for BCH encoder and BCH decoder still is 1024byte. So to support BCH encoder and decoder, software should configure page data as follows: 1th~512th bytes are invalid data which must be stuffed with 0xff, 513th~1024th bytes arevalid page data.

However, Randomizer function is not supported under this condition.

9.6.5 PageSize/SpareSize Application

FLCTL[21] determines whether the codeword size is 1024 bytes or 512 bytes when FLCTL[11]

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is 1.

1. Big Page

When FLCTL[11]=0(LbaEn=0), the flash to be operated is Raw NAND Flash. Every codeword size is 1024 bytes and FLCTL[21] should always be set to 0, and the PageStep in external memory is 1024 bytes if bus mode is master mode.

At this mode, the spare size and SpareStep in external memory are determined by BCH Mode as follows:

BCH Mode=16bitBCH: spare size=(28+4)bytes , SpareStep=64bytes

BCH Mode=24bitBCH: spare size=(42+4)bytes , SpareStep=64bytes

BCH Mode=40bitBCH: spare size=(70+4)bytes , SpareStep=128bytes

BCH Mode=60bitBCH: spare size=(105+4)bytes, SpareStep=128bytes

2. Small Page

When FLCTL[11]=1, LbaEn=1, the flash to be operated is Managed NAND Flash. Every codeword size could be 1024 bytes or 512 bytes according to FLCTL[21]. If FLCTL[21]=0, codeword size is 1024 bytes, PageStep in external memory is 1024 bytes, and SpareStep is 128bytes. If FLCTL[21]=1, codeword size is 512 bytes, PageStep in external memory is 512 bytes, and SpareStep is 64 bytes.

At this mode, the spare size is configured in FLCTL[18:12], and the max available number is 109.

In the summary, the total data size in every codeword for flash or for software including page data and spare data, is determined by BCHCTL[16], FLCTL[11], FLCTL[21], BCHCTL[4], BCHCTL[18]. Their relationship is shown as follows.

Table 9-5 NandC Page/Spare size for flash

page/spare size for software		page size /codeword	spare size /codeword
FLCTL[11]=0	16bitECC	1024 byte	(4+28)byte
	24bitECC	1024 byte	(4+42)byte
	40bitECC	1024 byte	(4+70)byte
	60bitECC	1024 byte	(4+105)byte
FLCTL[11]=1	FLCTL[21]=0	1024 byte	FLCTL[18:12]
	FLCTL[21]=1	512 byte	FLCTL[18:12]

Notes: that "page/spare size for flash" means that hardware should transfer these numbers of bytes in every codeword to or from flash.

9.6.6 Randomizer Application

RANDMZ_CFG[31] determines whether randomizer is enable or not. When RANDMZ_CFG[31] equals to 1, randomizer is active. Data should be scrambled before written into flash, and descrambled after read from flash.

RANDMZ_CFG[30:29] determines the randomizer polynomial.

When RANDMZ_CFG[30:29]=2'b00, Samsung randomizer, Polynomial = 1+x+x^15. RANDMZ_CFG[14:0] is the seed for randomizer.

When RANDMZ_CFG[30:29]=2'b01, TOSHIBA randomizer. RANDMZ_CFG[19:0] is the seed agitation register for randomizer. RANDMZ_CFG[23:20] is the basic seed start point for every page. RANDMZ_CFG[28:24] is the basic seed rotation bits for every 16 page.

When RANDMZ_CFG[30:29]=2'b10, Samsung randomizer, Polynomial = 1+x^14+x^15. RANDMZ_CFG[14:0] is the seed for randomizer.

The data unit for randomizer is one codeword(data+spare).

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However, Randomizer is just available for data transfer by internal DMA mode, but not by for bypass mode. Furthermore, it should not be enable if BCHCTL[16]=0 (BchPage=512bytes).

9.6.7 DLL Application

When Toggle Flash or ONFI Synchronous Flash interface is active, DLL should be used to adjust DQS input with DQ when reading flash.

There are 2 registers for DLL configuration(DLL_CFG_REG0 and DLL_CFG_REG1), and 1 register for DLL status(DLL_OBS_REG0).

The usage guide is as follows:

If bypass mode is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 1, and set *dll_dqs_dly_bypass* in DLL_CFG_REG0[23:16] to determine the dll element number needed. And then set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.

If auto adjusting is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 0, and set the *dll_start_point* in DLL_CFG_REG0[7:0] and *dll_incr* in DLL_CFG_REG1[11:4]. You also should set the adjusting mode *dll_qtren* in DLL_CFG_REG1[3:2] to compute the dll element number needed. If *dll_qtren*=2'b00, the dll element number is determined by *dll_dqs_dly* in DLL_CFG_REG0[15:8]; otherwise, it is 1/4 or 1/8 of the total number of dll elements used for *dll_qtren*=2'b01 or *dll_qtren*=2'b10 separately. The last step is to set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.

If you want to monitor the dll working status, you could read DLL_OBS_REG0. If DLL_OBS_REG0[0]=0, it means that DLL is not locked, and still in detecting status. Otherwise, it means that DLL is locked, and *dll_lock_value* in DLL_OBS_REG0[8:1] is the total number of dll elements used, *dll_dqs_delay_value* in DLL_OBS_REG0[16:9] is the total number of DQS delay used.

9.6.8 NandC Interrupt Application

NandC has 1 interrupt output signal and 4 interrupt sources: dma finish interrupt source, flash ready interrupt source, bch error interrupt source, bchfail interrupt source. When one or more of these interrupt source are enabled, NandC interrupt is asserted if one or more interrupt source is high. Software can determine the interrupt source by reading INTST and clear interrupt by writing corresponding bit in INTCLR.

9.6.9 LLP Application

LLP is used in NandC to store and execute instruction groups configured in external memory by software. When LLPCTL[0]=1, LLP is active, NandC will load instruction groups stored in {LLPCTL[31:6], 6'h0} and execute them. Next instruction groups should not be loaded until current instruction execution finished.

1. LLP Structure

The structure of LLP is shown as follows:

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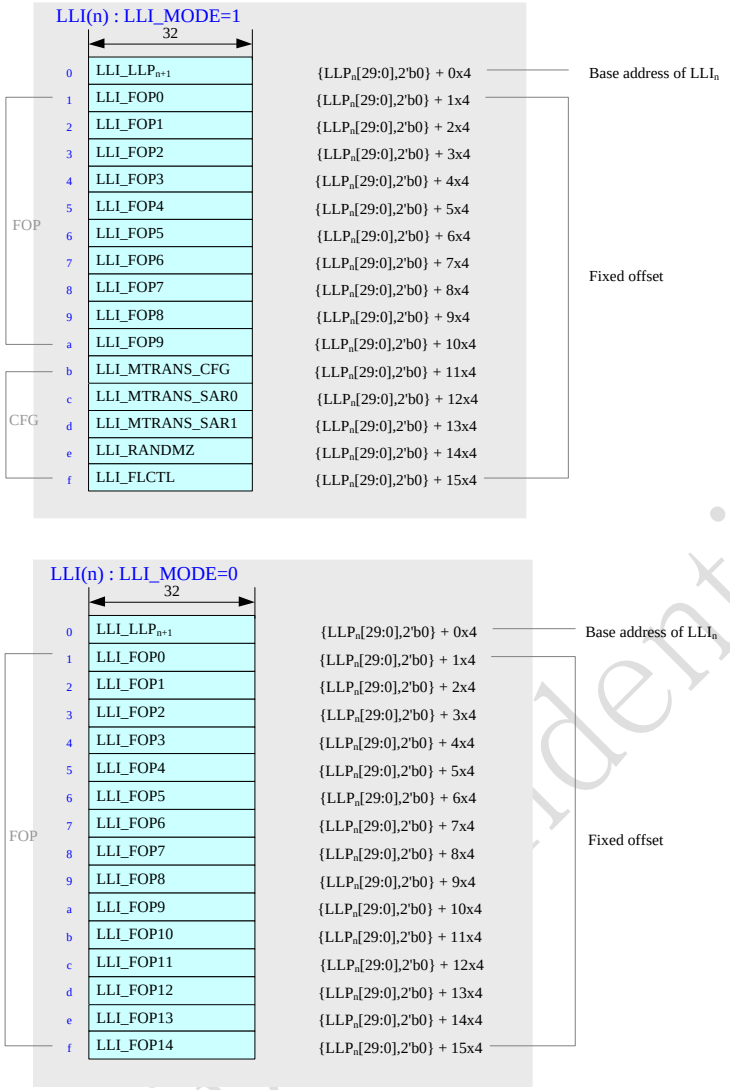


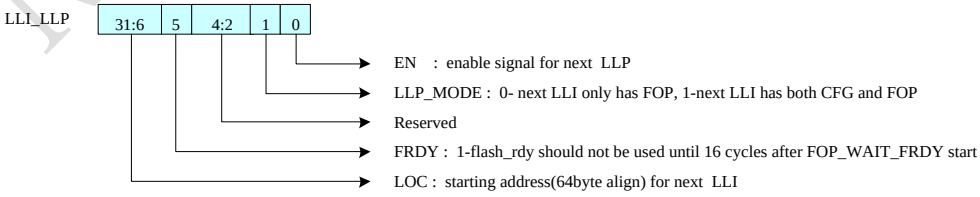
Fig. 9-4 NandC LLP Data Format

LLI_MODE is determined by LLPCTL[1]. If current operation is flash program or flash read, then LLI_MODE=1 is need; otherwise, LLI_MODE=0 is workable.

In addition, you could do more than one flash operation in one LLP group, but you should not separate one flash operation into two LLI groups.

2. LLI Format

a. LLI_LLPn+1 stores the address for next LLI group data



b. LLI_FOP0~LLI_FOP14 store the flash operation instruction

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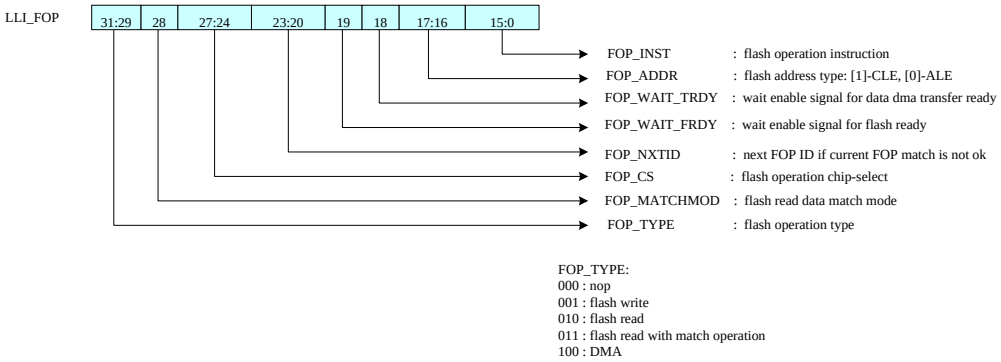

When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. It is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.

c. LLI_MTRANS_CFG/LLI_MTRANS_SADDR0/LLI_MTRANS_SADDR1/ LLI_RANDMZ/ LLI_FLCTL store the configuration for MTRANS_CFG/ MTRANS_SADDR0/MTRANS_SADDR1/RANDMZ/FLCTL.

3. LLP Working Mode

There are two working modes for LLP:

a. Normal mode: LLPCTL[0] is kept to 1 until all LLP loading and executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].

b. Pause mode: LLPCTL[0] is changed from 1 to 0 during LLP loading or LLP executing. NandC should not stop working until current LLP executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].

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Chapter 10 Power Management Unit (PMU)

10.1 Overview

In order to meet high performance and low power requirements, a power management unit is designed for saving power when RK3288 in low power mode. The RK3288 PMU is dedicated for managing the power of the whole chip.

10.1.1 Features

- Support 4 voltage domains including VD_CORE, VD_LOGIC, VD_GPU and VD_PMU
- Support 15 separate power domains in the whole chip, which can be power up/down by software based on different application scenes
- In low power mode, the pmu could power up/down pd_A17_0, pd_scu, vd_core, and pd_bus by hardware
- Support CORTEX-A17 core source clock gating in low power mode
- Support global interrupt disable in low power mode
- Support PLLs power down/up in low power mode
- Support VD_CORE/VD_LOGIC power down/up in low power mode
- Support pd_alive clock switch to 32KHz in low power mode
- Support pd_pmu clock switch to 32KHz request in low power mode
- Support OSC enable/disable request in low power mode
- Support to clamp all VD_LOGIC output before power off it in low power mode
- Support wakeup reset control in power off mode
- Support DDR self-refresh in low power mode
- Support DDR IO retention in low power mode
- Support DDR IO power off in low power mode
- Support DDR controller clock auto gating in low power mode
- Support to send idle requests to all NIU in the SoC (details will be described later)
- A group of configurable counter in PMU for HW control (such as PLL, PMIC, DDRIO and so on)
- Support varies configurable wakeup source for low power mode

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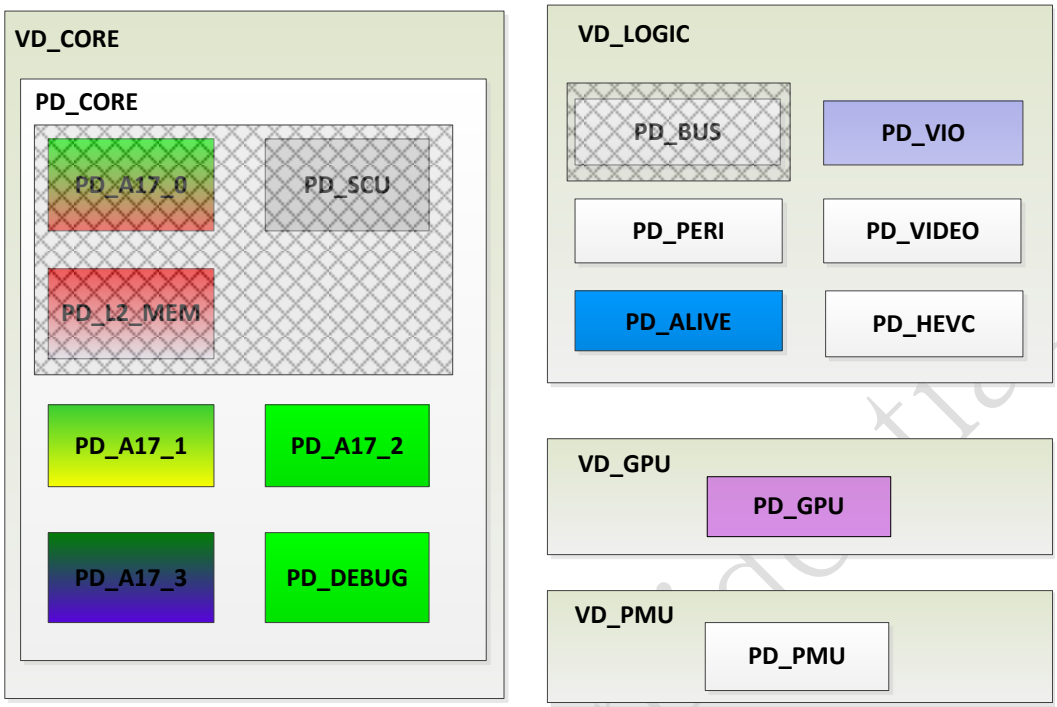
10.2 Block Diagram

10.2.1 power domain partition



Note:
VD_* : voltage domain
PD_* : power domain

Fig. 10-1 Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists all the power domains.

Table 10-1 RK3288 Power Domain and Voltage Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE (PD_CORE system)	PD_A17_0	A17 primary core logic，L1C and neon
	PD_A17_1	A17 slave core 1 logic，L1C and neon
	PD_A17_2	A17 slave core 2 logic，L1C and neon
	PD_A17_3	A17 slave core 3 logic，L1C and neon
	PD_SCU	SCU RAM，SCU，GIC，Periphral，L2 controller
	PD_DEBUG	A17 Debug
	PD_MEM	L2 Cache
VD_LOGIC	PD_BUS	Soc architecture subsystem, include soc architecture (NOC) ，eFuse，TZPC，ROM，DMAC_BUS，Crypto，Host，Timer(6ch), PWM(0~3), UART_DBG, I2C, DDR_PCTL, I2S, Spdif, Internal Memory(96K)
	PD_PERI	Peripheral subsystem , include DMAC_PERI, GMAC, NANDC0/1, USB Host0/USB Host1/ USB OTG, SDMMC/SDIO0/SDIO1/eMMC，HSADC, PS2C, TSADC, UART, I2C, SPI, GPS, TSP
	PD_VIO	Video input/output system, include VOPBIG, VOPLIT, ISP, IEP, RGA, MIPI-CSI, MIPI-DSI, LVDS, HDMI, eDP

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Voltage Domain	Power Domain	Description
	PD_ALIVE	CRU，GRF， GPIO 1~8， TIMER, WDT
	PD_HEVC	HEVC
	PD_VIDEO	Video Encode&Decode , include VEPU，VDPU
VD_GPU	PD_GPU	GPU
VD_PMU	PD_PMU	PMU, SRAM(4K), Secure GRF, GPIO0

Notes: "Always on" means that their power supply can be switched off only by external PMIC module. Only one "always on" power domain is in a voltage domain.

10.2.2 PMU block diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

APB interface and register, which can accept the system configuration
Low Power State Control, which generate low power control signals.
Power Switch Control, which control all power domain switch

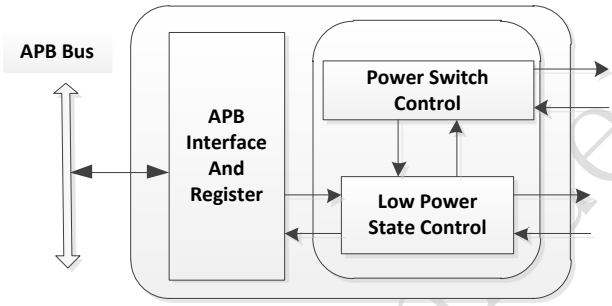

Fig. 10-2 PMU Bock Diagram

10.3 Power Switch Timing Requirement

The following table describe the switch time for power down and power up progress of each power domain. This table gives the time range, and each power domain switch time will be more than the min time and less than the max time.

Table 10-2 Power Switch Timing

Power domain	type	Power down Switch Timing① (ns)	Power up Switch Timing① (ns)
PD_A17_0	min	170.3	132.4
	max	306.7	237.5
PD_A17_1	min	170.3	132.4
	max	306.7	237.5
PD_A17_2	min	181.5	140.7
	max	326.2	251.9
PD_A17_3	min	181.5	140.7
	max	326.2	251.9
PD_DEBUG	min	169.4	131.7
	max	77.3	60
PD_BUS	min	169.4	131.7
	max	313.6	247
PD_PERI	min	103.7	80.5
	max	199.0	156.1
PD_VIO	min	280.6	217.5
	max	518.5	407.8

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Power domain	type	Power down Switch Timing① (ns)	Power up Switch Timing① (ns)
PD_VIDEO	min	315.4	244.2
	max	586.2	460.4
PD_GPU	min	470.2	364
	max	871.4	684.1
PD_HEVC	min	33.4	25.9
	max	62.4	49
	max	65.6	51.5

Notes: the power switch timing is just the chip power electrical parameter, this is not the parameter for the software to determine the power domain status. The software need to check each power domain status register to determine the power status.

10.4 Function Description

10.4.1 Normal Mode

First of all, we define two modes of power for chip, normal mode and low power mode.
In normal mode, the PMU can power off/on all power domain (except pd_A17_0 and pd_bus) by setting PMU_PWRDN_CON register. At same, pmu can send idle request for every power domain by setting PMU_IDLE_REQ register.
Don't set pd_A17_0 and pd_bus power off or send idle_req_core and idle_req_bus in normal mode. This will cause the system to not work properly.
Basically, there are 2 configurations that software can do in normal mode to save power.

- Configure DDR to self-refresh, DDR IO retention and DDR IO power off
- Power down power domains

The first one will save power consumption of using DDR controller and DDR IO. For avoiding confliction, the software must make sure the execution code of this step is not in DDR.
The second one will save power of the power domain which software is shutting down.

10.4.2 Low Power Mode

PMU can work in the Low Power Mode by setting bit[0] of PMU_PWRMODE_CON register. After setting the register, PMU would enter the Low Power mode. In the low power mode, pmu will auto power on/off the specified power domain, send idle req to specified power domain, shut down/up pll and so on. All of above are configurable by setting corresponding registers.

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Table 10-3 Low Power State

Num	Hardware Flow	Description of Flow	Corresponding Register
0	NORMAL	in normal	
1	L2FLUSH_REQ	send L2 cache flush request	bit[3] of PMU_PWRMODE_CON
2	STANDBYL2	wait L2 cache standy	
3	A17_CLK_DIS	close A17 clock	bit[1] of PMU_PWRMODE_CON
4	TRANS_NO_FIN	wait the corresponding noc interface end the transaction	PMU_PMRMODE_CON1
5	SREF_ENTER	enter DDR self-refresh	bit[16:15] of PMU_PWRMODE_CON
6	DDR_IO_RET	ddr io retention	bit[18:17] of PMU_PWRMODE_CON
7	DDR_IO_PWROFF	ddr io power off	bit[20:19] of PMU_PWRMODE_CON
8	BUS_PWRDN	pd_bus power down	bit[4] of PMU_PWRMODE_CON
9	A17_0_PWRDN	pd_a17_0 power down	bit[5] of PMU_PWRMODE_CON
10	L2MEM_PWRDN	pd_l2mem power down (vd_core power down)	bit[6] of PMU_PWRMODE_CON
11	ALIVE_PMU_LF	pd_alive& pd_pmu switch to 32KHz clock	bit[11:10] of PMU_PWRMODE_CON
12	PLL_PWRDN	pll power down	bit[7] of PMU_PWRMODE_CON
13	INPUT_CLAMP	isolation cell input clamp	bit[13] of PMU_PWRMODE_CON
14	POWEROFF	chip power off	bit[8] of PMU_PWRMODE_CON
15	24M_OSC_DIS	close 24MHz OSC	bit[12] of PMU_PWRMODE_CON
16	WAIT_WAKEUP	wait wakeup source	PMU_WAKEUP_CFG0/1
17	WAKEUP_RESET	send reset after wakeup	
18	EXT_PWRUP	pmic power up whole chip	
19	RELEASE_CLAMP	release isolation cell clamp	
20	24M_OSC_EN	open 24MHz OSC	
21	ALIVE_PMU_HF	switch pd_alive and pd_pmu back to 24MHz	
22	WAKEUP_RESET_CLR	release wakeup reset	
23	PLL_PWRUP	Pll power up	
24	BUS_PWRUP	PD_BUS power up	
25	DDR_IO_PWRUP	ddr io power up	
26	SREF_EXIT	exit ddr self-refresh	
27	L2MEM_PWRUP	pd_l2mem power up	
28	A17_0_PWRUP	pd_a17_0 power up	
29	TRANS_RESTORE	restore the transaction	
30	A17_CLK_EN	enable a17 clock	

The Low Power mode have three steps:

Enter Low Power mode, there are some sub-steps in the enter step, every sub-step can be enable/disable by setting the corresponding register.

Wait wakeup, you can select the wakeup source by setting PMU_WAKEUP_CFG0/1 register

Exit Low Power mode, the sub-step are executed depend on whether they were executed in enter low power step.

10.4.3 Wakeup source of AP

The wakeup source is a group of signals which can trigger PMU from power mode to normal mode, such as SDMMC detect, core interrupt, GPIO0, and gpio interrupt.

Table 10-4 Wakeup Source

Num	Wakeup Source	Description
1	software control	software control (in normal mode)
2	arm interrupt	a17 interrupt
3	pmu_gpio	gpio0, in pd_pmu
4	sdmmc0	detect_n of sdmmc0
5	gpio int	gpio interrupt outside of pd_pmu

If software expect PMU be woken up from power mode by a wake up source, it should be enabled by write 1 to the corresponding bit of PMU_WAKEUP_CFG0/1 register before entering into power mode.

Technically, wakeup source can be used in every power mode if only the path from wakeup source to PMU is not shut down.

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10.5 Register Description

10.5.1 Register Summary

Name	Offset	Size	Reset Value	Description
PMU_WAKEUP_CFG0	0x0000	W	0x00000000	PMU wake-up source configuration register0
PMU_WAKEUP_CFG1	0x0004	W	0x00000000	PMU wake-up source configuration register1
PMU_PWRDN_CON	0x0008	W	0x00000000	System power gating configuration register
PMU_PWRDN_ST	0x000c	W	0x00000000	System power gating status register
PMU_IDLE_REQ	0x0010	W	0x00000000	PMU Noc idle req control
PMU_IDLE_ST	0x0014	W	0x00000000	PMU Noc idle status
PMU_PWRMODE_CON	0x0018	W	0x00000000	PMU configuration register in power mode flow
PMU_PWR_STATE	0x001c	W	0x00000000	PMU Low power mode state
PMU_OSC_CNT	0x0020	W	0x00005dc0	24MHz OSC stabilization counter threshold
PMU_PLL_CNT	0x0024	W	0x10004000	PLL lock counter threshold
PMU_STABL_CNT	0x0028	W	0x00005dc0	External PMU stabilization counter threshold
PMU_DDR0IO_PWRON_CNT	0x002c	W	0x00005dc0	DDR0 IO power on counter threshold
PMU_DDR1IO_PWRON_CNT	0x0030	W	0x00005dc0	DDR1 IO power on counter threshold
PMU_CORE_PWRDWN_CNT	0x0034	W	0x00005dc0	CORE domain power down waiting counter in sleep mode
PMU_CORE_PWRUP_CNT	0x0038	W	0x00005dc0	CORE domain power up waiting counter in sleep mode
PMU_GPU_PWRDWN_CNT	0x003c	W	0x00005dc0	GPU domain power down waiting counter in sleep mode
PMU_GPU_PWRUP_CNT	0x0040	W	0x00005dc0	GPU domain power up waiting counter in sleep mode
PMU_WAKEUP_RST_CLR_CNT	0x0044	W	0x00005dc0	Wakeup reset deassert state wait counter in power off mode
PMU_SFT_CON	0x0048	W	0x00000000	PMU Software control in normal mode
PMU_DDR_SREF_ST	0x004c	W	0x00000000	PMU DDR self refresh status
PMU_INT_CON	0x0050	W	0x00000000	PMU interrupt configuration register
PMU_INT_ST	0x0054	W	0x00000000	PMU interrupt status register
PMU_BOOT_ADDR_SEL	0x0058	W	0x00005dc0	boot_addr_sel in power mode
PMU_GRF_CON	0x005c	W	0x00000008	grf control register

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Name	Offset	Size	Reset Value	Description
PMU_GPIO_SR	0x0060	W	0x00020000	GPIO slew rate control
PMU_GPIO0_A_PULL	0x0064	W	0x0000555a	GPIO0A input to PU/PD programmation section
PMU_GPIO0_B_PULL	0x0068	W	0x00005555	GPIO0B input to PU/PD programmation section
PMU_GPIO0_C_PULL	0x006c	W	0x00000015	GPIO0C input to PU/PD programmation section
PMU_GPIO0_A_DRV	0x0070	W	0x0000555a	GPIO0A Drive strength slector
PMU_GPIO0_B_DRV	0x0074	W	0x00005555	GPIO0B Drive strength slector
PMU_GPIO0_C_DRV	0x0078	W	0x00000015	GPIO0C Drive strength slector
PMU_GPIO_OP	0x007c	W	0x00000000	GPIO0 output value
PMU_GPIO0_SEL18	0x0080	W	0x00000006	gpio0 1.8v/3.3v sel
PMU_GPIO0_A_IOMUX	0x0084	W	0x00000000	GPIO0A iomux sel
PMU_GPIO0_B_IOMUX	0x0088	W	0x00000000	GPIO0B iomux sel
PMU_GPIO0_C_IOMUX	0x008c	W	0x00000000	GPIO0C iomux sel
PMU_PWRMODE_CON1	0x0090	W	0x00000000	PMU power mode controll1
PMU_SYS_REG0	0x0094	W	0x00000000	PMU system register0
PMU_SYS_REG1	0x0098	W	0x00000000	PMU system register1
PMU_SYS_REG2	0x009c	W	0x00000000	PMU system register2
PMU_SYS_REG3	0x00a0	W	0x00000000	PMU system register3

10.5.2 Detail Register Description

PMU_WAKEUP_CFG0

Address: Operational Base + offset (0x0000)

PMU wake-up source configuration register0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	gpio0c_2_wakeup_en GPIO0c bit2 wakeup enable 1'b0: disable 1'b1: enable
17	RW	0x0	gpio0c_1_wakeup_en GPIO0c bit1 wakeup enable 1'b0: disable 1'b1: enable
16	RW	0x0	gpio0c_0_wakeup_en GPIO0c bit0 wakeup enable 1'b0: disable 1'b1: enable
15	RW	0x0	gpio0b_7_wakeup_en GPIO0b bit7 wakeup enable 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
14	RW	0x0	gpio0b_6_wakeup_en GPIO0b bit6 wakeup enable 1'b0: disable 1'b1: enable
13	RW	0x0	gpio0b_5_wakeup_en GPIO0b bit5 wakeup enable 1'b0: disable 1'b1: enable
12	RW	0x0	gpio0b_4_wakeup_en GPIO0 bit12 wakeup enable 1'b0: disable 1'b1: enable
11	RW	0x0	gpio0b_3_wakeup_en GPIO0b bit3 wakeup enable 1'b0: disable 1'b1: enable
10	RW	0x0	gpio0b_2_wakeup_en GPIO0b bit2 wakeup enable 1'b0: disable 1'b1: enable
9	RW	0x0	gpio0b_1_wakeup_en GPIO0b bit1 wakeup enable 1'b0: disable 1'b1: enable
8	RW	0x0	gpio0b_0_wakeup_en GPIO0b bit0 wakeup enable 1'b0: disable 1'b1: enable
7	RW	0x0	gpio0a_7_wakeup_en GPIO0a bit7 wakeup enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0a_6_wakeup_en GPIO0a bit6 wakeup enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio0a_5_wakeup_en GPIO0a bit5 wakeup enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0a_4_wakeup_en GPIO0a bit4 wakeup enable 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	gpio0a_3_wakeup_en GPIO0a bit3 wakeup enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio0a_2_wakeup_en GPIO0a bit2 wakeup enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0a_1_wakeup_en GPIO0a bit1 wakeup enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0a_0_wakeup_en GPIO0a bit0 wakeup enable 1'b0: disable 1'b1: enable

PMU_WAKEUP_CFG1
Address: Operational Base + offset (0x0004)
PMU wake-up source configuration register1

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	gpioint_wakeup_en GPIO Interrupt wake enable 1'b0: disable 1'b1: enable
2	RW	0x0	sdmmc0_wakeup_en SDMMC0 wake-up enable 1'b0: disable 1'b1: enable
1	RW	0x0	pmu_gpio_wakeup_type GPIO in pmu wakeup type 1'b0: posedge 1'b1: negedge
0	RW	0x0	armint_wakeup_en ARM interrupt wake-up enable 1'b0: disable 1'b1: enable

PMU_PWRDN_CON
Address: Operational Base + offset (0x0008)
System power gating configuration register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	PD_HEVC_DWN_EN Power domain HEVC power down enable 1'b0: power on 1'b1: power off
13	RW	0x0	CHIP_PWROFF_EN software conifg power off chip logic 1'b1: power off 1'b0: not power off
12	RW	0x0	CORE_PWROFF_EN software conifg power off pd_core 1'b1: power off 1'b0: not power off
11	RW	0x0	PD_SCU_DWN_EN Power domain SCU power down enable 1'b0: power on 1'b1: power off
10	RO	0x0	reserved
9	RW	0x0	PD_GPU_DWN_EN Power domain GPU power down enable 1'b0: power on 1'b1: power off
8	RW	0x0	PD_VIDEO_DWN_EN Power domain VIDEO power down enable 1'b0: power on 1'b1: power off
7	RW	0x0	PD_VIO_DWN_EN Power domain VIO power down enable 1'b0: power on 1'b1: power off
6	RW	0x0	PD_PERI_DWN_EN Power domain PERI power down enable 1'b0: power on 1'b1: power off
5	RW	0x0	PD_BUS_DWN_EN Power domain BUS power down enable 1'b0: power on 1'b1: power off
4	RO	0x0	reserved
3	RW	0x0	PD_A17_3_DWN_EN Power Domain A17 slave core 3 power down enable 1'b0: power on 1'b1: power off

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Bit	Attr	Reset Value	Description
2	RW	0x0	PD_A17_2_DWN_EN Power Domain A17 slave core 2 power down enable 1'b0: power on 1'b1: power off
1	RW	0x0	PD_A17_1_DWN_EN Power domain A17 slave core 1 power down enable 1'b0: power on 1'b1: power off
0	RW	0x0	PD_A17_0_DWN_EN Power Domain A17 primary core power down enable 1'b0: power on 1'b1: power off

PMU_PWRDN_ST
Address: Operational Base + offset (0x000c)
System power gating status register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	l2_standywfi
12	RW	0x0	l2_flush_done
11	RO	0x0	pd_scu_pwr_st Power domain SCU power status 1'b0: power on 1'b1: power off
10	RO	0x0	pd_hevc_pwr_st Power domain HEVC power status 1'b0: power on 1'b1: power off
9	RO	0x0	pd_gpu_pwr_st Power domain GPU power status 1'b0: power on 1'b1: power off
8	RO	0x0	pd_video_pwr_st Power domain VIDEO power status 1'b0: power on 1'b1: power off
7	RO	0x0	pd_vio_pwr_st Power domain VIO power status 1'b0: power on 1'b1: power off

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Bit	Attr	Reset Value	Description
6	RO	0x0	pd_peri_pwr_st Power domain PERI power status 1'b0: power on 1'b1: power off
5	RO	0x0	pd_bus_pwr_st Power domain BUS power status 1'b0: power on 1'b1: power off
4	RO	0x0	reserved
3	RW	0x0	pd_A17_3_pwr_st Power domain A17 slave core 3 power status 1'b0: power on 1'b1: power off
2	RW	0x0	pd_A17_2_pwr_st Power domain A17 slave core 2 power status 1'b0: power on 1'b1: power off
1	RW	0x0	pd_A17_1_pwr_st Power domain A17 slave core 1 power status 1'b0: power on 1'b1: power off
0	RW	0x0	pd_A17_0_pwr_st Power domain A17 primary core power status 1'b0: power on 1'b1: power off

PMU_IDLE_REQ
Address: Operational Base + offset (0x0010)
PMU Noc idle req control

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	idle_req_hevc_cfg software config HEVC domain flush trasaction request 1'b1: idle req 1'b0: not idle req
8	RW	0x0	idle_req_cpup_cfg software config CPUP domain flush trasaction request 1'b1: idle req 1'b0: not idle req
7	RW	0x0	idle_req_dma_cfg software config DMA domain flush trasaction request 1'b1: idle req 1'b0: not idle req

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Bit	Attr	Reset Value	Description
6	RW	0x0	idle_req_alive_cfg software config ALIVE domain flush trasaction request 1'b1: idle req 1'b0: not idle req
5	RW	0x0	idle_req_core_cfg software config CORE domain flush trasaction request 1'b1: idle req 1'b0: not idle req
4	RW	0x0	idle_req_vio_cfg software config VIO domain flush trasaction request 1'b1: idle req 1'b0: not idle req
3	RW	0x0	idle_req_video_cfg software config VIDEO domain flush trasaction request 1'b1: idle req 1'b0: not idle req
2	RW	0x0	idle_req_gpu_cfg software config GPU domain flush trasaction request 1'b1: idle req 1'b0: not idle req
1	RW	0x0	idle_req_peri_cfg software config PERI domain flush trasaction request 1'b1: idle req 1'b0: not idle req
0	RW	0x0	idle_req_bus_cfg software config BUS domain flush trasaction request 1'b1: idle req 1'b0: not idle req

PMU_IDLE_ST
Address: Operational Base + offset (0x0014)
PMU Noc idle status

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	idle_ack_hevc hevc domain flush transaction acknowledge 1'b0: no ack 1'b1: ack

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Bit	Attr	Reset Value	Description
24	RW	0x0	idle_ack_cpup cpup domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
23	RW	0x0	idle_ack_dma dma domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
22	RW	0x0	idle_ack_alive ALIVE domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
21	RW	0x0	idle_ack_core core domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
20	RW	0x0	idle_ack_vio VIO domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
19	RW	0x0	idle_ack_video VIDEO domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
18	RW	0x0	idle_ack_gpu GPU domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
17	RW	0x0	idle_ack_peri PERI domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
16	RW	0x0	idle_ack_bus BUS domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
15:10	RO	0x0	reserved
9	RW	0x0	IDLE_HEVC HEVC domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
8	RW	0x0	IDLE_CPUP CPUP domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish

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Bit	Attr	Reset Value	Description
7	RW	0x0	IDLE_DMA DMA domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
6	RW	0x0	IDLE_ALIVE ALIVE domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
5	RW	0x0	IDLE_CORE CORE domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
4	RW	0x0	IDLE_VIO VIO domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
3	RW	0x0	IDLE_VIDEO VIDEO domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
2	RW	0x0	IDLE_GPU GPU domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
1	RW	0x0	IDLE_PERI PERI domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
0	RW	0x0	IDLE_BUS BUS domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish

PMU_PWRMODE_CON

Address: Operational Base + offset (0x0018)

PMU configuration register in power mode flow

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	ddr1io_ret_de_req ddr1io retention de-assert request 1'b0: de-assert request 1'b1: not de-assert request
21	RW	0x0	ddr0io_ret_de_req ddr0io retention de-assert request 1'b0: de-assert request 1'b1: not de-assert request

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Bit	Attr	Reset Value	Description
20	RW	0x0	ddrc1_gating_en ddrc1 clock auto gating after self-refresh in low power mode 1'b1: auto gating 1'b0: not auto gating
19	RW	0x0	ddr0_gating_en ddrc0 auto gating in low power mode 1'b0: disable 1'b1: enable
18	RW	0x0	ddr1io_ret_en ddr1 io ret enable in low power mode 1'b1: enable 1'b0: disable
17	RW	0x0	ddr0io_ret_en DDR0 IO retention function enable or not 1'b0: DDR0 IO retention disable 1'b1: DDR0 IO retention enable
16	RW	0x0	sref1_enter_en ddr1 enter self-refresh in low power mode 1'b1: enable 1'b0: disable
15	RW	0x0	sref0_enter_en DDR0 enter self-refresh enable in low power mode 1'b0: disable DDR0 enter self-refresh 1'b1: enable DDR0 enter self-refresh
14	RW	0x0	wakeup_reset_en wakeup reset enable if power up 1'b0: diable 1'b1: enable
13	RW	0x0	input_clamp_en input clamp enable if power off input clamp for PD_PMU enable if power off 1'b0: disable 1'b1: enable
12	RW	0x0	osc_24m_dis 24MHz OSC disable in low power mode 1'b0: 24MHz OSC enable 1'b1: 24MHz OSC disable
11	RW	0x0	pmu_use_lf pmu domain clock switch to 32.768kHz enable 1'b0: not switch to 32.768kHz 1'b1: switch to 32.768kHz

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Bit	Attr	Reset Value	Description
10	RW	0x0	alive_use_lf ALIVE domain clock switch to 32.768kHz enable 1'b0: not switch to 32.768kHz 1'b1: switch to 32.768kHz
9	RW	0x0	pwroff_comb three power off signal combination 1'b0: not combine 1'b1: combine enable
8	RW	0x0	chip_pd_en chip power down enable in power mode flow 1'b0: chip power on 1'b1: chip power off
7	RW	0x0	pll_pd_en pll power down enable in power mode flow 1'b0: pll power on 1'b1: pll power off
6	RW	0x0	scu_en scu power down enable in power mode flow 1'b0: scu power on 1'b1: scu power off
5	RW	0x0	A17_0_pd_en A17_0 power down in power mode flow 1'b0: A17_0 power on 1'b1: A17_0 power off
4	RW	0x0	bus_pd_en bus power off enable in low power mode 1'b0: bus power on 1'b1: bus power off
3	RW	0x0	l2flush_en l2 flush enable 1'b1: l2 flush enable 1'b0: l2 flush disable
2	RW	0x0	global_int_disable Global interrupt disable 1'b0: enable global interrupt 1'b1: disable global interrupt
1	RW	0x0	clk_core_src_gate_en A17 core clock source gating enable in idle mode 1'b0: enable 1'b1: disable

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Bit	Attr	Reset Value	Description
0	RW	0x0	power_mode_en power mode flow enable 1'b0: disable 1'b1: enable

PMU_PWR_STATE
Address: Operational Base + offset (0x001c)
PMU Low power mode state

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	A17_CLK_EN A17 source clock enable 1'b0: state not happened 1'b1: state happened
29	RW	0x0	TRANS_RESTORE noc trans restore 1'b0: state not happened 1'b1: state happened
28	RW	0x0	A17_0_PWRUP A17 core0 power up state 1'b0: state not happened 1'b1: state happened
27	RW	0x0	L2MEM_PWRUP pd_l2mem powerup state 1'b0: state not happened 1'b1: state happened
26	RW	0x0	SREF_EXIT ddr exit self-refresh 1'b0: state not happened 1'b1: state happened
25	RW	0x0	DDR_IO_PWRUP ddr io powerup state 1'b0: state not happened 1'b1: state happened
24	RW	0x0	BUS_PWRUP pd_bus powerup state 1'b0: state not happened 1'b1: state happened
23	RW	0x0	PLL_PWRUP pll power up state 1'b0: state not happened 1'b1: state happened
22	RW	0x0	WAKEUP_RESET_CLR deassert wakeup reset 1'b0: state not happened 1'b1: state happened

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Bit	Attr	Reset Value	Description
21	RW	0x0	ALIVE_PMU_HF pd_alive & pd_pmu switch to normal clock 1'b0: state not happened 1'b1: state happened
20	RW	0x0	X24M_OSC_EN 24MHz OSC enable 1'b0: state not happened 1'b1: state happened
19	RW	0x0	RELEASE_CLAMP release pd_pmu input clamp 1'b0: state not happened 1'b1: state happened
18	RW	0x0	EXT_PWRUP ext pmic power up 1'b0: state not happened 1'b1: state happened
17	RW	0x0	WAKEUP_RESET wakeup reset 1'b0: state not happened 1'b1: state happened
16	RW	0x0	WAIT_WAKEUP wati wakeup state 1'b0: state not happened 1'b1: state happened
15	RW	0x0	X24M_OSC_DIS 24MHz soc diable state 1'b0: state not happened 1'b1: state happened
14	RW	0x0	POWEROFF chip power off state 1'b0: state not happened 1'b1: state happened
13	RW	0x0	INPUT_CLAMP pd_pmu input clamp 1'b0: state not happened 1'b1: state happened
12	RW	0x0	PLL_PWRDN pll power down state 1'b0: state not happened 1'b1: state happened
11	RW	0x0	ALIVE_PMU_LF pd_alive&pd_pmu switch to 32khz 1'b0: state not happened 1'b1: state happened

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Bit	Attr	Reset Value	Description
10	RW	0x0	L2MEM_PWRDN l2 mem power down state 1'b0: state not happened 1'b1: state happened
9	RW	0x0	A17_0_PWRDN A17 core0 power down state 1'b0: state not happened 1'b1: state happened
8	RW	0x0	BUS_PWRDN pd_bus power down state 1'b0: A17_0 power on 1'b1: A17_0 power off
7	RW	0x0	DDR_IO_PWROFF ddr io power off 1'b0: state not happened 1'b1: state happened
6	RW	0x0	DDR_IO_RET DDR io retention 1'b0: state not happened 1'b1: state happened
5	RW	0x0	SREF_ENTER ddr selfrefresh enter 1'b0: state not happened 1'b1: state happened
4	RW	0x0	TRANS_NO_FIN transfer no finish 1'b0: state not happened 1'b1: state happened
3	RW	0x0	A17_CLK_DIS A17 clock disable 1'b0: state not happened 1'b1: state happened
2	RW	0x0	STANDBYL2 L2 Standby 1'b0: state not happened 1'b1: state happened
1	RW	0x0	L2FLUSH_REQ L2 Flush req 1'b0: state not happened 1'b1: state happened
0	RW	0x0	NORMAL normal state 1'b0: state not happened 1'b1: state happened

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PMU_OSC_CNT
Address: Operational Base + offset (0x0020)
24MHz OSC stabilization counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	osc_stabl_cnt_thresh 24MHz OSC stabilization counter threshold

PMU_PLL_CNT
Address: Operational Base + offset (0x0024)
PLL lock counter threshold

Bit	Attr	Reset Value	Description
31:20	RW	0x100	pllrst_cnt_thresh PLL reset wait counter threshold
19:0	RW	0x04000	plllock_cnt_thresh PLL lock wait counter threshold

PMU_STABL_CNT
Address: Operational Base + offset (0x0028)
External PMU stabilization counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_stabl_cnt_thresh External PMU stabilization counter threshold

PMU_DDR0IO_PWRON_CNT
Address: Operational Base + offset (0x002c)
DDR0 IO power on counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	ddr0io_pwron_cnt_thresh DDR0 IO power on counter threshold

PMU_DDR1IO_PWRON_CNT
Address: Operational Base + offset (0x0030)
DDR1 IO power on counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	ddr1io_pwron_cnt_thresh DDR1 IO power on counter threshold

PMU_CORE_PWRDWN_CNT
Address: Operational Base + offset (0x0034)
CORE domain power down waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	core_pwrdwn_cnt_thresh CORE domain power down waiting counter threshold

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PMU_CORE_PWRUP_CNT
Address: Operational Base + offset (0x0038)
CORE domain power up waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	core_pwrup_cnt_thresh CORE domain power up waiting counter threshold

PMU_GPU_PWRDWN_CNT
Address: Operational Base + offset (0x003c)
GPU domain power down waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	gpu_pwrdwn_cnt_thresh GPU domain power down waiting counter threshold

PMU_GPU_PWRUP_CNT
Address: Operational Base + offset (0x0040)
GPU domain power up waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	gpu_pwrup_cnt_thresh GPU domain power up waiting counter threshold

PMU_WAKEUP_RST_CLR_CNT
Address: Operational Base + offset (0x0044)
Wakeup reset deassert state wait counter in power off mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	wakeup_rst_clr_cnt_thresh Power off mode wakeup reset clear counter threshold

PMU_SFT_CON
Address: Operational Base + offset (0x0048)
PMU Software control in normal mode

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	l2flush_cfg l2 flush config in normal mode 1'b1: l2 flush req 1'b0: l2 flush disable
14	RW	0x0	osc_disable_cfg software config OSC disable 1'b1: OSC disable 1'b0: OSC enable

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Bit	Attr	Reset Value	Description
13	RW	0x0	osc_bypass osc bypass control 1'b0: disable 1'b1: enable
12	RW	0x0	alive_lf_ena_cfg software config ALIVE domain clock switch to 32.768kHz 1'b1: switch to 32.768kHz 1'b0: not switch
11	RW	0x0	pmu_lf_ena_cfg software config PMU domain clock switch to 32.768kHz 1'b1: switch to 32.768kHz 1'b0: not switch
10	RW	0x0	power_off_ddr1io_cfg software conifg power off DDR1 IO 1'b1: power off 1'b0: not power off
9	RW	0x0	ddr1_io_ret_cfg software config DDR1 IO retention 1'b1: retention 1'b0: not retention
8	RW	0x0	upctl1_c_sysreq_cfg software config enter DDR1 self-refresh by lowpower interface 1'b1: request enter self-refresh 1'b0: not enter self-refresh
7	RW	0x0	power_off_ddr0io_cfg software conifg power off DDR0 IO 1'b1: power off 1'b0: not power off
6	RW	0x0	ddr0_io_ret_cfg software config DDR0 IO retention 1'b1: retention 1'b0: not retention
5	RW	0x0	upctl0_c_sysreq_cfg software config enter DDR0 self-refresh by lowpower interface 1'b1: request enter self-refresh 1'b0: not enter self-refresh
4	RW	0x0	clk_core_src_gating_cfg software config A17 core clock source gating 1'b1: gating 1'b0: not gating

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Bit	Attr	Reset Value	Description
3	RW	0x0	dbgnopwrdwn3_enable ARM CORE3 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support
2	RW	0x0	dbgnopwrdwn2_enable ARM CORE2 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support
1	RW	0x0	dbgnopwrdwn1_enable ARM CORE1 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support
0	RW	0x0	dbgnopwrdwn0_enable ARM CORE0 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support

PMU_DDR_SREF_ST
Address: Operational Base + offset (0x004c)
PMU DDR self refresh status

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	upctl0_c_sysack DDR0 enter self-refresh acknowledge 1'b0: no ack 1'b1: ack
2	RW	0x0	upctl0_c_active DDR0 enter self-refresh 1'b0: no active 1'b1: active
1	RW	0x0	upctl1_c_sysack DDR1 enter self-refresh acknowledge 1'b0: no ack 1'b1: ack
0	RW	0x0	upctl1_c_active DDR1 enter self-refresh 1'b0: no active 1'b1: active

PMU_INT_CON
Address: Operational Base + offset (0x0050)
PMU interrupt configuration register

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	pd_mem_int_en Power domain L2 MEM power switch interrupt enable 1'b0: disable 1'b1: enable
26	RW	0x0	pd_hevc_int_en Power domain hevc power switch interrupt enable 1'b0: disable 1'b1: enable
25	RW	0x0	pd_gpu_int_en Power domain GPU power switch interrupt enable 1'b0: disable 1'b1: enable
24	RW	0x0	pd_video_int_en Power domain VIDEO power switch interrupt enable 1'b0: disable 1'b1: enable
23	RW	0x0	pd_vio_int_en Power domain VIO power switch interrupt enable 1'b0: disable 1'b1: enable
22	RW	0x0	pd_peri_int_en Power domain PERI power switch interrupt enable 1'b0: disable 1'b1: enable
21	RW	0x0	pd_bus_int_en Power domain BUS power switch interrupt enable 1'b0: disable 1'b1: enable
20	RO	0x0	reserved
19	RW	0x0	pd_a2_3_int_en Power domain A17 slave core 3 power switch interrupt enable 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
18	RW	0x0	pd_A17_2_int_en Power domain A17 slave core 2 power switch interrupt enable 1'b0: disable 1'b1: enable
17	RW	0x0	pd_A17_1_int_en Power domain A17 slave core 1 power switch interrupt enable 1'b0: disable 1'b1: enable
16	RW	0x0	pd_A17_0_int_en Power domain A17 primary core power switch interrupt enable 1'b0: disable 1'b1: enable
15:6	RO	0x0	reserved
5	RW	0x0	pwrmode_wakeup_int_en wakeup interrupt enable in power mode 1'b0: disable 1'b1: enable
4	RW	0x0	gpioint_wakeup_int_en gpio interrupt wakeup interrupt enable 1'b0: disable 1'b1: enable
3	RW	0x0	sdmmc0_wakeup_int_en SDMMC0 wakeup status interrupt enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio_wakeup_int_en GPIO0 wakeup status interrupt enable 1'b0: disable 1'b1: enable
1	RW	0x0	armint_wakeup_int_en ARM interrupt wakeup status interrupt enable 1'b0: disable 1'b1: enable
0	RW	0x0	pmu_int_en PMU interrupt enable 1'b0: disable 1'b1: enable

PMU_INT_ST

Address: Operational Base + offset (0x0054)

PMU interrupt status register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	pd_mem_int_st Power domain l2 mem power switch status 1'b0: no power switch happen 1'b1: power switch happen
26	RW	0x0	pd_hevc_int_st Power domain HEVC power switch status 1'b0: no power switch happen 1'b1: power switch happen
25	W1C	0x0	pd_gpu_int_st Power domain GPU power switch status 1'b0: no power switch happen 1'b1: power switch happen
24	W1C	0x0	pd_video_int_st Power domain VIDEO power switch status 1'b0: no power switch happen 1'b1: power switch happen
23	W1C	0x0	pd_vio_int_st Power domain VIO power switch status 1'b0: no power switch happen 1'b1: power switch happen
22	W1C	0x0	pd_peri_int_st Power domain PERI power switch status 1'b0: no power switch happen 1'b1: power switch happen
21	W1C	0x0	pd_bus_int_st Power domain BUS power switch status 1'b0: no power switch happen 1'b1: power switch happen
20	RO	0x0	reserved
19	RW	0x0	pd_A17_3_int_st Power domain A17 slave core 3 power switch status 1'b0: no power switch happen 1'b1: power switch happen
18	RW	0x0	pd_A17_2_int_st Power domain A17 slave core 2 power switch status 1'b0: no power switch happen 1'b1: power switch happen
17	RW	0x0	pd_A17_1_int_st Power domain A17 slave core 1 power switch status 1'b0: no power switch happen 1'b1: power switch happen

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Bit	Attr	Reset Value	Description
16	RW	0x0	pd_A17_0_int_st Power domain A17 primary core power switch status 1'b0: no power switch happen 1'b1: power switch happen
15:5	RO	0x0	reserved
4	RW	0x0	pwrmode_wakeup_event_trig power mode flow wakeup 1'b0: no wakeup 1'b1: wakeup
3	RW	0x0	gpioint_wakeup_event_trig ARM interrupt wake-up enent trigger 1'b0: no wakeup 1'b1: wakeup
2	W1C	0x0	sdmmc0_wakeup_event_trig SDMMC0 wake-up enent trigger 1'b0: no wakeup 1'b1: wakeup
1	W1C	0x0	gpio_wakeup_event_trig GPIO0 wake-up enent trigger 1'b0: no wakeup 1'b1: wakeup
0	RW	0x0	armint_wakeup_event_trig ARM interrupt wake-up enent trigger 1'b0: no wakeup 1'b1: wakeup

PMU_BOOT_ADDR_SEL
Address: Operational Base + offset (0x0058)
boot_addr_sel in power mode

Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	boot_addr_sel boot addr sel when wakeup from power mode

PMU_GRF_CON
Address: Operational Base + offset (0x005c)
grf control register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:10	RW	0x00	GRF_NPOR_CRNT_CTRL Npor signal crnt control register
9:4	RW	0x00	GRF_TEST_CRNT_CTRL Test signal crnt control register
3:2	RW	0x2	GRF_X32K_CRNT_CTRL X32K signal crnt control register

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	GRF_X24M_CRNT_CTRL X24M signal crnt control register

PMU_GPIO_SR
Address: Operational Base + offset (0x0060)
GPIO slew rate control

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	gpio0_c2_sr gpio0_c2 slew rate control 1'b0: slow (half frequency) 1'b1: fast
17	RW	0x1	gpio0_c1_sr gpio0_c1 slew rate control 1'b0: slow (half frequency) 1'b1: fast
16	RW	0x0	gpio0_c0_sr gpio0_c0 slew rate control 1'b0: slow (half frequency) 1'b1: fastl
15	RW	0x0	gpio0_b7_sr gpio0_b7 slew rate control 1'b0: slow (half frequency) 1'b1: fast
14	RW	0x0	gpio0_b6_sr gpio0_b6 slew rate control 1'b0: slow (half frequency) 1'b1: fast
13	RW	0x0	gpio0_b5_sr gpio0_b5 slew rate control 1'b0: slow (half frequency) 1'b1: fast
12	RW	0x0	gpio0_b4_sr gpio0_b4 slew rate control 1'b0: slow (half frequency) 1'b1: fast
11	RW	0x0	gpio0_b3_sr gpio0_b3 slew rate control 1'b0: slow (half frequency) 1'b1: fast
10	RW	0x0	gpio0_b2_sr gpio0_b2 slew rate control 1'b0: slow (half frequency) 1'b1: fast

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Bit	Attr	Reset Value	Description
9	RW	0x0	gpio0_b1_sr gpio0_b1 slew rate control 1'b0: slow (half frequency) 1'b1: fast
8	RW	0x0	gpio0_b0_sr gpio0_b0 slew rate control 1'b0: slow (half frequency) 1'b1: fast
7	RW	0x0	gpio0_a7_sr gpio0_a7 slew rate control 1'b0: slow (half frequency) 1'b1: fastll
6	RW	0x0	gpio0_a6_sr gpio0_a6 slew rate control 1'b0: slow (half frequency) 1'b1: fast
5	RW	0x0	gpio0_a5_sr gpio0_a5 slew rate control 1'b0: slow (half frequency) 1'b1: fast
4	RW	0x0	gpio0_a4_sr gpio0_a4 slew rate control 1'b0: slow (half frequency) 1'b1: fast
3	RW	0x0	gpio0_a3_sr gpio0_a3 slew rate control 1'b0: slow (half frequency) 1'b1: fast
2	RW	0x0	gpio0_a2_sr gpio0_a2 slew rate control 1'b0: slow (half frequency) 1'b1: fast
1	RW	0x0	gpio0_a1_sr gpio0_a1 slew rate control 1'b0: slow (half frequency) 1'b1: fast
0	RW	0x0	gpio0_a0_sr gpio0_a0 slew rate control 1'b0: slow (half frequency) 1'b1: fast

PMU_GPIO0_A_PULL
Address: Operational Base + offset (0x0064)
GPIO0A input to PU/PD programmation section

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x1	gpio0_a7_pull gpio0_a7 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
13:12	RW	0x1	gpio0_a6_pull gpio0_a6 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
11:10	RW	0x1	gpio0_a5_pull gpio0_a5 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
9:8	RW	0x1	gpio0_a4_pull gpio0_a4 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
7:6	RW	0x1	gpio0_a3_pull gpio0_a3 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
5:4	RW	0x1	gpio0_a2_pull gpio0_a2 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio0_a1_pull gpio0_a1 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
1:0	RW	0x2	gpio0_a0_pull gpio0_a0 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

PMU_GPIO0_B_PULL
Address: Operational Base + offset (0x0068)
GPIO0B input to PU/PD programmation section

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_b7_pull gpio0_b7 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
13:12	RW	0x1	gpio0_b6_pull gpio0_b6 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
11:10	RW	0x1	gpio0_b5_pull gpio0_b5 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	gpio0_b4_pull gpio0_b4 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
7:6	RW	0x1	gpio0_b3_pull gpio0_b3 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
5:4	RW	0x1	gpio0_b2_pull gpio0_b2 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
3:2	RW	0x1	gpio0_b1_pull gpio0_b1 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
1:0	RW	0x1	gpio0_b0_pull gpio0_b0 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

PMU_GPIO0_C_PULL

Address: Operational Base + offset (0x006c)

GPIO0C input to PU/PD programmation section

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	gpio0_c2_pull gpio0_c2 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
3:2	RW	0x1	gpio0_c1_pull gpio0_c1 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
1:0	RW	0x1	gpio0_c0_pull gpio0_c0 pu/pd programmation section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

PMU_GPIO0_A_DRV
Address: Operational Base + offset (0x0070)
GPIO0A Drive strength slector

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_a7_e gpio0_a7 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
13:12	RW	0x1	gpio0_a6_e gpio0_a6 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

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Bit	Attr	Reset Value	Description
11:10	RW	0x1	gpio0_a5_e gpio0_a5 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
9:8	RW	0x1	gpio0_a4_e gpio0_a4 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
7:6	RW	0x1	gpio0_a3_e gpio0_a3 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
5:4	RW	0x1	gpio0_a2_e gpio0_a2 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
3:2	RW	0x2	gpio0_a1_e gpio0_a1 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
1:0	RW	0x2	gpio0_a0_e gpio0_a0 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMU_GPIO0_B_DRV
Address: Operational Base + offset (0x0074)
GPIO0B Drive strength slector

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_b7_e gpio0_b7 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
13:12	RW	0x1	gpio0_b6_e gpio0_b6 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
11:10	RW	0x1	gpio0_b5_e gpio0_b5 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
9:8	RW	0x1	gpio0_b4_e gpio0_b4 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
7:6	RW	0x1	gpio0_b3_e gpio0_b3 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
5:4	RW	0x1	gpio0_b2_e gpio0_b2 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	gpio0_b1_e gpio0_b1 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
1:0	RW	0x1	gpio0_b0_e gpio0_b0 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMU_GPIO0_C_DRV
Address: Operational Base + offset (0x0078)
GPIO0C Drive strength slector

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x1	gpio0_c2_e gpio0_c2 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
3:2	RW	0x1	gpio0_c1_e gpio0_c1 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
1:0	RW	0x1	gpio0_c0_e gpio0_c0 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMU_GPIO_OP
Address: Operational Base + offset (0x007c)
GPIO0 output value

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	gpio0_c2_op gpio0_c2 output value
17	RW	0x0	gpio0_c1_op gpio0_c1 output value
16	RW	0x0	gpio0_c0_op gpio0_c0 output value
15	RW	0x0	gpio0_b7_op gpio0_b7 output value
14	RW	0x0	gpio0_b6_op gpio0_b6 output value
13	RW	0x0	gpio0_b5_op gpio0_b5 output value
12	RW	0x0	gpio0_b4_op gpio0_b4 output value
11	RW	0x0	gpio0_b3_op gpio0_b3 output value
10	RW	0x0	gpio0_b2_op gpio0_b2 output value
9	RW	0x0	gpio0_b1_op gpio0_b1 output value
8	RW	0x0	gpio0_b0_op gpio0_b0 output value
7	RW	0x0	gpio0_a7_op gpio0_a7 output value
6	RW	0x0	gpio0_a6_op gpio0_a6 output value
5	RW	0x0	gpio0_a5_op gpio0_a5 output value
4	RW	0x0	gpio0_a4_op gpio0_a4 output value
3	RW	0x0	gpio0_a3_op gpio0_a3 output value
2	RW	0x0	gpio0_a2_op gpio0_a2 output value
1	RW	0x0	gpio0_a1_op gpio0_a1 output value
0	RW	0x0	gpio0_a0_op gpio0_a0 output value

PMU_GPIO0_SEL18
Address: Operational Base + offset (0x0080)
gpio0 1.8v/3.3v sel

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x1	gpio0_c0_smt
1	RW	0x1	gpio0_b7_smt gpio0_a0 output value
0	RW	0x0	gpio0_a0_op gpio0_a0 output value 1'b0: >=2.5v 1'b1: <=1.8v

PMU_GPIO0_A_IOMUX
Address: Operational Base + offset (0x0084)
GPIO0A iomux sel

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RW	0x0	gpio0_a3 iomux 1'b0: gpioa3 1'b1: ddr1_retention
5	RO	0x0	reserved
4	RW	0x0	gpio0_a2 iomux 1'b0: gpioa2 1'b1: ddr0_retention
3	RO	0x0	reserved
2	RW	0x0	gpio0_a1 iomux 1'b0: gpioa1 1'b1: ddrio_pwroff
1	RO	0x0	reserved
0	RW	0x0	gpio0_a0 iomux 1'b0: gpioa0 1'b1: global_pwroff

PMU_GPIO0_B_IOMUX
Address: Operational Base + offset (0x0088)
GPIO0B iomux sel

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	gpio0_b7 iomux 1'b0: gpiob7 1'b1: i2c0pmu_sda
13:11	RO	0x0	reserved
10	RW	0x0	gpio0_b5 iomux 1'b0: gpiob5 1'b1: CLK_27M
9:5	RO	0x0	reserved
4	RW	0x0	gpio0_b2 iomux 1'b0: gpiob2 1'b1: tsadc_int
3:0	RO	0x0	reserved

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PMU_GPIO0_C_IOMUX
Address: Operational Base + offset (0x008c)
GPIO0C iomux sel

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x0	gpio0_c1 iomux 2'b00: gpioc1 2'b01: test_clkout 2'b10: clkt1_27m 2'b11: reserved
1	RO	0x0	reserved
0	RW	0x0	gpio0_c0 iomux 1'b0: gpioc0 1'b1: i2c0pmu_scl

PMU_PWRMODE_CON1
Address: Operational Base + offset (0x0090)
PMU PowerMode CON1

Bit	Attr	Reset Value	Description
31:10	-	0x0	reserved
9	RW	0x0	clr_vio issue idle_req_vio in low power mode 1'b0: not issue 1'b1: issue
8	RW	0x0	clr_hevc issue idle_req_hevc in low power mode 1'b0: not issue 1'b1: issue
7	RW	0x0	clr_video issue idle_req_video in low power mode 1'b0: not issue 1'b1: issue
6	RW	0x0	clr_gpu issue idle_req_gpu in low power mode 1'b0: not issue 1'b1: issue
5	RW	0x0	clr_peri issue idle_req_peri in low power mode 1'b0: not issue 1'b1: issue
4	RW	0x0	clr_dma issue idle_req_dma in low power mode 1'b0: not issue 1'b1: issue

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Bit	Attr	Reset Value	Description
3	RW	0x0	clr_alive issue idle_req_alive in low power mode 1'b0: not issue 1'b1: issue
2	RW	0x0	clr_cpup issue idle_req_cpup in low power mode 1'b0: not issue 1'b1: issue
1	RW	0x0	clr_core issue idle_req_core in low power mode 1'b0: not issue 1'b1: issue
0	RW	0x0	clr_bus issue idle_req_bus in low power mode 1'b0: not issue 1'b1: issue

PMU_SYS_REG0
Address: Operational Base + offset (0x0094)
PMU system register0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg0 PMU system register0

PMU_SYS_REG1
Address: Operational Base + offset (0x0098)
PMU system register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg1 PMU system register1

PMU_SYS_REG2
Address: Operational Base + offset (0x009c)
PMU system register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg2 PMU system register2

PMU_SYS_REG3
Address: Operational Base + offset (0x00a0)
PMU system register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg3 PMU system register3

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10.6 Timing Diagram

10.6.1 Each domain power switch timing

The following figure is the each domain power down and power up timing.

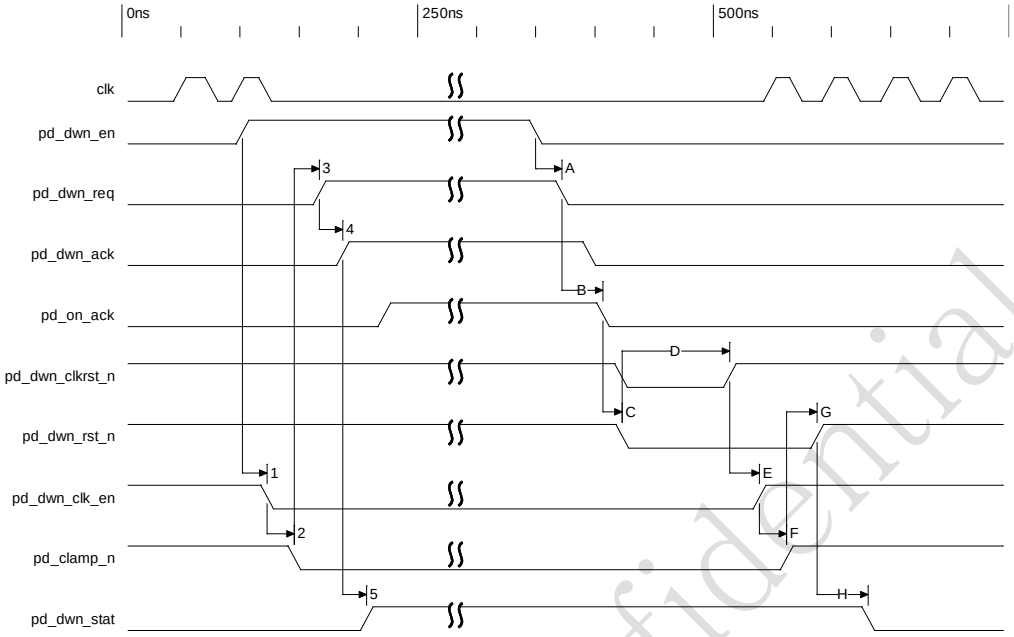

Fig. 10-3 Each Domain Power Switch Timing

10.6.2 External wakeup PAD timing

The PMU supports a lot of external wakeup sources, such as SD/MMDC, USBDEV, SIM0/1 detect wakeup, GPIO0 wakeup source and so on. All these external wakeup sources must meet the timing requirement (at least 200us) when the wakeup event is asserted. The following figure gives the timing information.

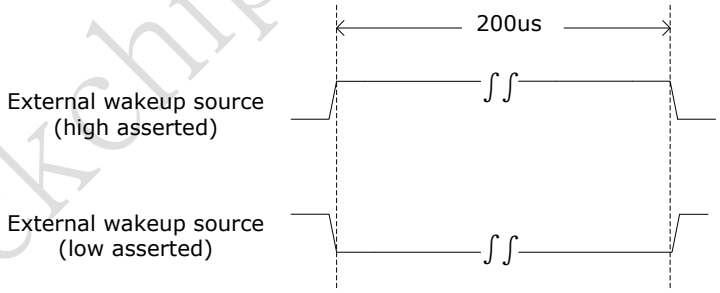

Fig. 10-4 External Wakeup Source PAD Timing

10.7 Application Notes

10.7.1 Recommend configurations for power mode.

The PMU is a design with great flexibilities, but just for facilities and inheritances, a group of recommend configurations will be shown below for software. And for convenience, we will define several modes.

The RK3288 can support following 5 recommended power modes:

- normal
- idle mode
- deep idle mode
- sleep mode
- power off mode

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The following table lists the detailed description of the modes.

Table 10-5 Power Domain Status Summary in all Work Mode

Power Domain		Power Mode				
		Mode0(normal)	Mode1(idle)	Mode2(didle)	Mode3(sleep)	Mode4(poweroff)
VD_CORE	PD_A17_0	Running	Standby	Power off	Power off	Power off
	PD_A17_1	Running/Standby/Power off	Running/Standby/Power off	Power off	Power off	Power off
	PD_A17_2	Running/Standby/Power off	Running/Standby/Power off	Power off	Power off	Power off
	PD_A17_3	Running/Standby/Power off	Running/Standby/Power off	Power off	Power off	Power off
	PD_SCU	Running	Running	Running	Power off	Power off
	PD_CS	Power on	Power off	Running	Power off	Power off
	PD_MEM	Runing	Runing	Running	Power off	Power off
PD_BUS		Power on	Power on	Running	Power off	Power off
PD_PERI		Power on	Power on/off	Power on/off	Power off	Power off
PD_VIO		Power on	Power on/off	Power on/off	Power off	Power off
PD_VIDEO		Power on	Power on/off	Power on/off	Power off	Power off
PD_HEVC		Power on	Power on/off	Power on/off	Power off	Power off
PD_GPU		Power on	Power on/off	Power on/off	Power off	Power off
PD_ALIVE		Power on	Power on	Power on	Power on. Clocked by 24MHz or 32KHz	Power off
PD_PMU		Power on	Power on	Power on	Power on. Clocked by 24MHz or 32KHz	Power on. Clocked by 32KHz
PLL		All PLLs on	All PLLs on	All PLLs on	ALL PLLs off	ALL PLLs off
OSC_24MHz		OSC enable	OSC enable	OSC enable	OSC enable/disable	OSC disable
DDR		Running	Running	Self refresh	Self refresh	Self refresh
Wakeup Sources		Software control to wake up all the module in power off or clock off states	1. all arm interrupts (include EVENTI input) 2. sdmmc0 detect_n 3. gpio int(not gpio0) 4. gpio0 io	1. all arm interrupts (include EVENTI input) 2. sdmmc0 detect_n 3. gpio int(not gpio0) 4. gpio0 io	1. sdmmc0 detect_n 2. gpio io int(not gpio0) 3. gpio0 io	GPIO0 IO

Normal mode

In this mode, you can power off/on or enable/disable the following power domain to save power: PD_PERI/PD_VIO/PD_VIDEO/PD_HEVC/PD_GPU

Idle mode

This mode is used when the core do not have load for a shot while such as waiting for interrupt and the software want to save power by gating Cortex-A17 source clock.

In idle mode, core1/2/3 of Cortex-A17 should be either power off or in WFI/WFE state. The core0 of A17 should be in WFI/WFE state. The configurations of core clock source gating and disable global interrupt are presented. The Cortex-A17 can waked up by an interrupt.

Deep idle mode

Deep idle mode is used in the scenario of audio player. In deep idle mode, powering off Cortex-A17 cores or VD_CORE voltage domain is operational, and others are same as normal mode.

In deep idle mode, you can set ddr enter the self-refresh, and power off DDRIO and enable DDR retention function in this mode, but it will takes a longer time for the recovery of DDR IO.

Sleep mode

The sleep mode can power off all power domains except PD_ALIVE. The VD_CORE is turned off externally, PD_BUS power off by hardware, and other domains power off by software.

In sleep mode the clock of PD_ALIVE can be switched from 24MHz to 32.768kHz optionally by hardware.

In sleep mode all PLLs power down mandatorily to save power by hardware.

In sleep mode OSC can be disabled optionally by hardware.

In sleep mode DDR self-refresh can be issued by hardware mandatorily.

In sleep mode DDR IO can power off and enter retention optionally by hardware.

Power off mode

The power off mode turns off the power of all VD_LOGIC externally.

In power off mode all PLLs power down mandatorily to save power by hardware.

In power off mode OSC disable request should be send by hardware.

In power off mode DDR self-refresh should be issued mandatorily by hardware.

In power off mode DDR IO can power off and enter retention optionally by hardware.

10.7.2 System Register

PMU support 4 words register: PMU_SYS_REG0, PMU_SYS_REG1, PMU_SYS_REG2, PMU_SYS_REG3. These registers are always on no matter what low power mode. So software can use these registers to retain some information which is useful after wakeup from any mode.

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10.7.3 Configuration Constraint

In order to shut down the power domains correctly, the software must obey the rules bellow:

Send NIU request to the NIU in power domain that you want to shut down.

Querying PMU_NOC_ST register to get the information until the pacific NIU is in idle state.

Send power request to the power domain through PMU_PWRDN_CON register.

Querying PMU_PWRDN_ST register to make sure the pacific power domain is power down.

The power domains controlled only by software are showing below:

PD_VIO, PD_PERI, PD_GPU, PD_VIDEO, PD_HEVC, and PD_A17_1 and PD_A17_2 to PD_A17_3.

So you must power off these power domains before enter low power mode if you need.

10.7.4 Poweroff Request Combine

There is only two poweroff request, one is for VD_CORE and VD_LOGIC (power_off_req), another is for DDRIO (power_off_ddrio).

POWER_OFF_REQ

In normal mode, If you set the chip power down (bit[13] of PMU_PWRDN_CON), or set core power down (bit[12] of PMU_PWRDN_CON), the power_off_req will be set to 1 immediate.

In Low Power mode, if you set the chip power down (bit[8] of PMU_PWRMODE_CON) or set core power down (bit[6] of PMU_PWRMODE_CON), the power_off_req will be set to 1 at the sub-step POWEROFF.

POWER_OFF_DDRIO

In normal mode, If you set the power_off_ddr0io_cfg (bit[7] of PMU_SFT_CON), or set power_off_ddr1io_cfg (bit[10] of PMU_SFT_CON), the power_off_ddrio will be set to 1 immediate.

In Low Power mode, if you set the ddr0io_ret_en (bit[17] of PMU_PWRMODE_CON) or set ddr1io_ret_en (bit[18] of PMU_PWRMODE_CON), the power_off_ddrio will be set to 1 at the sub-step DDR_IO_POWEROFF.

In Low Power mode, if you set pwroff_comb (bit[9] of PMU_PWRMODE_CON) at same time, the power_off_ddrio would not be set to 1, and the power_off_req would be set to 1 at the sub-step DDR_IO_POWEROFF.

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Chapter 11 Memory-Management-Unit (MMU)

11.1 Overview

An MMU controls address translation, access permissions, memory attribute.determination, and checking at a memory system level.
The MMU used in other modules will be introduced below.

11.2 Block Diagram

The MMU divides memory into 4KB pages, where each page can be individually configured.
The MMU uses a 2-level page table structure:
1. The first level, the Page Directory consists of 1024 Directory Table Entries (DTEs), each pointing to a Page Table.
2. The second level, the Page Table consists of 1024 Page Table Entries (PTEs), each pointing to a page in memory
Fig. 11-1 shows the structure of the two-level page table.

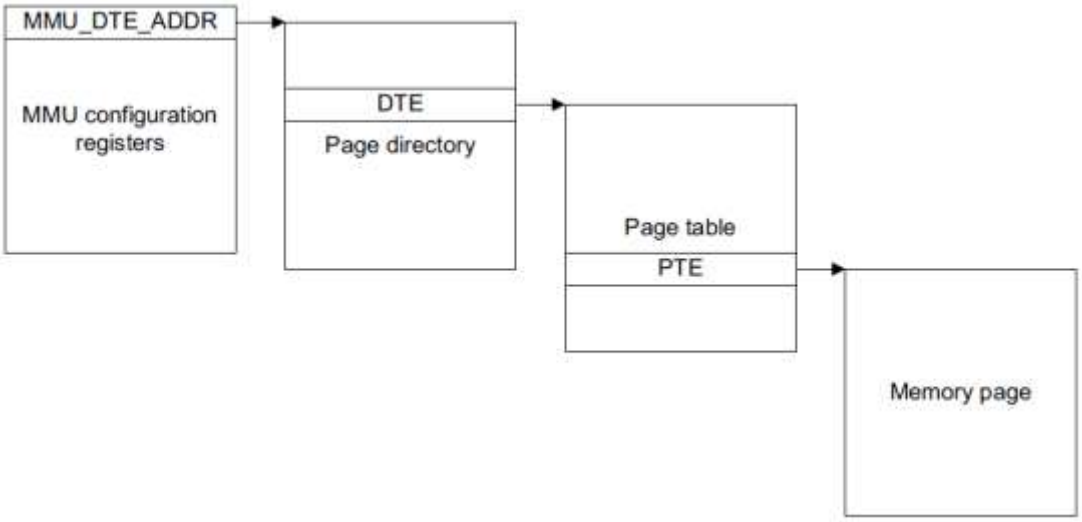

Fig. 11-1 Power Domain Partition

Fig. 11-2 shows the arrangement of the MMU address bits.

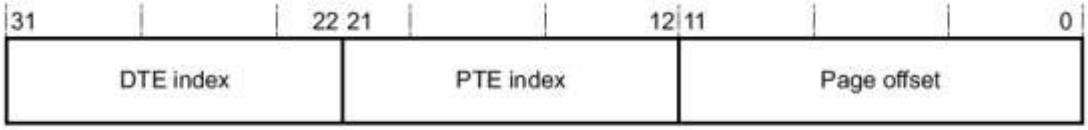

Fig. 11-2 Power Domain Partition

The MMU uses the following algorithm to translate an address:

1. Find the DTE at address given by:
MMU_DTE_ADDR + (4 * DTE index)
2. Find the PTE at address given by:
Page table address from DTE + (4 * PTE index)
3. Calculate effective address as follows:
Page address from PTE + Page offset.

The page directory is a 4KB data structure that contains 1024 32-bit DTEs. The page directory

must align at a 4KB boundary in memory.

Each DTE contains the address of a page table and a page table present bit. The system:

• initializes the entire page directory before use
• clears the page table present bit for any DTE that does not point to a valid page table.

Fig. 11-3 shows the page bit assignments.

Fig. 11-3 Page directory entry bit assignments

Bits	Name	Function
[31:12]	Page table address	This field stores bits [31:12] of the address for a page table
[11:1]	Reserved	Reserved, write as zero
[0]	Page table present	This bit indicates when the page table address points to a valid page table. 0 = page table not valid 1= page table valid.

The page table is a 4KB data structure containing 1024 32-bit PTEs. The page table must be aligned at a 4KB boundary in memory.

Each PTE contains the address of a page of memory, a Page Table present bit, and Read/Write Permission bits. The entire Page Table must be initialized before use, and any PTE not pointing to a valid page must clear the Page Present bit.

Fig.11-3 shows the page table entry bit assignments.

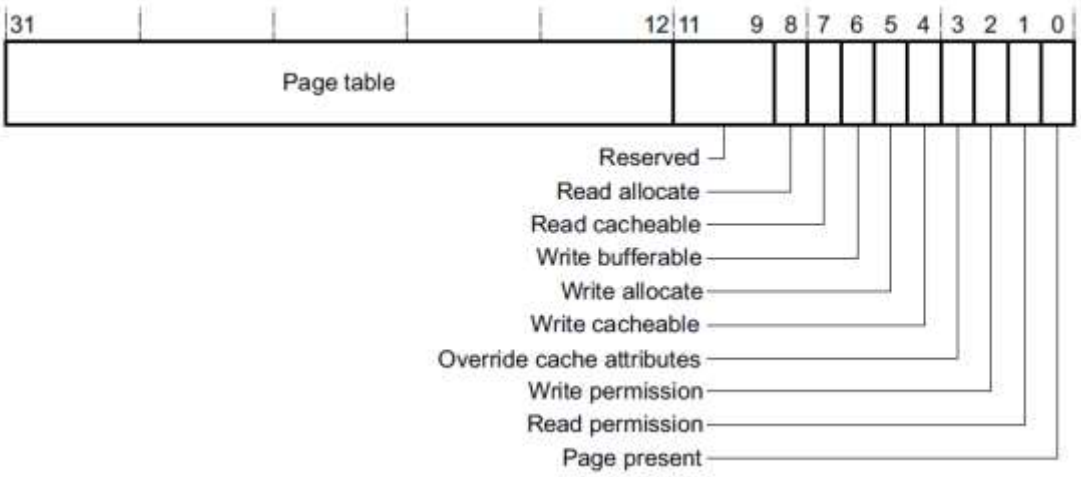

Fig. 11-4 Page directory entry bit assignments

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Bits	Name	Function
[31:12]	Page table address	This field stores bits [31:12] of the address for a page table
[11:9]	Reserved	Reserved, write as zero
[8]	Read allocate	If set, allocate cache space on read misses. Must not be set if the Read cacheable bit is not set. Only used for reads, if the Override cache attributes bit is set.
[7]	Read cacheable	If set, enable caching or prefetching of data. Only used for reads, if the Override cache attributes bit is set.
[6]	Write bufferable	If set, enable write to be delayed on their way to memory. Only used for writes, if the Override cache attributes bit is set.
[5]	Write allocate	If set, allocate cache space on write misses. Must not be set if the Write cachecable bit is not set. Only used for writes, if the Override cache attributes is set.
[4]	Write cachecable	If set, enable different writes to be merged together. Only used for writes, if the Override cache attributes bit is set.
[3]	Override cache attributes	If set, the cacheability attributes specified in bits [8:4] are used to control the cache attribytes used on the memory bus. If cleared, the default cacheability attributes from the specific processors are used on the system bus.
[2]	Write permission	Enable write accesses to the page, if present.
[1]	Read permission	Enable read accesses from the page, if present.
[0]	Page present	This bit indicates when the page table field points to a valid page. 0 = page not valid 1 = page valid.

11.3 Register Description

11.3.1 Register Summary

Name	Offset	Size	Reset Value	Description
MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page table address
MMU_STATUS	0x0004	W	0x00000018	MMU status register
MMU_CMD	0x0008	W	0x00000000	MMU command register
MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logic address of last page fault register
MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU zap cache line register
MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
MMU_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register
MMU_INT_MASK	0x001c	W	0x00000000	MMU interrupt mask register
MMU_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register

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Name	Offset	Size	Reset Value	Description
MMU_AUTO_GATING	0x0024	W	0x00000000	clock atuo gating register

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

11.3.2 Detail Register Description

MMU_DTE_ADDR
Address: Operational Base + offset (0x0000)
MMU current page table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr page table address

MMU_STATUS
Address: Operational Base + offset (0x0004)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RO	0x0	mmu_page_fault_is_write The direction of access for last page fault: 0: read 1:write
4	RO	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty.
3	RO	0x1	mmu_idle the MMu is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: the MMU can be idle in page fault mode.
2	RO	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	mmu_page_fault_active MMU page fault mode currently enabled.The mode is enabled by command
0	RO	0x0	mmu_paging_enabled mmu paging is enabled.

MMU_CMD
Address: Operational Base + offset (0x0008)
MMU command register

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	mmu_cmd 0: MMU_ENABLE_PAGING. enable paging. 1: MMU_DISABLE_PAGING. disable paging. 2: MMU_ENABLE_STALL. turn on stall mode. 3: MMU_DISABLE_STALL. turn off stall mode. 4: MMU_ZAP_CACHE. zap the entire page table cache. 5: MMU_PAGE_FAULT_DONE. leave page fault mode. 6: MMU_FORCE_RESET. reset the mmu. The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled.

MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000c)
MMU logic address of last page fault register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu_page_fault_addr address of last page fault

MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x0010)
MMU zap cache line register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line address to be invalidated from the page table cache.

MMU_INT_RAWSTAT
Address: Operational Base + offset (0x0014)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	read_bus_error read bus error
0	RO	0x0	page_fault page fault

MMU_INT_CLEAR
Address: Operational Base + offset (0x0018)
MMU interrupt clear register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_clear read bus error interrupt clear. write 1 to this register can clear read bus error interrupt.

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Bit	Attr	Reset Value	Description
0	RW	0x0	page_fault_clear page fault interrupt clear, write 1 to this register can clear page fault interrupt.

MMU_INT_MASK
Address: Operational Base + offset (0x001c)
MMU interrupt mask register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_int_en read bus error interrupt enable
0	RW	0x0	page_fault_int_en page fault interrupt enable

MMU_INT_STATUS
Address: Operational Base + offset (0x0020)
MMU interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error interrupt
0	RO	0x0	page_fault page fault interrupt

MMU_AUTO_GATING
Address: Operational Base + offset (0x0024)
clock atuo gating register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_atuo_gating mmu clock auto gating when it is 1, the mmu will auto gating itself

11.4 MMU Base address

The table below shows the MMU base address in different modules.

ISP_MMU0_BASE	ISP_BASEADDR + 0x4000
ISP_MMU1_BASE	ISP_BASEADDR + 0x5000
VOP_BIG_MMU_BASE	VOP_BIG_BASEADDR + 0x300
VOP_LIT_MMU_BASE	VOP_LIT_BASEADDR + 0x300
IEP_MMU_BASE	IEP_BASE + 0x800

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VIP_MMU_BASE	VIP_BASE + 0x800

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Chapter 12 Timer

12.1 Overview

Timer is a programmable timer peripheral. This component is an APB slave device.
Timer0~4 and Timer6 count down from a programmed value and generate an interrupt when the count reaches zero.
Timer5 and Timer7 count up from zero to a programmed value and generate an interrupt when the count reaches the programmed value.
Timer supports the following features:

- Two APB timers in the soc system. One is in the alive subsystem, include two programmable 64 bits timer channel, acts as TIMER6 and TIMER7; The other is in the cpu subsystem, include six programmable 64 bits timer channel, acts as TIMER0, TIMER1, TIMER2, TIMER3, TIMER4, and TIMER5 respectively.
- Two operation modes: free-running and user-defined count.
- Maskable for each individual interrupt.
- TIMER5 is used for gpu ; TIMER7 is used for core.

12.2 Block Diagram

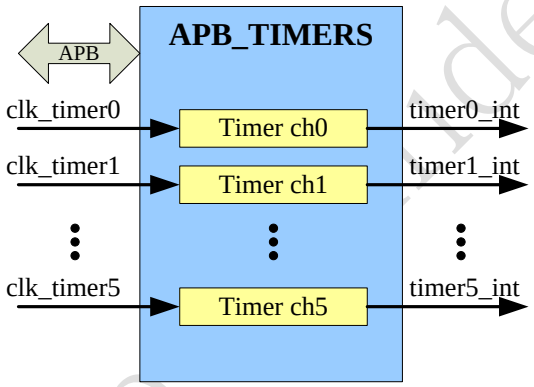

Fig. 12-1 Timers Block Diagram

The above figure shows the architecture of the APB timers (include six programmable timer channel) that in the cpu subsystem. The other APB timers that in the alive subsystem only include one programmable timer channel.

12.3 Function description

12.3.1 Timer clock

TIMER0, TIMER1, TIMER2, Timer3, TIMER4 and TIMER5 are in the CPU subsystem, using timer ch0 ~ ch5 respectively. The timer clock is 24MHz OSC.
TIMER6 and TIMER7 are in the ALIVE subsystem, using timer ch0 ~ ch1. The timer clock is 24MHz OSC.

12.3.2 Programming sequence

1. Initialize the timer by the TIMERn_CONTROLREG (0≤n≤5) register:

- Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
- Program the timer mode—user-defined or free-running—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
- Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).

2. Load the timer count value into the TIMERn_LOAD_COUNT1 (0≤n≤5) and TIMERn_ LOAD_COUNT0 (0≤n≤5) register.

3. Enable the timer by writing a "1" to bit 0 of TIMERn_CONTROLREG (0≤n≤5).

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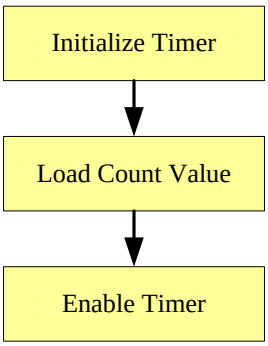

Fig. 12-2 Timer Usage Flow

12.3.3 Loading a timer count value

The initial value for each timer — that is, the value from which it counts down — is loaded into the timer using the load count register (TIMERn_LOAD_ COUNT1 (0≤n≤5) and TIMERn_ LOAD_COUNT0 (0≤n≤5)). Two events can cause a timer to load the initial value from its load count register:

- Timer is enabled after reset or disabled.
- Timer counts down to 0, when timer is configured into free-running mode.

12.3.4 Timer mode selection

- User-defined count mode – Timer loads TIMERn_LOAD_COUNT1 (0≤n≤5) and TIMERn_ LOAD_ COUNT0 (0≤n≤5) register as initial value. Timer will not automatically load the count register, when timer counts down to 0. User need to disable timer firstly and follow the programming sequence to make timer work again.
- Free-running mode – Timer loads the TIMERn_LOAD_COUNT1 (0≤n≤5) and TIMERn_ LOAD_ COUNT0 (0≤n≤5) register as initial value. Timer will automatically load the count register, when timer counts down to 0.

12.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses.

12.4.1 Registers Summary

Timer0 - Timer5
Base = 0xff6b_0000

Name	Offset	Size	Reset Value	Description
TIMER0_LOAD_COUNT0	0x0000	W	0x00000000	Timer0 Load Count Register
TIMER0_LOAD_COUNT1	0x0004	W	0x00000000	Timer0 Load Count Register
TIMER0_CURRENT_VALUE0	0x0008	W	0x00000000	Timer0 Current Value Register
TIMER0_CURRENT_VALUE1	0x000C	W	0x00000000	Timer0 Current Value Register
TIMER0_CONTROLREG	0x0010	W	0x00000000	Timer0 Control Register
TIMER0_INTSTATUS	0x0018	W	0x00000000	Timer0 Interrupt Status Register
TIMER1_LOAD_COUNT0	0x0020	W	0x00000000	Timer1 Load Count Register
TIMER1_LOAD_COUNT1	0x0024	W	0x00000000	Timer1 Load Count Register
TIMER1_CURRENT_VALUE0	0x0028	W	0x00000000	Timer1 Current Value Register
TIMER1_CURRENT_VALUE1	0x002c	W	0x00000000	Timer1 Current Value Register
TIMER1_CONTROLREG	0x0030	W	0x00000000	Timer1 Control Register
TIMER1_INTSTATUS	0x0038	W	0x00000000	Timer1 Interrupt Status Register
TIMER2_LOAD_COUNT0	0x0040	W	0x00000000	Timer2 Load Count Register
TIMER2_LOAD_COUNT1	0x0044	W	0x00000000	Timer2 Load Count Register
TIMER2_CURRENT_VALUE0	0x0048	W	0x00000000	Timer2 Current Value Register
TIMER2_CURRENT_VALUE1	0x004c	W	0x00000000	Timer2 Current Value Register

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Name	Offset	Size	Reset Value	Description
TIMER2_CONTROLREG	0x0050	W	0x00000000	Timer2 Control Register
TIMER2_INTSTATUS	0x0058	W	0x00000000	Timer2 Interrupt Status Register
TIMER3_LOAD_COUNT0	0x0060	W	0x00000000	Timer3 Load Count Register
TIMER3_LOAD_COUNT1	0x0064	W	0x00000000	Timer3 Load Count Register
TIMER3_CURRENT_VALUE0	0x0068	W	0x00000000	Timer3 Current Value Register
TIMER3_CURRENT_VALUE1	0x006c	W	0x00000000	Timer3 Current Value Register
TIMER3_CONTROLREG	0x0070	W	0x00000000	Timer3 Control Register
TIMER3_INTSTATUS	0x0078	W	0x00000000	Timer3 Interrupt Status Register
TIMER4_LOAD_COUNT0	0x0080	W	0x00000000	Timer4 Load Count Register
TIMER4_LOAD_COUNT1	0x0084	W	0x00000000	Timer4 Load Count Register
TIMER4_CURRENT_VALUE0	0x0088	W	0x00000000	Timer4 Current Value Register
TIMER4_CURRENT_VALUE1	0x008c	W	0x00000000	Timer4 Current Value Register
TIMER4_CONTROLREG	0x0090	W	0x00000000	Timer4 Control Register
TIMER4_INTSTATUS	0x0098	W	0x00000000	Timer4 Interrupt Status Register
TIMER5_LOAD_COUNT0	0x00a0	W	0x00000000	Timer5 Load Count Register
TIMER5_LOAD_COUNT1	0x00a4	W	0x00000000	Timer5 Load Count Register
TIMER5_CURRENT_VALUE0	0x00a8	W	0x00000000	Timer5 Current Value Register
TIMER5_CURRENT_VALUE1	0x00ac	W	0x00000000	Timer5 Current Value Register
TIMER5_CONTROLREG	0x00b0	W	0x00000000	Timer5 Control Register
TIMER5_INTSTATUS	0x00b8	W	0x00000000	Timer5 Interrupt Status Register

Timer6-7
Base: 0xff81_0000

Name	Offset	Size	Reset Value	Description
TIMER6_LOAD_COUNT0	0x0000	W	0x00000000	Timer6 Load Count Register
TIMER6_LOAD_COUNT1	0x0004	W	0x00000000	Timer6 Load Count Register
TIMER6_CURRENT_VALUE0	0x0008	W	0x00000000	Timer6 Current Value Register
TIMER6_CURRENT_VALUE1	0x000C	W	0x00000000	Timer6 Current Value Register
TIMER6_CONTROLREG	0x0010	W	0x00000000	Timer6 Control Register
TIMER6_INTSTATUS	0x0018	W	0x00000000	Timer6 Interrupt Status Register
TIMER7_LOAD_COUNT0	0x0020	W	0x00000000	Timer7 Load Count Register
TIMER7_LOAD_COUNT1	0x0024	W	0x00000000	Timer7 Load Count Register
TIMER7_CURRENT_VALUE0	0x0028	W	0x00000000	Timer7 Current Value Register
TIMER7_CURRENT_VALUE1	0x002c	W	0x00000000	Timer7 Current Value Register
TIMER7_CONTROLREG	0x0030	W	0x00000000	Timer7 Control Register
TIMER7_INTSTATUS	0x0038	W	0x00000000	Timer7 Interrupt Status Register

*Notes: Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access*

12.4.2 Detail Register Description

TIMERn_LOAD_COUNT0
Address: Operational Base + offset(0x00+n*0x20)
Timer n Load Count Register (0≤n≤5)

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:0	RW	0x0	Low 32 bits Value to be loaded into Timer n. This is the value from which counting commences.

TIMERn_LOAD_COUNT1
Address: Operational Base + offset(0x04+n*0x20)
Timer n Load Count Register (0≤n≤5)

Bit	Attr	Reset Value	Description
31:0	RW	0x0	High 32 bits Value to be loaded into Timer n. This is the value from which counting commences.

TIMERn_CURRENT_VALUE0
Address: Operational Base + offset(0x08+n*0x20)
Timer n Current Value Register (0≤n≤5)

Bit	Attr	Reset Value	Description
31:0	R	0x0	Low 32 bits of Current Value of Timer n.

TIMERn_CURRENT_VALUE1
Address: Operational Base + offset(0x0c+n*0x20)
Timer n Current Value Register (0≤n≤5)

Bit	Attr	Reset Value	Description
31:0	R	0x0	High 32 bits of Current Value of Timer n.

TIMERn_CONTROLREG
Address: Operational Base + offset(0x10+n*0x20)
Timer n Control Register (0≤n≤5)

Bit	Attr	Reset Value	Description
31:3	-	-	Reserved
2	RW	0x0	Timer interrupt mask. 1'b0: mask 1'b1: not mask
1	RW	0x0	Timer mode. 1'b0: free-running mode 1'b1: user-defined count mode
0	RW	0x0	Timer enable. 1'b0: disable 1'b1: enable

TIMERn_INTSTATUS
Address: Operational Base + offset(0x18+n*0x20)
Timer n Interrupt Status Register (0≤n≤5)

Bit	Attr	Reset Value	Description
31:1	-	-	Reserved
0	RW	0x0	This register contains the interrupt status for timer n Write 1 to this register will clear the interrupt

*Notes: Attr: **RW** – Read/writable, **R** – read only, **W** – write only*

12.5 Application Notes

In the chip, the timer_clk is from 24MHz OSC, asynchronous to the pclk. When user disable the timer enable bit (bit 0 of TIMERn_CONTROLREG (0≤n≤5)), the timer_en output signal is de-asserted, and timer_clk will stop. When user enable the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-config registers when timer_en is low.

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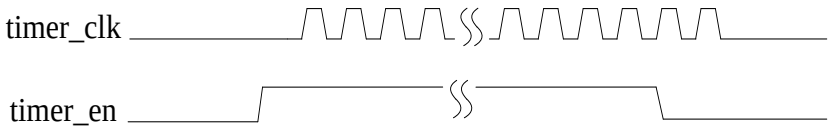

Fig. 12-3 Timing between timer_en and timer_clk

Please refer to funciton description section for the timer usage flow.

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Chapter 13 Generic Interrupt Controller (GIC)

13.1 Overview

The generic interrupt controller (GIC400) in this device has two interfaces, the distributor interface connects to the interrupt source, and the CPU interface connects to Cortex-A17.

It supports the following features:

Supports 160 hardware interrupt inputs
Masking of any interrupts
Prioritization of interrupts
Distribution of the interrupts to the target Cortex-A17 processor(s)
Generation of interrupts by software
Supports Security Extensions

13.2 Block Diagram

The generic interrupt controller comprises with:

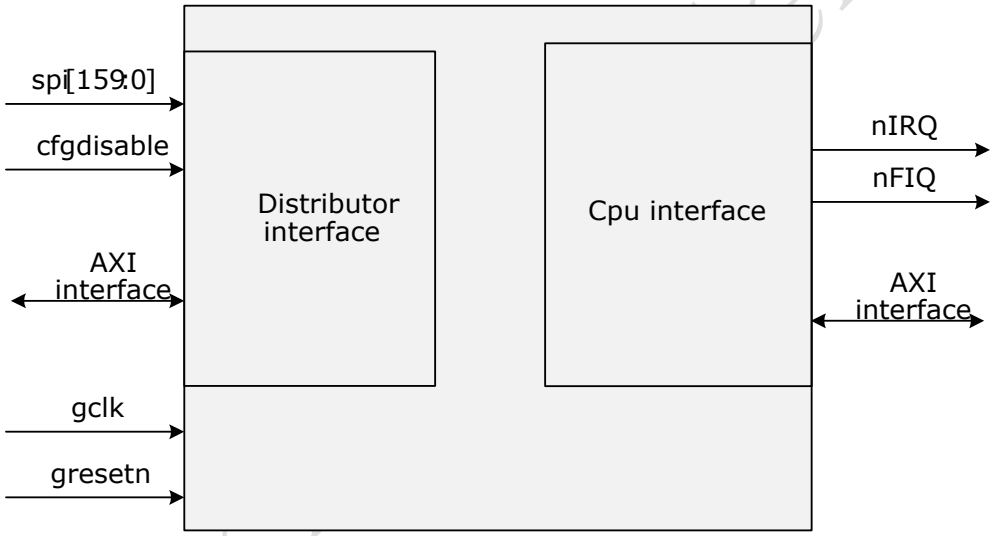

Fig. 13-1 Block Diagram

13.3 Function Description

Please refer to the document IHI0048B_gic_architecture_specification.pdf for the cpu detail description.

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Chapter 14 DMA Controller for Bus System (DMAC_BUS)

14.1 Overview

This device supports 2 Direct Memory Access (DMA) tops, one for cpu system (DMAC_BUS), and the other one for Peripheral system (PERI_DMAC).Both of these two dma support transfers between memory and memory, peripheral and memory.

DMAC_BUS supports TrustZone technology and is under secure state after reset. The secure state can be changed by configuring TZPC module.

DMAC_BUS is mainly used for data transfer of the following slaves: I2S0/I2S1/ SPDIF/UART0/Embedded SRAM and transfer data from/to external DDR SDRAM.

Following table shows the DMAC_BUS peripheral request mapping scheme.

Table 14-1 DMAC_BUS Request Mapping Table

Req number	Source	Polarity
0	I2S tx	High level
1	I2S rx	High level
2	SPDIF	High level
3	SPDIF (8ch)	High level
4	UART DBG tx	High level
5	UART DBG rx	High level

DMAC_BUS supports the following features:

- Supports Trustzone technology
- Supports 6 peripheral request
- Up to 64bits data size
- 5 channel at the same time
- Up to burst 16
- 10 interrupt output and 1 abort output
- Supports 32 MFIFO depth

14.2 Block Diagram

Figure 14-1 shows the block diagram of DMAC_BUS

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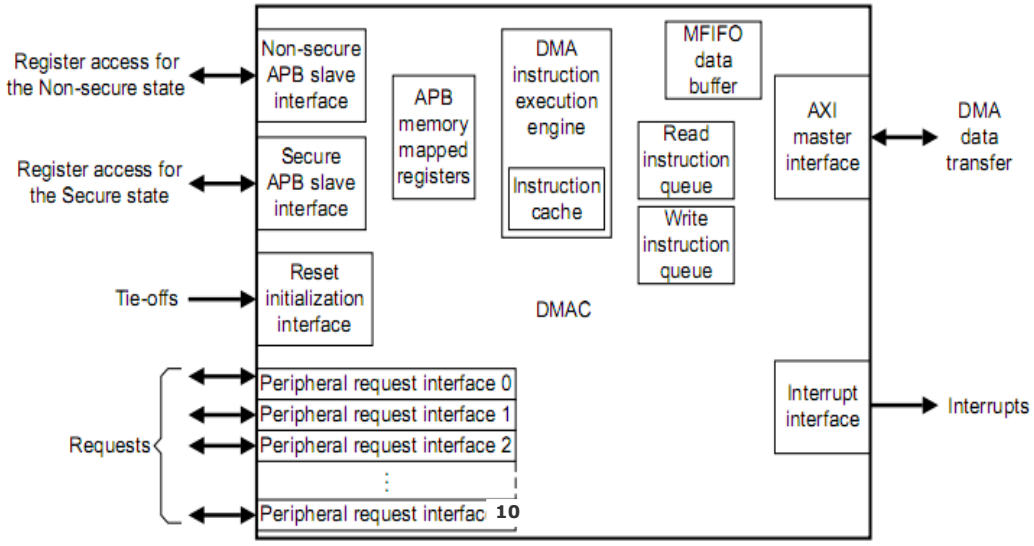

Fig. 14-1 Block diagram of DMAC_BUS

As the DMAC_BUS supports Trustzone technology, so dual APB interfaces enable the operation of the DMAC_BUS to be partitioned into the secure state and Non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC_BUS.The default interface after reset is secure apb interface.

14.3 Function Description

14.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache.

DMAC_BUS supports 6 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin process when selecting the next active DMA channel thread to execute.

The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.

When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete.

When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

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14.3.2 Operating states

Figure shows the operating states for the DMA manager thread and DMA channel threads.

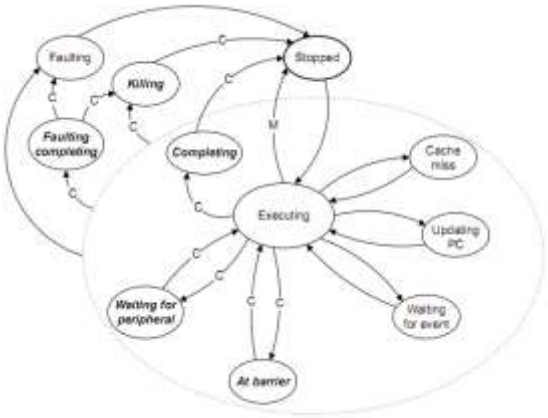

Fig. 14-2 DMAC_BUS operation states

Note:
arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and the status of boot_from_pc(tie-off interface of dmac) controls the DMA manager thread state:

boot_from_pc is LOW :DMA manager thread moves to the Stopped state.
boot_from_pc is HIGH :DMA manager thread moves to the Executing state.

14.4 Register Description

14.4.1 Register summary

Name	Offset	Size	Reset Value	Description
DMAC_BUS_DSR	0x0000	W	0x0	DMA Status Register.
DMAC_BUS_DPC	0x0004	W	0x0	DMA Program Counter Register.
-	-	-	-	reserved
DMAC_BUS_INTEN	0x0020	W	0x0	Interrupt Enable Register
DMAC_BUS_EVENT_RIS	0x0024	W	0x0	Event Status Register.
DMAC_BUS_INTMIS	0x0028	W	0x0	Interrupt Status Register
DMAC_BUS_INTCLR	0x002C	W	0x0	Interrupt Clear Register
DMAC_BUS_FSRD	0x0030	W	0x0	Fault Status DMA Manager Register.
DMAC_BUS_FSRC	0x0034	W	0x0	Fault Status DMA Channel Register.
DMAC_BUS_FTRD	0x0038	W	0x0	Fault Type DMA Manager Register.
-	-	-	-	reserved
DMAC_BUS_FTR0	0x0040	W	0x0	Fault type for DMA Channel 0
DMAC_BUS_FTR1	0x0044	W	0x0	Fault type for DMA Channel 1
DMAC_BUS_FTR2	0x0048	W	0x0	Fault type for DMA Channel 2
DMAC_BUS_FTR3	0x004C	W	0x0	Fault type for DMA Channel 3
DMAC_BUS_FTR4	0x0050	W	0x0	Fault type for DMA Channel 4
DMAC_BUS_FTR5	0x0054	W	0x0	Fault type for DMA Channel 5
-	-	-	-	reserved
DMAC_BUS_CSR0	0x0100	W	0x0	Channel Status for DMA Channel 0

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Name	Offset	Size	Reset Value	Description
DMAC_BUS_CSR1	0x0108	W	0x0	Channel Status for DMA Channel 1
DMAC_BUS_CSR2	0x0110	W	0x0	Channel Status for DMA Channel 2
DMAC_BUS_CSR3	0x0118	W	0x0	Channel Status for DMA Channel 3
DMAC_BUS_CSR4	0x0120	W	0x0	Channel Status for DMA Channel 4
DMAC_BUS_CSR5	0x0128	W	0x0	Channel Status for DMA Channel 5
DMAC_BUS_CPC0	0x0104	W	0x0	Channel PC for DMA Channel 0
DMAC_BUS_CPC1	0x010c	W	0x0	Channel PC for DMA Channel 1
DMAC_BUS_CPC2	0x0114	W	0x0	Channel PC for DMA Channel 2
DMAC_BUS_CPC3	0x011c	W	0x0	Channel PC for DMA Channel 3
DMAC_BUS_CPC4	0x0124	W	0x0	Channel PC for DMA Channel 4
DMAC_BUS_CPC5	0x012c	W	0x0	Channel PC for DMA Channel 5
DMAC_BUS_SAR0	0x0400	W	0x0	Source Address for DMA Channel 0
DMAC_BUS_SAR1	0x0420	W	0x0	Source Address for DMA Channel 1
DMAC_BUS_SAR2	0x0440	W	0x0	Source Address for DMA Channel 2
DMAC_BUS_SAR3	0x0460	W	0x0	Source Address for DMA Channel 3
DMAC_BUS_SAR4	0x0480	W	0x0	Source Address for DMA Channel 4
DMAC_BUS_SAR5	0x04a0	W	0x0	Source Address for DMA Channel 5
DMAC_BUS_DAR0	0x0404	W	0x0	Dest Address for DMAChannel 0
DMAC_BUS_DAR1	0x0424	W	0x0	Dest Address for DMAChannel 1
DMAC_BUS_DAR2	0x0444	W	0x0	Dest Address for DMAChannel 2
DMAC_BUS_DAR3	0x0464	W	0x0	Dest Address for DMAChannel 3
DMAC_BUS_DAR4	0x0484	W	0x0	Dest Address for DMAChannel 4
DMAC_BUS_DAR5	0x04a4	W	0x0	Dest Address for DMAChannel 5
DMAC_BUS_CCR0	0x0408	W	0x0	Channel Control for DMA Channel 0
DMAC_BUS_CCR1	0x0428	W	0x0	Channel Control for DMA Channel 1
DMAC_BUS_CCR2	0x0448	W	0x0	Channel Control for DMA Channel 2
DMAC_BUS_CCR3	0x0468	W	0x0	Channel Control for DMA Channel 3
DMAC_BUS_CCR4	0x0488	W	0x0	Channel Control for DMA Channel 4
DMAC_BUS_CCR5	0x04a8	W	0x0	Channel Control for DMA Channel 5
DMAC_BUS_LC0_0	0x040C	W	0x0	Loop Counter 0 for DMA Channel 0
DMAC_BUS_LC0_1	0x042C	W	0x0	Loop Counter 0 for DMA Channel 1
DMAC_BUS_LC0_2	0x044C	W	0x0	Loop Counter 0 for DMA Channel 2
DMAC_BUS_LC0_3	0x046C	W	0x0	Loop Counter 0 for DMA Channel 3
DMAC_BUS_LC0_4	0x048C	W	0x0	Loop Counter 0 for DMA Channel 4
DMAC_BUS_LC0_5	0x04aC	W	0x0	Loop Counter 0 for DMA Channel 5
DMAC_BUS_LC1_0	0x0410	W	0x0	Loop Counter 1 for DMA Channel 0
DMAC_BUS_LC1_1	0x0430	W	0x0	Loop Counter 1 for DMA Channel 1
DMAC_BUS_LC1_2	0x0450	W	0x0	Loop Counter 1 for DMA Channel 2
DMAC_BUS_LC1_3	0x0470	W	0x0	Loop Counter 1 for DMA Channel 3
DMAC_BUS_LC1_4	0x0490	W	0x0	Loop Counter 1 for DMA Channel 4
DMAC_BUS_LC1_5	0x04b0	W	0x0	Loop Counter 1 for DMA Channel 5
-	-	-	-	reserved
DMAC_BUS_DBGST DMAC_BUS_ATUS	0x0D00	W	0x0	Debug Status Register.
DMAC_BUS_DBGCMD	0x0D04	W	0x0	Debug Command Register.
DMAC_BUS_DBGINST0	0x0D08	W	0x0	Debug Instruction-0 Register.
DMAC_BUS_DBGINST1	0x0D0C	W	0x0	Debug Instruction-1 Register.
DMAC_BUS_CR0	0x0E00	W		Configuration Register 0.
DMAC_BUS_CR1	0x0E04	W		Configuration Register 1.
DMAC_BUS_CR2	0x0E08	W		Configuration Register 2.
DMAC_BUS_CR3	0x0E0C	W		Configuration Register 3.
DMAC_BUS_CR4	0x0E10	W		Configuration Register 4.
DMAC_BUS_CRDn	0x0E14	W		Configuration Register Dn.

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Name	Offset	Size	Reset Value	Description
DMAC_BUS_WD	0x0E80	W	0x0	Watchdog Register.

Notes:
*Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access*

14.4.2 Detail Register Description

DMAC_BUS_DSR
Address:Operational Base+0x0
DMA Manager Status Register

Bit	Attr	Reset Value	Description
31:10	-	-	Reserved
9	R	0x0	Provides the security status of the DMA manager thread: 0 = DMA manager operates in the Secure state 1 = DMA manager operates in the Non-secure state.
8:4	R	0x0	When the DMA manager thread executes a DMAWFE instruction, it waits for the following event to occur: b00000 = event[0] b00001 = event[1] b00010 = event[2] … b11111 = event[31].
3:0	R	0x0	The operating state of the DMA manager: b0000 = Stopped b0001 = Executing b0010 = Cache miss b0011 = Updating PC b0100 = Waiting for event b0101-b1110 = reserved b1111 = Faulting.

DMAC_BUS_DPC
Address:Operational Base+0x4
DMA Program Counter Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Program counter for the DMA manager thread

DMAC_BUS_INTEN
Address:Operational Base+0x20
Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:0	RW	0x0	Program the appropriate bit to control how the DMAC responds when it executes DMASEV: Bit [N] = 0 If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request. Bit [N] = 1 If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interrupt request.

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DMAC_BUS_EVENT_RIS
Address:Operational Base+0x24
Event-Interrupt Raw Status Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Returns the status of the event-interrupt resources: Bit [N] = 0 Event N is inactive or irq[N] is LOW. Bit [N] = 1 Event N is active or irq[N] is HIGH.

DMAC_BUS_INTMIS
Address:Operational Base+0x28
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the status of the interrupts that are active in the DMAC: Bit [N] = 0 Interrupt N is inactive and therefore irq[N] is LOW. Bit [N] = 1 Interrupt N is active and therefore irq[N] is HIGH

DMAC_BUS_INTCLR
Address:Operational Base+0x2c
Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:0	W	0x0	Controls the clearing of the irq outputs: Bit [N] = 0 The status of irq[N] does not change. Bit [N] = 1 The DMAC sets irq[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change.

DMAC_BUS_FSRD
Address:Operational Base+0x30
Fault Status DMA Manager Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the fault status of the DMA manager. Read as: 0 = the DMA manager thread is not in the Faulting state 1 = the DMA manager thread is in the Faulting state.

DMAC_BUS_FSRC
Address:Operational Base+0x34
Fault Status DMA Channel Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Each bit provides the fault status of the corresponding channel. Read as: Bit [N] = 0 No fault is present on DMA channel N. Bit [N] = 1 DMA channel N is in the Faulting or Faulting completing state.

DMAC_BUS_FTRD
Address:Operational Base+0x38
Fault Type DMA Manager Register

Bit	Attr	Reset Value	Description
31	-	-	reserved
30	R	0x0	If the DMA manager aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface: 0 = instruction that generated an abort was read from

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Bit	Attr	Reset Value	Description
			system memory 1 = instruction that generated an abort was read from the debug interface.
29:17	-	-	reserved
16	R	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA manager performs an instruction fetch: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response
15:6	-	-	reserved
5	R	0x0	Indicates if the DMA manager was attempting to execute DMAWFE or DMASEV with inappropriate security permissions: 0 = DMA manager has appropriate security to execute DMAWFE or DMASEV 1 = a DMA manager thread in the Non-secure state attempted to execute either: • DMAWFE to wait for a secure event • DMASEV to create a secure event or secure interrupt
4	R	0x0	ndicates if the DMA manager was attempting to execute DMAGO with inappropriate security permissions: 0 = DMA manager has appropriate security to execute DMAGO 1 = a DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state.
3:2	-	-	reserved
1	R	0x0	Indicates if the DMA manager was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 0 = valid operand 1 = invalid operand.
0	R	0x0	Indicates if the DMA manager was attempting to execute an undefined instruction: 0 = defined instruction 1 = undefined instruction.

DMAC_BUS_FTR0~DMAC_BUS_FTR5

Address:Operational Base+0x40
Operational Base+0x44
Operational Base+0x48
Operational Base+0x4c
Operational Base+0x50
Operational Base+0x54

Fault Type DMA Channel Register

Bit	Attr	Reset Value	Description
31	R	0x0	Indicates if the DMA channel has locked-up because of resource starvation: 0 = DMA channel has adequate resources 1 = DMA channel has locked-up because of insufficient resources. This fault is an imprecise abort
30	R	0x0	If the DMA channel aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface:

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Bit	Attr	Reset Value	Description
			0 = instruction that generated an abort was read from system memory 1 = instruction that generated an abort was read from the debug interface. This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	-	-	reserved
18	R	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs a data read: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is an imprecise abort
17	R	0x0	Indicates the AXI response that the DMAC receives on the BRESP bus, after the DMA channel thread performs a data write: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is an imprecise abort.
16	R	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs an instruction fetch: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is a precise abort.
15:14	-	-	reserved
13	R	0x0	Indicates if the MFIFO did not contain the data to enable the DMAC to perform the DMAST: 0 = MFIFO contains all the data to enable the DMAST to complete 1 = previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete. This fault is a precise abort.
12	R	0x0	Indicates if the MFIFO prevented the DMA channel thread from executing DMALD or DMAST. Depending on the instruction: DMALD 0 = MFIFO contains sufficient space 1 = MFIFO is too small to hold the data that DMALD requires. DMAST 0 = MFIFO contains sufficient data 1 = MFIFO is too small to store the data to enable DMAST to complete. This fault is an imprecise abort
11:8	-	-	reserved
7	R	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to program the CCRn Register to perform a secure read or secure write: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write. This fault is a precise abort
6	R	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to execute DMAWFP, DMALDP, DMASTP, or DMAFLUSHP with inappropriate security permissions: 0 = a DMA channel thread in the Non-secure state is not

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Bit	Attr	Reset Value	Description
			violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to execute either: • DMAWFP to wait for a secure peripheral • DMALDP or DMASTP to notify a secure peripheral • DMAFLUSHP to flush a secure peripheral. This fault is a precise abort.
5	R	0x0	Indicates if the DMA channel thread attempts to execute DMAWFE or DMASEV with inappropriate security permissions: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to execute either: • DMAWFE to wait for a secure event • DMASEV to create a secure event or secure interrupt. This fault is a precise abort.
4:2	-	-	reserved
1	R	0x0	Indicates if the DMA channel thread was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 0 = valid operand 1 = invalid operand. This fault is a precise abort.
0	R	0x0	Indicates if the DMA channel thread was attempting to execute an undefined instruction: 0 = defined instruction 1 = undefined instruction. This fault is a precise abort

DMAC_BUS_CSR0~DMAC_BUS_CSR5

Address:Operational Base+0x100
Operational Base+0x108
Operational Base+0x110
Operational Base+0x118
Operational Base+0x120
Operational Base+0x128

Channel Status Registers

Bit	Attr	Reset Value	Description
31:22	-	-	reserved
21	R	0x0	The channel non-secure bit provides the security of the DMA channel: 0 = DMA channel operates in the Secure state 1 = DMA channel operates in the Non-secure state
20:16	-	-	reserved
15	R	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the periph operand was set: 0 = DMAWFP executed with the periph operand not set 1 = DMAWFP executed with the periph operand set
14	R	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the burst or single operand were set: 0 = DMAWFP executed with the single operand set 1 = DMAWFP executed with the burst operand set.
13:9	-	-	reserved

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Bit	Attr	Reset Value	Description
8:4	R	0x0	If the DMA channel is in the Waiting for event state or the Waiting for peripheral state then these bits indicate the event or peripheral number that the channel is waiting for: b00000 = DMA channel is waiting for event, or peripheral, 0 b00001 = DMA channel is waiting for event, or peripheral, 1 b00010 = DMA channel is waiting for event, or peripheral, 2... b11111 = DMA channel is waiting for event, or peripheral, 31
3:0	R	0x0	The channel status encoding is: b0000 = Stopped b0001 = Executing b0010 = Cache miss b0011 = Updating PC b0100 = Waiting for event b0101 = At barrier b0110 = reserved b0111 = Waiting for peripheral b1000 = Killing b1001 = Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMAC_BUS_CPC0~DMAC_BUS_CPC5

Address:Operational Base+0x104
Operational Base+0x10c
Operational Base+0x114
Operational Base+0x11c
Operational Base+0x124
Operational Base+0x12c

Channel Program Counter Registers

Bit	Attr	Reset Value	Description
31:0	R	0x0	Program counter for the DMA channel n thread

DMAC_BUS_SAR0~DMAC_BUS_SAR5

Address:Operational Base+0x400
Operational Base+0x420
Operational Base+0x440
Operational Base+0x460
Operational Base+0x480
Operational Base+0x4a0

Source Address Registers

Bit	Attr	Reset Value	Description
31:0	R	0x0	Address of the source data for DMA channel n

DMAC_BUS_DAR0~DMAC_BUS_DAR5

Address:Operational Base+0x404
Operational Base+0x424
Operational Base+0x444
Operational Base+0x464
Operational Base+0x484
Operational Base+0x4a4

DestinationAddress Registers

Bit	Attr	Reset Value	Description
31:0	R	0x0	Address of the Destinationdata for DMA channel n

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DMAC_BUS_CCR0~DMAC_BUS_CCR5

Address:Operational Base+0x408
Operational Base+0x428
Operational Base+0x448
Operational Base+0x468
Operational Base+0x488
Operational Base+0x4a8

Channel Control Registers

Bit	Attr	Reset Value	Description
31:28	-	-	reserved
27:25	R	0x0	Programs the state of AWCACHE[3,1:0]a when the DMAC writes the destination data. Bit [27] 0 = AWCACHE[3] is LOW 1 = AWCACHE[3] is HIGH. Bit [26] 0 = AWCACHE[1] is LOW 1 = AWCACHE[1] is HIGH. Bit [25] 0 = AWCACHE[0] is LOW 1 = AWCACHE[0] is HIGH
24:22	R	0x0	Programs the state of AWPROT[2:0]a when the DMAC writes the destination data. Bit [24] 0 = AWPROT[2] is LOW 1 = AWPROT[2] is HIGH. Bit [23] 0 = AWPROT[1] is LOW 1 = AWPROT[1] is HIGH. Bit [22] 0 = AWPROT[0] is LOW 1 = AWPROT[0] is HIGH
21:18	R	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it writes the destination data: b0000 = 1 data transfer b0001 = 2 data transfers b0010 = 3 data transfers ... b1111 = 16 data transfers. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size
17:15	R	0x0	For each beat within a burst, it programs the number of bytes that the DMAC writes to the destination: b000 = writes 1 byte per beat b001 = writes 2 bytes per beat b010 = writes 4 bytes per beat b011 = writes 8 bytes per beat b100 = writes 16 bytes per beat b101-b111 = reserved. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	R	0x0	Programs the burst type that the DMAC performs when it writes the destination data: 0 = Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1 = Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	R	0x0	Set the bits to control the state of ARCACHE[2:0]a when the DMAC reads the source data.

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Bit	Attr	Reset Value	Description
			Bit [13] 0 = ARCACHE[2] is LOW 1 = ARCACHE[2] is HIGH. Bit [12] 0 = ARCACHE[1] is LOW 1 = ARCACHE[1] is HIGH. Bit [11] 0 = ARCACHE[0] is LOW 1 = ARCACHE[0] is HIGH.
10:8	R	0x0	Programs the state of ARPROT[2:0]a when the DMAC reads the source data. Bit [10] 0 = ARPROT[2] is LOW 1 = ARPROT[2] is HIGH. Bit [9] 0 = ARPROT[1] is LOW 1 = ARPROT[1] is HIGH. Bit [8] 0 = ARPROT[0] is LOW 1 = ARPROT[0] is HIGH.
7:4	R	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it reads the source data: b0000 = 1 data transfer b0001 = 2 data transfers b0010 = 3 data transfers ... b1111 = 16 data transfers. The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size
3:1	R	0x0	For each beat within a burst, it programs the number of bytes that the DMAC reads from the source: b000 = reads 1 byte per beat b001 = reads 2 bytes per beat b010 = reads 4 bytes per beat b011 = reads 8 bytes per beat b100 = reads 16 bytes per beat b101-b111 = reserved. The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size
0	R	0x0	Programs the burst type that the DMAC performs when it reads the source data: 0 = Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1 = Incrementing-address burst. The DMAC signals ARBURST[0] HIGH

DMAC_BUS_LC0_0~DMAC_BUS_LC0_5

Address:Operational Base+0x40c
Operational Base+0x42c
Operational Base+0x44c
Operational Base+0x46c
Operational Base+0x48c
Operational Base+0x4ac

Loop Counter 0 Registers

Bit	Attr	Reset Value	Description
31:8	-	-	reserved
7:0	R	0x0	Loop counter 0 iterations

DMAC_BUS_LC1_0~DMAC_BUS_LC1_5

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Address:Operational Base+0x410
Operational Base+0x430
Operational Base+0x450
Operational Base+0x470
Operational Base+0x490
Operational Base+0x4b0
Loop Counter 1 Registers

Bit	Attr	Reset Value	Description
31:8	-	-	reserved
7:0	R	0x0	Loop counter 1 iterations

DMAC_BUS_DBGSTATUS
Address:Operational Base+0xd00
Debug Status Register

Bit	Attr	Reset Value	Description
31:2	-	-	reserved
1:0	R	0x0	The debug encoding is as follows: b00 = execute the instruction that the DBGINST [1:0] Registers contain b01 = reserved b10 = reserved b11 = reserved.

DMAC_BUS_DBGCMD
Address:Operational Base+0xd04
Debug Command Register

Bit	Attr	Reset Value	Description
31:2	-	-	reserved
1:0	W	0x0	The debug encoding is as follows: b00 = execute the instruction that the DBGINST [1:0] Registers contain b01 = reserved b10 = reserved b11 = reserved

DMAC_BUS_DBGINST0
Address:Operational Base+0xd08
Debug Instruction-0 Register

Bit	Attr	Reset Value	Description
31:24	W	0x0	Instruction byte 1
23:16	W	0x0	Instruction byte 0
15:11	-	-	reserved
10:8	W	0x0	DMA channel number: b000 = DMA channel 0 b001 = DMA channel 1 b010 = DMA channel 2 … b111 = DMA channel 7
7:1	-	-	reserved
0	W	0x0	The debug thread encoding is as follows: 0 = DMA manager thread 1 = DMA channel.

DMAC_BUS_DBGINST1
Address:Operational Base+0xd0c
Debug Instruction-1 Register

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Bit	Attr	Reset Value	Description
31:24	W	0x0	Instruction byte 5
23:16	W	0x0	Instruction byte 4
15:8	W	0x0	Instruction byte 3
7:0	W	0x0	Instruction byte 2

DMAC_BUS_CR0
Address:Operational Base+0xe00
Configuration Register 0

Bit	Attr	Reset Value	Description
31:22	-	-	reserved
21:17	R	0x2	Number of interrupt outputs that the DMAC provides: b00000 = 1 interrupt output, irq[0] b00001 = 2 interrupt outputs, irq[1:0] b00010 = 3 interrupt outputs, irq[2:0] ... b11111 = 32 interrupt outputs, irq[31:0].
16:12	R	0x7	Number of peripheral request interfaces that the DMAC provides: b00000 = 1 peripheral request interface b00001 = 2 peripheral request interfaces b00010 = 3 peripheral request interfaces ... b11111 = 32 peripheral request interfaces.
11:7	-	-	reserved
6:4	R	0x5	Number of DMA channels that the DMAC supports: b000 = 1 DMA channel b001 = 2 DMA channels b010 = 3 DMA channels ... b111 = 8 DMA channels.
3	-	-	reserved
2	R	0x0	Indicates the status of the boot_manager_ns signal when the DMAC exited from reset: 0 = boot_manager_ns was LOW 1 = boot_manager_ns was HIGH.
1	R	0x0	Indicates the status of the boot_from_pc signal when the DMAC exited from reset: 0 = boot_from_pc was LOW 1 = boot_from_pc was HIGH
0	R	0x1	Supports peripheral requests: 0 = the DMAC does not provide a peripheral request interface 1 = the DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies.

DMAC_BUS_CR1
Address:Operational Base+0xe04
Configuration Register 1

Bit	Attr	Reset Value	Description
31:8	-	-	reserved
7:4	R	0x5	[7:4] num_i-cache_lines Number of i-cache lines: b0000 = 1 i-cache line b0001 = 2 i-cache lines b0010 = 3 i-cache lines …

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Bit	Attr	Reset Value	Description
			b1111 = 16 i-cache lines.
3	-	-	reserved
2:0	R	0x7	The length of an i-cache line: b000-b001 = reserved b010 = 4 bytes b011 = 8 bytes b100 = 16 bytes b101 = 32 bytes b110-b111 = reserved

DMAC_BUS_CR2
Address:Operational Base+0xe08
Configuration Register 2

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMAC_BUS_CR3
Address:Operational Base+0xe0c
Configuration Register 3

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the security state of an event-interrupt resource: Bit [N] = 0 Assigns event<N> or irq[N] to the Secure state. Bit [N] = 1 Assigns event<N> or irq[N] to the Non-secure state.

DMAC_BUS_CR4
Address:Operational Base+0xe10
Configuration Register 4

Bit	Attr	Reset Value	Description
31:0	R	0x6	Provides the security state of the peripheral request interfaces: Bit [N] = 0 Assigns peripheral request interface N to the Secure state. Bit [N] = 1 Assigns peripheral request interface N to the Non-secure state

DMAC_BUS_CRDn
Address:Operational Base+0xe14
DMA Configuration Register

Bit	Attr	Reset Value	Description
31:30	-	-	reserved
29:20	R	0x20	The number of lines that the data buffer contains: b000000000 = 1 line b000000001 = 2 lines … b111111111 = 1024 lines
19:16	R	0x9	The depth of the read queue: b0000 = 1 line b0001 = 2 lines ... b1111 = 16 lines.
15	-	-	reserved

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Bit	Attr	Reset Value	Description
14:12	R	0x4	Read issuing capability that programs the number of outstanding read transactions: b000 = 1 b001 = 2 … b111 = 8
11:8	R	0x7	The depth of the write queue: b0000 = 1 line b0001 = 2 lines … b1111 = 16 lines.
7	-	-	reserved
6:4	R	0x3	Write issuing capability that programs the number of outstanding write transactions: b000 = 1 b001 = 2 … b111 = 8
3	-	-	reserved
2:0		0x3	The data bus width of the AXI interface: b000 = reserved b001 = reserved b010 = 32-bit b011 = 64-bit b100 = 128-bit b101-b111 = reserved.

DMAC_BUS_WD
Address:Operational Base+0xe80
DMA Watchdog Register

Bit	Attr	Reset Value	Description
-	-	-	reserved
0	RW	0x0	Controls how the DMAC responds when it detects a lock-up condition: 0 = the DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1 = the DMAC sets irq_abort HIGH.

14.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

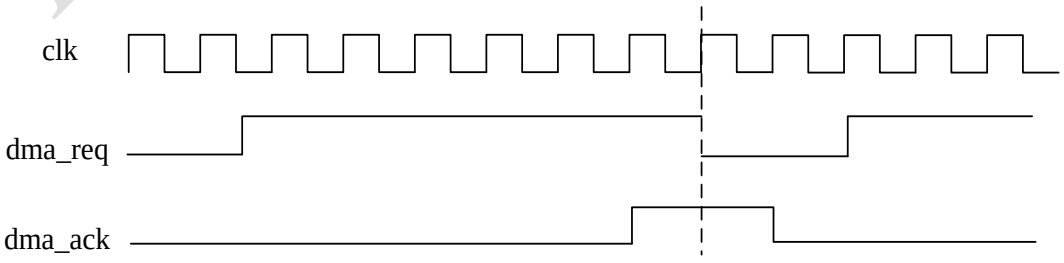

Fig. 14-3 DMAC_BUS request and acknowledge timing

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14.6 Interface Description

DMAC_BUS has the following tie-off signals. It can be configured by GRF register or TZPC register. (Please refer to these two chapters to find how to configure)

interface	Reset value	Control source
boot_addr	0x0	Secure GRF
boot_from_pc	0x0	Secure GRF
boot_manager_ns	0x0	Secure GRF / TZPC
boot_irq_ns	0x0	Secure GRF / TZPC
boot_periph_ns	0x0	TZPC

boot_addr
Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
boot_from_pc
Controls the location in which the DMAC executes its initial instruction, after it exits from reset:
0 = DMAC waits for an instruction from either APB interface
1 = DMA manager thread executes the instruction that is located at the address that
boot_manager_ns
When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
0 = assigns DMA manager to the Secure state
1 = assigns DMA manager to the Non-secure state.
boot_irq_ns
Controls the security state of an event-interrupt resource, when the DMAC exits from reset:
boot_irq_ns[x] is LOW
The DMAC assigns event<x> or irq[x] to the Secure state.
boot_irq_ns[x] is HIGH
The DMAC assigns event<x> or irq[x] to the Non-secure state.
boot_periph_ns
Controls the security state of a peripheral request interface, when the DMAC exits from reset:
boot_periph_ns[x] is LOW
The DMAC assigns peripheral request interface x to the Secure state.
boot_periph_ns[x] is HIGH
The DMAC assigns peripheral request interface x to the Non-secure state.

14.7 Application Notes

14.7.1 Using the APB slave interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the Non-secure state.
The necessary steps to start a DMA channel thread using the debug instruction registers as following:
1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DBGINST0 Register and enter the:
• Instruction byte 0 encoding for DMAGO.

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• Instruction byte 1 encoding for DMAGO.
• Debug thread bit to 0. This selects the DMA manager thread.
5. Write to the DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register o. You must set these four bytes to the address of the first instruction in the program, that was written to system memory in step 2.
6. Writing zero to the DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

14.7.2 Security usage

When the DMAC exits from reset, the status of the configuration signals that tie-off signals which descripted in chapter 10.6.

DMA manager thread is in the secure state

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:

DMAGO

It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

DMAWFE

It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

DMASEV

It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

DMA manager thread is in the Non-secure state

If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:

DMAGO

The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:

ns = 0

The DMAC does not start a DMA channel thread and instead it:

1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

ns = 1

The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3Register, to control if it creates the event-interrupt. If:

INS = 0

The event-interrupt resource is in the Secure state. The DMAC:

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1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state

When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.

When a DMA channel thread in the secure state processes the following instructions:

DMAWFE

The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the CR3 Register.

DMASEV

The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the CR3 Register.

DMAWFP

The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

DMALDP, DMASTP

The DMAC sends a message to the peripheral to communicate that data transfer is complete, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

DMAFLUSHP

The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses

DMA channel thread is in the Non-secure state

When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.

When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it creates the event. If:

INS = 0

The event-interrupt resource is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the FTRn Register, see Fault Type DMA Channel Registers .
4. Moves the DMA channel to the Faulting completing state.

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INS = 1
The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.
DMAWFP
The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it waits for the peripheral to signal a request. If:
PNS = 0
The peripheral is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.
DMALDP, DMASTP
The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it sends an acknowledgement to the peripheral. If:
PNS = 0
The peripheral is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.
DMAFLUSHP
The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Registe.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:

1. Executes a DMANOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Registe.
3. Sets the ch_rdwr_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

14.7.3 Programming restrictions

Fixed unaligned bursts
The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read
• src_inc field is 0 in the CCRn Register
• the SARn Register contains an address that is not aligned to the size of data

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that the src_burst_size field contain
Unaligned write
• dst_inc field is 0 in the CCRn Register
• the DARn Register contains an address that is not aligned to the size of data
that the dst_burst_size field contains

Endian swap size restrictions

If you program the endian_swap_size field in the CCRn Register, to enable a DMA channel to perform an endian swap then you must set the corresponding SARn Register and the corresponding DARn Register to contain an address that is aligned to the value that the endian_swap_size field contains.

Updating DMA channel control registers during a DMA cyclerestrictions

Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the CCRn Register, SARn Register, and DARn Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.

Resource sharing between DMA channels

DMA channel programs share the MFIFO data storage resource. You must not start a set ofconcurrently running DMA channel programs with a resource requirement that exceeds theconfigured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

14.7.4 Unaligned transfers may be corrupted

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.

Data corruption might occur if all of the following are true:

1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is split across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats .
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below)

Splitting data

Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface mneed to be split across two lines in the internal data buffer. This occurs when the read data beat contains datbytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMA-330 do not split data in this way, so are NOT vulnerable to data corruption from thisdefect.

The following cases are NOT vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 When source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size

Source size in CCRn	Allowed offset between SARn and DARn
SS8	any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

14.7.5 Interrupt shares between channel.

As the DMAC_BUS does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that

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program can be used to determine progress, and help identify the interrupt source.

There are 4 likely information sources that can be used to determine the progress made by a program:

- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.

The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:

1. Disable interrupts
2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

14.7.6 Instruction sets

Table 14-2 DMAC Instruction sets

Mnemonic	**Instruction**	**Thread usage:** **● M = DMA manager** **● C = DMA channel**
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C
DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C
DMAMOV	Move	C
DMANOP	No operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wai t For Event M	M/C
DMAWFP	Wait For Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

14.7.7 Assembler directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled. *For the other instructions , please refer to pl330_trm.pdf.*
DMAADNH

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Add Negative Halfword adds an immediate negative 16-bit value to the SARn Register or DA Rn Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operati ons, or reading or writing an area of memory in adifferent order to naturally incrementing ad dresses. See Source Address Registers and Destination Address Registers.
The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is th e two's complement representation of a negative number between -65536 and -1, before th e DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 655 36 and 1 from the current value in the Source or Destination Address Register.
Following table shows the instruction encoding.

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax
DMAADNH <address_register>, <16-bit immediate>
where:
<address_register>
Selects the address register to use. It must be either:
SAR
SARn Register and sets ra to 0.
DAR
DARn Register and sets ra to 1.

<16-bit immediate>
The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instr uction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be a dded to the current value of the Destination Address Register, effectively subtracting 16 fro m the DAR.
You can only use this instruction in a DMA channel thread.

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Chapter 15 DMA Controller for Peripheral System (DMAC_PERI)

15.1 Overview

DMAC_PERI does not support TrustZone technology and work under non-secure state only.

DMAC_PERI is mainly used for data transfer of the following slaves: HSADC, UART BT, UART BB, UART GPS, UART EXP, SPI0, SPI1,SPI2.

Following table shows the DMAC_PERI request mapping scheme.

Table 15-1 DMAC_PERI Request Mapping Table

Req number	Source	Polarity
0	HSADC/TSI	High level
1	UART BT tx	High level
2	UART BT rx	High level
3	UART BB tx	High level
4	UART BB rx	High level
5	Reserved	
6	Reserved	
7	UART GPS tx	High level
8	UART GPS rx	High level
9	UART EXP tx	High level
10	UART EXP rx	High level
11	SPI0 tx	High level
12	SPI0 rx	High level
13	SPI1 tx	High level
14	SPI1 rx	High level
15	SPI2 tx	High level
16	SPI2 rx	High level
17	Reserved	
18	Reserved	
19	Reserved	

DMAC_PERI supports the following features:

- Supports 20 peripheral request.
- Up to 64bits data size.
- 8 channel at the same time.
- Up to burst 16.
- 16 interrupts output and 1 abort output.
- Supports 64 MFIFO depth.

15.2 Block Diagram

Figure 11-1 shows the block diagram of DMAC_PERI.

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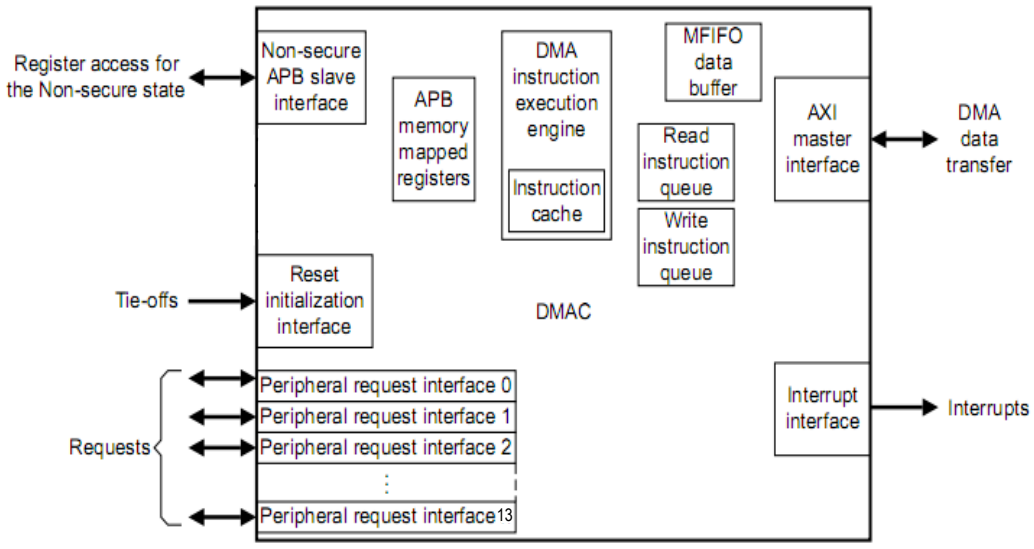

Fig. 15-1 Block diagram of DMAC_PERI

15.3 Function Description

Please refer to chapter 14.3 for the similar description.

15.4 Register Description

15.4.1 Register summary

Name	Offset	Size	Reset Value	Description
DMAC_PERI_DSR	0x0000	W	0x0	DMA Status Register.
DMAC_PERI_DPC	0x0004	W	0x0	DMA Program Counter Register.
-	-	-	-	reserved
DMAC_PERI_INTEN	0x0020	W	0x0	Interrupt Enable Register
DMAC_PERI_EVENT_RIS	0x0024	W	0x0	Event Status Register.
DMAC_PERI_INTMIS	0x0028	W	0x0	Interrupt Status Register
DMAC_PERI_INTCLR	0x002C	W	0x0	Interrupt Clear Register
DMAC_PERI_FSRD	0x0030	W	0x0	Fault Status DMA Manager Register.
DMAC_PERI_FSRC	0x0034	W	0x0	Fault Status DMA Channel Register.
DMAC_PERI_FTRD	0x0038	W	0x0	Fault Type DMA Manager Register.
-	-	-	-	reserved
DMAC_PERI_FTR0	0x0040	W	0x0	Fault type for DMA Channel 0
DMAC_PERI_FTR1	0x0044	W	0x0	Fault type for DMA Channel 1
DMAC_PERI_FTR2	0x0048	W	0x0	Fault type for DMA Channel 2
DMAC_PERI_FTR3	0x004C	W	0x0	Fault type for DMA Channel 3
DMAC_PERI_FTR4	0x0050	W	0x0	Fault type for DMA Channel 4
DMAC_PERI_FTR5	0x0054	W	0x0	Fault type for DMA Channel 5
DMAC_PERI_FTR6	0x0058	W	0x0	Fault type for DMA Channel 6
-	-	-	-	reserved
DMAC_PERI_CSR0	0x0100	W	0x0	Channel Status for DMA Channel 0
DMAC_PERI_CSR1	0x0108	W	0x0	Channel Status for DMA Channel 1
DMAC_PERI_CSR2	0x0110	W	0x0	Channel Status for DMA Channel 2
DMAC_PERI_CSR3	0x0118	W	0x0	Channel Status for DMA Channel 3
DMAC_PERI_CSR4	0x0120	W	0x0	Channel Status for DMA Channel 4
DMAC_PERI_CSR5	0x0128	W	0x0	Channel Status for DMA Channel 5

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Name	Offset	Size	Reset Value	Description
DMAC_PERI_CSR6	0x0130	W	0x0	Channel Status for DMA Channel 6
DMAC_PERI_CPC0	0x0104	W	0x0	Channel PC for DMA Channel 0
DMAC_PERI_CPC1	0x010c	W	0x0	Channel PC for DMA Channel 1
DMAC_PERI_CPC2	0x0114	W	0x0	Channel PC for DMA Channel 2
DMAC_PERI_CPC3	0x011c	W	0x0	Channel PC for DMA Channel 3
DMAC_PERI_CPC4	0x0124	W	0x0	Channel PC for DMA Channel 4
DMAC_PERI_CPC5	0x012c	W	0x0	Channel PC for DMA Channel 5
DMAC_PERI_CPC6	0x0134	W	0x0	Channel PC for DMA Channel 6
DMAC_PERI_SAR0	0x0400	W	0x0	Source Address for DMA Channel 0
DMAC_PERI_SAR1	0x0420	W	0x0	Source Address for DMA Channel 1
DMAC_PERI_SAR2	0x0440	W	0x0	Source Address for DMA Channel 2
DMAC_PERI_SAR3	0x0460	W	0x0	Source Address for DMA Channel 3
DMAC_PERI_SAR4	0x0480	W	0x0	Source Address for DMA Channel 4
DMAC_PERI_SAR5	0x04a0	W	0x0	Source Address for DMA Channel 5
DMAC_PERI_SAR6	0x04c0	W	0x0	Source Address for DMA Channel 6
DMAC_PERI_DAR0	0x0404	W	0x0	Dest Address for DMAChannel 0
DMAC_PERI_DAR1	0x0424	W	0x0	Dest Address for DMAChannel 1
DMAC_PERI_DAR2	0x0444	W	0x0	Dest Address for DMAChannel 2
DMAC_PERI_DAR3	0x0464	W	0x0	Dest Address for DMAChannel 3
DMAC_PERI_DAR4	0x0484	W	0x0	Dest Address for DMAChannel 4
DMAC_PERI_DAR5	0x04a4	W	0x0	Dest Address for DMAChannel 5
DMAC_PERI_DAR6	0x04c4	W	0x0	Dest Address for DMAChannel 6
DMAC_PERI_CCR0	0x0408	W	0x0	Channel Control for DMA Channel 0
DMAC_PERI_CCR1	0x0428	W	0x0	Channel Control for DMA Channel 1
DMAC_PERI_CCR2	0x0448	W	0x0	Channel Control for DMA Channel 2
DMAC_PERI_CCR3	0x0468	W	0x0	Channel Control for DMA Channel 3
DMAC_PERI_CCR4	0x0488	W	0x0	Channel Control for DMA Channel 4
DMAC_PERI_CCR5	0x04a8	W	0x0	Channel Control for DMA Channel 5
DMAC_PERI_CCR6	0x04c8	W	0x0	Channel Control for DMA Channel 6
DMAC_PERI_LC0_0	0x040C	W	0x0	Loop Counter 0 for DMA Channel 0
DMAC_PERI_LC0_1	0x042C	W	0x0	Loop Counter 0 for DMA Channel 1
DMAC_PERI_LC0_2	0x044C	W	0x0	Loop Counter 0 for DMA Channel 2
DMAC_PERI_LC0_3	0x046C	W	0x0	Loop Counter 0 for DMA Channel 3
DMAC_PERI_LC0_4	0x048C	W	0x0	Loop Counter 0 for DMA Channel 4
DMAC_PERI_LC0_5	0x04aC	W	0x0	Loop Counter 0 for DMA Channel 5
DMAC_PERI_LC0_6	0x04cC	W	0x0	Loop Counter 0 for DMA Channel 6
DMAC_PERI_LC1_0	0x0410	W	0x0	Loop Counter 1 for DMA Channel 0
DMAC_PERI_LC1_1	0x0430	W	0x0	Loop Counter 1 for DMA Channel 1
DMAC_PERI_LC1_2	0x0450	W	0x0	Loop Counter 1 for DMA Channel 2
DMAC_PERI_LC1_3	0x0470	W	0x0	Loop Counter 1 for DMA Channel 3
DMAC_PERI_LC1_4	0x0490	W	0x0	Loop Counter 1 for DMA Channel 4
DMAC_PERI_LC1_5	0x04b0	W	0x0	Loop Counter 1 for DMA Channel 5
DMAC_PERI_LC1_6	0x04d0	W	0x0	Loop Counter 1 for DMA Channel 6
-	-	-	-	reserved
DMAC_PERI_DBGST DMAC_PERI_ATUS	0x0D00	W	0x0	Debug Status Register.
DMAC_PERI_DBGCMD	0x0D04	W	0x0	Debug Command Register.
DMAC_PERI_DBGINST0	0x0D08	W	0x0	Debug Instruction-0 Register.
DMAC_PERI_DBGINST1	0x0D0C	W	0x0	Debug Instruction-1 Register.
DMAC_PERI_CR0	0x0E00	W		Configuration Register 0.
DMAC_PERI_CR1	0x0E04	W		Configuration Register 1.
DMAC_PERI_CR2	0x0E08	W		Configuration Register 2.
DMAC_PERI_CR3	0x0E0C	W		Configuration Register 3.

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Name	Offset	Size	Reset Value	Description
DMAC_PERI_CR4	0x0E10	W		Configuration Register 4.
DMAC_PERI_CRDn	0x0E14	W		Configuration Register Dn.
DMAC_PERI_WD	0X0E80	W		Watchdog Register

Notes:
*Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access*

15.4.2 Detail Register Description

DMAC_PERI_DSR
Address:Operational Base+0x0
DMA Manager Status Register

Bit	Attr	Reset Value	Description
31:10	-	-	Reserved
9	R	0x0	Provides the security status of the DMA manager thread: 0 = DMA manager operates in the Secure state 1 = DMA manager operates in the Non-secure state.
8:4	R	0x0	When the DMA manager thread executes a DMAWFE instruction, it waits for the following event to occur: b00000 = event[0] b00001 = event[1] b00010 = event[2] … b11111 = event[31].
3:0	R	0x0	The operating state of the DMA manager: b0000 = Stopped b0001 = Executing b0010 = Cache miss b0011 = Updating PC b0100 = Waiting for event b0101-b1110 = reserved b1111 = Faulting.

DMAC_PERI_DPC
Address:Operational Base+0x4
DMA Program Counter Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Program counter for the DMA manager thread

DMAC_PERI_INTEN
Address:Operational Base+0x20
Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:0	RW	0x0	Program the appropriate bit to control how the DMAC responds when it executes DMASEV: Bit [N] = 0 If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request. Bit [N] = 1 If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interrupt request.

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DMAC_PERI_EVENT_RIS
Address:Operational Base+0x24
Event-Interrupt Raw Status Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Returns the status of the event-interrupt resources: Bit [N] = 0 Event N is inactive or irq[N] is LOW. Bit [N] = 1 Event N is active or irq[N] is HIGH.

DMAC_PERI_INTMIS
Address:Operational Base+0x28
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the status of the interrupts that are active in the DMAC: Bit [N] = 0 Interrupt N is inactive and therefore irq[N] is LOW. Bit [N] = 1 Interrupt N is active and therefore irq[N] is HIGH

DMAC_PERI_INTCLR
Address:Operational Base+0x2c
Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:0	W	0x0	Controls the clearing of the irq outputs: Bit [N] = 0 The status of irq[N] does not change. Bit [N] = 1 The DMAC sets irq[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change.

DMAC_PERI_FSRD
Address:Operational Base+0x30
Fault Status DMA Manager Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the fault status of the DMA manager. Read as: 0 = the DMA manager thread is not in the Faulting state 1 = the DMA manager thread is in the Faulting state.

DMAC_PERI_FSRC
Address:Operational Base+0x34
Fault Status DMA Channel Register

Bit	Attr	Reset Value	Description
31:0	R	0x0	Each bit provides the fault status of the corresponding channel. Read as: Bit [N] = 0 No fault is present on DMA channel N. Bit [N] = 1 DMA channel N is in the Faulting or Faulting completing state.

DMAC_PERI_FTRD
Address:Operational Base+0x38
Fault Type DMA Manager Register

Bit	Attr	Reset Value	Description
31	-	-	reserved
30	R	0x0	If the DMA manager aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface: 0 = instruction that generated an abort was read from

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Bit	Attr	Reset Value	Description
			system memory 1 = instruction that generated an abort was read from the debug interface.
29:17	-	-	reserved
16	R	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA manager performs an instruction fetch: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response
15:6	-	-	reserved
5	R	0x0	Indicates if the DMA manager was attempting to execute DMAWFE or DMASEV with inappropriate security permissions: 0 = DMA manager has appropriate security to execute DMAWFE or DMASEV 1 = a DMA manager thread in the Non-secure state attempted to execute either: • DMAWFE to wait for a secure event • DMASEV to create a secure event or secure interrupt
4	R	0x0	ndicates if the DMA manager was attempting to execute DMAGO with inappropriate security permissions: 0 = DMA manager has appropriate security to execute DMAGO 1 = a DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state.
3:2	-	-	reserved
1	R	0x0	Indicates if the DMA manager was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 0 = valid operand 1 = invalid operand.
0	R	0x0	Indicates if the DMA manager was attempting to execute an undefined instruction: 0 = defined instruction 1 = undefined instruction.

DMAC_PERI_FTR0~DMAC_PERI_FTR6

Address:Operational Base+0x40
Operational Base+0x44
Operational Base+0x48
Operational Base+0x4c
Operational Base+0x50
Operational Base+0x54
Operational Base+0x58

Fault Type DMA Channel Register

Bit	Attr	Reset Value	Description
31	R	0x0	Indicates if the DMA channel has locked-up because of resource starvation: 0 = DMA channel has adequate resources 1 = DMA channel has locked-up because of insufficient resources. This fault is an imprecise abort
30	R	0x0	If the DMA channel aborts, this bit indicates if the

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Bit	Attr	Reset Value	Description
			erroneous instruction was read from the system memory or from the debug interface: 0 = instruction that generated an abort was read from system memory 1 = instruction that generated an abort was read from the debug interface. This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	-	-	reserved
18	R	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs a data read: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is an imprecise abort
17	R	0x0	Indicates the AXI response that the DMAC receives on the BRESP bus, after the DMA channel thread performs a data write: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is an imprecise abort.
16	R	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs an instruction fetch: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is a precise abort.
15:14	-	-	reserved
13	R	0x0	Indicates if the MFIFO did not contain the data to enable the DMAC to perform the DMAST: 0 = MFIFO contains all the data to enable the DMAST to complete 1 = previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete. This fault is a precise abort.
12	R	0x0	Indicates if the MFIFO prevented the DMA channel thread from executing DMALD or DMAST. Depending on the instruction: DMALD 0 = MFIFO contains sufficient space 1 = MFIFO is too small to hold the data that DMALD requires. DMAST 0 = MFIFO contains sufficient data 1 = MFIFO is too small to store the data to enable DMAST to complete. This fault is an imprecise abort
11:8	-	-	reserved
7	R	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to program the CCRn Register to perform a secure read or secure write: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write. This fault is a precise abort
6	R	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to execute DMAWFP, DMALDP, DMASTP,

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Bit	Attr	Reset Value	Description
			or DMAFLUSHP with inappropriate security permissions: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to execute either: • DMAWFP to wait for a secure peripheral • DMALDP or DMASTP to notify a secure peripheral • DMAFLUSHP to flush a secure peripheral. This fault is a precise abort.
5	R	0x0	Indicates if the DMA channel thread attempts to execute DMAWFE or DMASEV with inappropriate security permissions: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to execute either: • DMAWFE to wait for a secure event • DMASEV to create a secure event or secure interrupt. This fault is a precise abort.
4:2	-	-	reserved
1	R	0x0	Indicates if the DMA channel thread was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 0 = valid operand 1 = invalid operand. This fault is a precise abort.
0	R	0x0	Indicates if the DMA channel thread was attempting to execute an undefined instruction: 0 = defined instruction 1 = undefined instruction. This fault is a precise abort

DMAC_PERI_CSR0~DMAC_PERI_CSR6

Address:Operational Base+0x100
Operational Base+0x108
Operational Base+0x110
Operational Base+0x118
Operational Base+0x120
Operational Base+0x128
Operational Base+0x130

Channel Status Registers

Bit	Attr	Reset Value	Description
31:22	-	-	reserved
21	R	0x0	The channel non-secure bit provides the security of the DMA channel: 0 = DMA channel operates in the Secure state 1 = DMA channel operates in the Non-secure state
20:16	-	-	reserved
15	R	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the periph operand was set: 0 = DMAWFP executed with the periph operand not set 1 = DMAWFP executed with the periph operand set
14	R	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the burst or single operand were set:

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			0 = DMAWFP executed with the single operand set 1 = DMAWFP executed with the burst operand set.
13:9	-	-	reserved
8:4	R	0x0	If the DMA channel is in the Waiting for event state or the Waiting for peripheral state then these bits indicate the event or peripheral number that the channel is waiting for: b00000 = DMA channel is waiting for event, or peripheral, 0 b00001 = DMA channel is waiting for event, or peripheral, 1 b00010 = DMA channel is waiting for event, or peripheral, 2 ... b11111 = DMA channel is waiting for event, or peripheral, 31
3:0	R	0x0	The channel status encoding is: b0000 = Stopped b0001 = Executing b0010 = Cache miss b0011 = Updating PC b0100 = Waiting for event b0101 = At barrier b0110 = reserved b0111 = Waiting for peripheral b1000 = Killing b1001 = Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMAC_PERI_CPC0~DMAC_PERI_CPC6

Address:Operational Base+0x104
Operational Base+0x10c
Operational Base+0x114
Operational Base+0x11c
Operational Base+0x124
Operational Base+0x12c
Operational Base+0x134

Channel Program Counter Registers

Bit	Attr	Reset Value	Description
31:0	R	0x0	Program counter for the DMA channel n thread

DMAC_PERI_SAR0~DMAC_PERI_SAR6

Address:Operational Base+0x400
Operational Base+0x420
Operational Base+0x440
Operational Base+0x460
Operational Base+0x480
Operational Base+0x4a0
Operational Base+0x4c0

Source Address Registers

Bit	Attr	Reset Value	Description
31:0	R	0x0	Address of the source data for DMA channel n

DMAC_PERI_DAR0~DMAC_PERI_DAR5

Address:Operational Base+0x404
Operational Base+0x424
Operational Base+0x444
Operational Base+0x464
Operational Base+0x484
Operational Base+0x4a4

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DestinationAddress Registers

Bit	Attr	Reset Value	Description
31:0	R	0x0	Address of the Destinationdata for DMA channel n

DMAC_PERI_CCR0~DMAC_PERI_CCR6

Address:Operational Base+0x408
Operational Base+0x428
Operational Base+0x448
Operational Base+0x468
Operational Base+0x488
Operational Base+0x4a8
Operational Base+0x4c8

Channel Control Registers

Bit	Attr	Reset Value	Description
31:28	-	-	reserved
27:25	R	0x0	Programs the state of AWCACHE[3,1:0]a when the DMAC writes the destination data. Bit [27] 0 = AWCACHE[3] is LOW 1 = AWCACHE[3] is HIGH. Bit [26] 0 = AWCACHE[1] is LOW 1 = AWCACHE[1] is HIGH. Bit [25] 0 = AWCACHE[0] is LOW 1 = AWCACHE[0] is HIGH
24:22	R	0x0	Programs the state of AWPROT[2:0]a when the DMAC writes the destination data. Bit [24] 0 = AWPROT[2] is LOW 1 = AWPROT[2] is HIGH. Bit [23] 0 = AWPROT[1] is LOW 1 = AWPROT[1] is HIGH. Bit [22] 0 = AWPROT[0] is LOW 1 = AWPROT[0] is HIGH
21:18	R	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it writes the destination data: b0000 = 1 data transfer b0001 = 2 data transfers b0010 = 3 data transfers ... b1111 = 16 data transfers. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size
17:15	R	0x0	For each beat within a burst, it programs the number of bytes that the DMAC writes to the destination: b000 = writes 1 byte per beat b001 = writes 2 bytes per beat b010 = writes 4 bytes per beat b011 = writes 8 bytes per beat b100 = writes 16 bytes per beat b101-b111 = reserved. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	R	0x0	Programs the burst type that the DMAC performs when it writes the destination data: 0 = Fixed-address burst. The DMAC signals AWBURST[0] LOW.

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Bit	Attr	Reset Value	Description
			1 = Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	R	0x0	Set the bits to control the state of ARCACHE[2:0]a when the DMAC reads the source data. Bit [13] 0 = ARCACHE[2] is LOW 1 = ARCACHE[2] is HIGH. Bit [12] 0 = ARCACHE[1] is LOW 1 = ARCACHE[1] is HIGH. Bit [11] 0 = ARCACHE[0] is LOW 1 = ARCACHE[0] is HIGH.
10:8	R	0x0	Programs the state of ARPROT[2:0]a when the DMAC reads the source data. Bit [10] 0 = ARPROT[2] is LOW 1 = ARPROT[2] is HIGH. Bit [9] 0 = ARPROT[1] is LOW 1 = ARPROT[1] is HIGH. Bit [8] 0 = ARPROT[0] is LOW 1 = ARPROT[0] is HIGH.
7:4	R	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it reads the source data: b0000 = 1 data transfer b0001 = 2 data transfers b0010 = 3 data transfers ... b1111 = 16 data transfers. The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size
3:1	R	0x0	For each beat within a burst, it programs the number of bytes that the DMAC reads from the source: b000 = reads 1 byte per beat b001 = reads 2 bytes per beat b010 = reads 4 bytes per beat b011 = reads 8 bytes per beat b100 = reads 16 bytes per beat b101-b111 = reserved. The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size
0	R	0x0	Programs the burst type that the DMAC performs when it reads the source data: 0 = Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1 = Incrementing-address burst. The DMAC signals ARBURST[0] HIGH

DMAC_PERI_LC0_0~DMAC_PERI_LC0_6

Address:Operational Base+0x40c
Operational Base+0x42c
Operational Base+0x44c
Operational Base+0x46c
Operational Base+0x48c
Operational Base+0x4ac
Operational Base+0x4cc

Loop Counter 0 Registers

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Bit	Attr	Reset Value	Description
31:8	-	-	reserved
7:0	R	0x0	Loop counter 0 iterations

DMAC_PERI_LC1_0~DMAC_PERI_LC1_6

Address:Operational Base+0x410
Operational Base+0x430
Operational Base+0x450
Operational Base+0x470
Operational Base+0x490
Operational Base+0x4b0
Operational Base+0x4e0

Loop Counter 1 Registers

Bit	Attr	Reset Value	Description
31:8	-	-	reserved
7:0	R	0x0	Loop counter 1 iterations

DMAC_PERI_DBGSTATUS

Address:Operational Base+0xd00
Debug Status Register

Bit	Attr	Reset Value	Description
31:2	-	-	reserved
1:0	R	0x0	The debug encoding is as follows: b00 = execute the instruction that the DBGINST [1:0] Registers contain b01 = reserved b10 = reserved b11 = reserved.

DMAC_PERI_DBGCMD

Address:Operational Base+0xd04
Debug Command Register

Bit	Attr	Reset Value	Description
31:2	-	-	reserved
1:0	W	0x0	The debug encoding is as follows: b00 = execute the instruction that the DBGINST [1:0] Registers contain b01 = reserved b10 = reserved b11 = reserved

DMAC_PERI_DBGINST0

Address:Operational Base+0xd08
Debug Instruction-0 Register

Bit	Attr	Reset Value	Description
31:24	W	0x0	Instruction byte 1
23:16	W	0x0	Instruction byte 0
17:11	-	-	reserved
10:8	W	0x0	DMA channel number: b000 = DMA channel 0 b001 = DMA channel 1 b010 = DMA channel 2 … b111 = DMA channel 7

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Bit	Attr	Reset Value	Description
7:1	-	-	reserved
0	W	0x0	The debug thread encoding is as follows: 0 = DMA manager thread 1 = DMA channel.

DMAC_PERI_DBGINST1

Address:Operational Base+0xd0c

Debug Instruction-1 Register

Bit	Attr	Reset Value	Description
31:24	W	0x0	Instruction byte 5
23:16	W	0x0	Instruction byte 4
15:8	W	0x0	Instruction byte 3
7:0	W	0x0	Instruction byte 2

DMAC_PERI_CR0

Address:Operational Base+0xe00

Configuration Register 0

Bit	Attr	Reset Value	Description
31:22	-	-	reserved
21:17	R	0x2	Number of interrupt outputs that the DMAC provides: b00000 = 1 interrupt output, irq[0] b00001 = 2 interrupt outputs, irq[1:0] b00010 = 3 interrupt outputs, irq[2:0] ... b11111 = 32 interrupt outputs, irq[31:0].
16:12	R	0x7	Number of peripheral request interfaces that the DMAC provides: b00000 = 1 peripheral request interface b00001 = 2 peripheral request interfaces b00010 = 3 peripheral request interfaces ... b11111 = 32 peripheral request interfaces.
11:7	-	-	reserved
6:4	R	0x5	Number of DMA channels that the DMAC supports: b000 = 1 DMA channel b001 = 2 DMA channels b010 = 3 DMA channels ... b111 = 8 DMA channels.
3	-	-	reserved
2	R	0x0	Indicates the status of the boot_manager_ns signal when the DMAC exited from reset: 0 = boot_manager_ns was LOW 1 = boot_manager_ns was HIGH.
1	R	0x0	Indicates the status of the boot_from_pc signal when the DMAC exited from reset: 0 = boot_from_pc was LOW 1 = boot_from_pc was HIGH
0	R	0x1	Supports peripheral requests: 0 = the DMAC does not provide a peripheral request interface 1 = the DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies.

DMAC_PERI_CR1

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Address:Operational Base+0xe04
Configuration Register 1

Bit	Attr	Reset Value	Description
31:8	-	-	reserved
7:4	R	0x5	[7:4] num_i-cache_lines Number of i-cache lines: b0000 = 1 i-cache line b0001 = 2 i-cache lines b0010 = 3 i-cache lines … b1111 = 16 i-cache lines.
3	-	-	reserved
2:0	R	0x7	The length of an i-cache line: b000-b001 = reserved b010 = 4 bytes b011 = 8 bytes b100 = 16 bytes b101 = 32 bytes b110-b111 = reserved

DMAC_PERI_CR2
Address:Operational Base+0xe08
Configuration Register 2

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMAC_PERI_CR3
Address:Operational Base+0xe0c
Configuration Register 3

Bit	Attr	Reset Value	Description
31:0	R	0x0	Provides the security state of an event-interrupt resource: Bit [N] = 0 Assigns event<N> or irq[N] to the Secure state. Bit [N] = 1 Assigns event<N> or irq[N] to the Non-secure state.

DMAC_PERI_CR4
Address:Operational Base+0xe10
Configuration Register 4

Bit	Attr	Reset Value	Description
31:0	R	0x6	Provides the security state of the peripheral request interfaces: Bit [N] = 0 Assigns peripheral request interface N to the Secure state. Bit [N] = 1 Assigns peripheral request interface N to the Non-secure state

DMAC_PERI_CRDn
Address:Operational Base+0xe14
DMA Configuration Register

Bit	Attr	Reset Value	Description
31:30	-	-	reserved
29:20	R	0x20	The number of lines that the data buffer contains: b000000000 = 1 line b000000001 = 2 lines

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Bit	Attr	Reset Value	Description
			… b111111111 = 1024 lines
19:16	R	0x9	The depth of the read queue: b0000 = 1 line b0001 = 2 lines ... b1111 = 16 lines.
15	-	-	reserved
14:12	R	0x4	Read issuing capability that programs the number of outstanding read transactions: b000 = 1 b001 = 2 … b111 = 8
11:8	R	0x7	The depth of the write queue: b0000 = 1 line b0001 = 2 lines … b1111 = 16 lines.
7	-	-	reserved
6:4	R	0x3	Write issuing capability that programs the number of outstanding write transactions: b000 = 1 b001 = 2 … b111 = 8
3	-	-	reserved
2:0		0x3	The data bus width of the AXI interface: b000 = reserved b001 = reserved b010 = 32-bit b011 = 64-bit b100 = 128-bit b101-b111 = reserved.

DMAC_PERI_WD
Address:Operational Base+0xe80
DMA Watchdog Register

Bit	Attr	Reset Value	Description
31:1	-	-	reserved
0	RW	0x0	Controls how the DMAC responds when it detects a lock-up condition: 0 = the DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1 = the DMAC sets irq_abort HIGH.

15.5 Timing Diagram

Please refer to chapter 14.5 for the similar description.

15.6 Interface Description

DMAC_PERI has the following tie-off signals.It can be configured by GRF register.(Please refer

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to the chapter to find how to configure)

DMAC_PERI

interface	Reset value	Control source
boot_addr	0x0	GRF
boot_from_pc	0x0	GRF
boot_manager_ns	0x0	GRF
boot_irq_ns	0xf	GRF
boot_periph_ns	0xfffff	GRF

boot_addr
Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
boot_from_pc
Controls the location in which the DMAC executes its initial instruction, after it exits from reset:
0 = DMAC waits for an instruction from either APB interface
1 = DMA manager thread executes the instruction that is located at the address that
boot_manager_ns
When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
0 = assigns DMA manager to the Secure state
1 = assigns DMA manager to the Non-secure state.
boot_irq_ns
Controls the security state of an event-interrupt resource, when the DMAC exits from reset:
boot_irq_ns[x] is LOW
The DMAC assigns event<x> or irq[x] to the Secure state.
boot_irq_ns[x] is HIGH
The DMAC assigns event<x> or irq[x] to the Non-secure state.
boot_periph_ns
Controls the security state of a peripheral request interface, when the DMAC exits from reset:
boot_periph_ns[x] is LOW
The DMAC assigns peripheral request interface x to the Secure state.
boot_periph_ns[x] is HIGH
The DMAC assigns peripheral request interface x to the Non-secure state.

15.7 Application Notes

Please refer to chapter 14.7 for the similar description.

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Chapter 16 System Security

16.1 Overview

The RK3288 uses the TrustZone access control scheme to support the system security application requirement.

16.2 Block Diagram

The following figure is the system security architecture. All the devices which support security access are demonstrated in this figure.

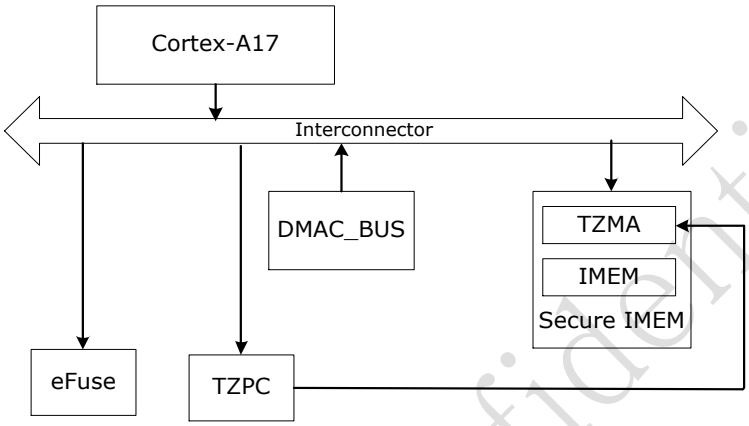

Fig. 16-1 RK3288 security architecture

16.3 Function Description

16.3.1 Cortex-A17 Security Extension architecture

The processor implements the TrustZone Security Extensions architecture to facilitate the development of secure applications.
Security Extensions are based on these fundamental principles:

- The extensions define a class of core operation that you can switch between secure and non-secure state. Most code runs in non-secure state. Only trusted code runs in secure state
- The extensions define some memory as secure memory. When the core is in secure state, it can access secure memory
- Entry into secure state is strictly controlled
- Exit from secure state can only occur at programmed points
- Debug is strictly controlled
- The processor enters secure state on reset

16.3.2 TZPC

The TZPC (Trust Protection Controller) is the APB slave, which configured by software and control secure memory space of Embedded SRAM and system security device setting. The TZPC support the following feature

control the secure memory size of secure Embedded SRAM by configuring TZPCR0SIZE
control DMAC_BUS Secure-Configuration bit by configuring TZPCDECPROT1 and TZPCDECPROT2

The following is the TZPC block diagram.

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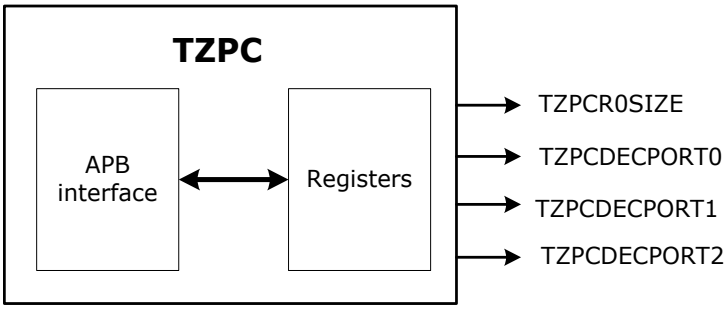

Fig. 16-2 TZPC block diagram

The TZPC can only be accessed on secure world and the software can configure the following items:

- Configure TZPCR0SIZE to set TZMA secure access space, which can be 0KB, 4KB, 8KB, 12KB… up to 96KB by 4KB step
- Configure TZPCDECPORTx to set DMAC_BUS secure input port

Note: Please refer to the registers of TZPC_DECPROT0Set, TZPC_DECPROT1Set and TZPC_DECPROT2 Set for detailed information about TZPCDECPORTx.

16.3.3 TZMA

The TZMA (TrustZone Memory Adapter) is a bridge between AXI bus and Embedded SRAM, which support the flexible secure access by controlling R0SIZE port.

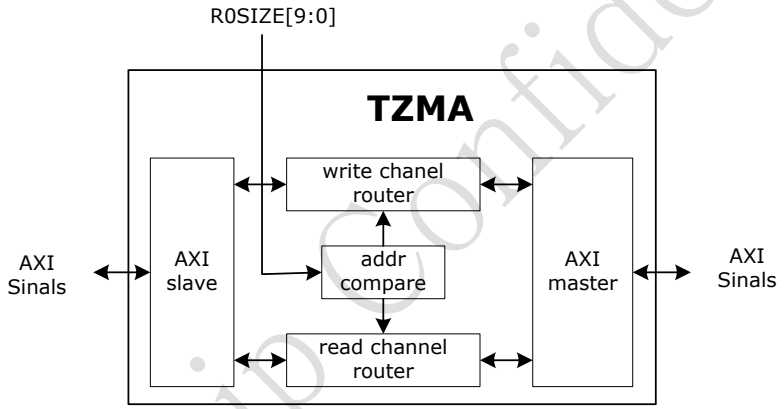

Fig. 16-3 TZMA block diagram

TZMA can support 0KB, 4KB, 8KB, 12KB… up to 96KB by 4KB step(the whole Embedded SRAM space) secure access by setting R0SIZE[9:0].

16.3.4 DMAC_BUS secure access

The DMAC_BUS is an AMBA compliant peripheral, which provides an AXI interface to perform the DMA transfer and two APB interfaces that control its operation. The DMAC_BUS implements TrustZone secure technology with one APB interface operating in the secure state and the other operating in the Non-secure state. For the detailed description for DMAC_BUS, please refer to Chapter 14.

The following diagram shows the interface of DMAC_BUS.

Fig. 16-4 DMAC_BUS interface

The DMAC_BUS support the secure feature in the following section:

DMA manager thread
DMA channel thread
Event and interrupts

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Peripheral request interface
1. The security of DMA manager thread is controlled by input port boot_manager_ns.
0=assign DMA manager to the Secure state
1=assign DMA manager to the Non-secure state
2. The security of DMA channel thread is controlled by instruction DMAGO ns bit. If ns is present, DMA channel operation is in the non-secure state. Otherwise, the execution of the instruction depends on the security of the state of DMA manager:
DMA manager is in the secure state, DMA channel operates in the secure state
DMA manager is in the non-secure state, DMA abort
3. The security state of the event-interrupt source is controlled by the input port boot_irq_ns[x:0], if boot_irq_ns[x] is LOW, the DMAC_BUS assign event<x> or irq[x] to the secure state, otherwise the DMAC_BUS assign event<x> or irq[x] to the non-secure state.
4. The security state of peripheral request interface is controlled by the input port boot_irq_ns[x], if boot_irq_ns[x] is lOW, the DMAC_BUS assign peripheral interface x to secure state, otherwise the DMAC_BUS assign peripheral interface x to non-secure state.

16.3.5 Bus components security setting

The following table describes the security support on bus components which have the master interface or slave interface.

Table 16-1 bus components security setting

AXI master	secure	All transactions originating from this master interface are flagged as secure transaction and can access both secure and non-secure component.
	non-secure	All transactions originating from this master interface are flagged as non-secure transactions and cannot access secure component
	per access	The AxPROTx signal determines the security setting of each transaction, and the slave that it can access
AHB-Lite master	secure	All transactions originating from this master interface are flagged as secure transaction and can access both secure and non-secure component.
	non-secure	All transactions originating from this master interface are flagged as non-secure transactions and cannot access secure component
AXI slave	secure	Only secure transactions can access this component
	non-secure	Both secure and non-secure transactions can access this components
	boot-secure	You can use software to configure whether it permits secure and non-secure transactions to access component. When boot up, this component only can be accessed by secure transactions.
AHB slave	secure	Only secure transactions can access this components
	non-secure	Both secure and non-secure transactions can access this components
	boot-secure	You can use software to configure whether it permit secure and non-secure transactions to access this components. When boot up, this component only can be accessed by secure transactions.
APB slave	secure	Only secure transactions can access this components
	non-secure	Both secure and non-secure transactions can access this components
	boot-secure	You can use software to configure whether it permit secure and non-secure transactions to access this components. When boot up, this component only can be accessed by secure transactions.

Notes: When a non-secure master tries to access a secure slave, an error response will be returned. In RK3288,

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Cortex-A17 non-secure access a secure slave will cause a data-abort, and dmac_bus non-secure access a secure slave will cause an interrupt for access error.

16.3.6 RK3288 secure device setting

Table 16-2 RK3288 secure device setting

Cortex-A17	AXI master	Per access
TZPC	APB slave	Secure
eFuse	APB slave	Secure
Embedded SRAM	AXI slave	Controlled by TZMA, the secure space can be set to 0, 4KB, 8KB, 12KB …up to 96KB
DMAC_BUS	AXI master	Per access
	Secure APB slave	Secure
	Non-secure APB slave	Non-secure

16.3.7 RK3288 device secure input port setting

The following table lists all the secure input ports for the secure device. These secure input ports could be set by configuring TZPCDECPORTx registers. Please refer to 16.4.2 for detailed information.

Table 16-3 RK3288 device secure input port setting

Input Port	Module	Function description
boot_manager_ns	DMAC_BUS	When the DMAC exits from reset, this signal controls the security state of the DMAmanager thread: 1'b0: assigns DMA manager to the secure state 1'b1: assigns DMA manager to the non-secure state
boot_perih_ns[2:0]	DMAC_BUS	Controls the security state of a peripheral request interface, when the DMAC exits from reset: boot_periph_ns[x] is LOW The DMAC assigns peripheral request interface x to the secure state boot_periph_ns[x] is HIGH The DMAC assigns peripheral request interface x to the non-secure state.
boot_irq_ns[7:0]	DMAC_BUS	Controls the security state of an event-interrupt resource, when the DMAC exits fromreset: boot_irq_ns[x] is LOW The DMAC assigns event<x> or irq[x] to the secure state. boot_irq_ns[x] is HIGH The DMAC assigns event<x> or irq[x] to the non-secure state.

16.4 Register Description

The base address of secure components TZPC is 0xffb00000.

16.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
TZPC_R0SIZE	0x000	W	0x00000200	Secure RAM region size register
TZPC_DECPROT1Stat	0x80c	W	0x000000ff	Secure-GRF register status
TZPC_DECPROT1Set	0x810	W	N/A	Secure-GRF register set
TZPC_DECPROT1Clr	0x814	W	N/A	Secure-GRF register clear
TZPC_DECPROT2Stat	0x818	W	0x00000006	Secure-GRF register status
TZPC_DECPROT2Set	0x81c	W	N/A	Secure-GRF register set
TZPC_DECPROT2Clr	0x820	W	N/A	Secure-GRF register clear

16.4.2 Detail Register Description

TZPC_R0SIZE

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Address :TZPC_BASE + offset(0x00)
Secure RAM Region Size Register

Bits	Attr	Reset Value	Description
31:10	R	0x0	Reserved
9:0	RW	0x200	Secure RAM region size in 4KB steps 9'b00: no secure region 9'b01: 4KB secure region 9'b10: 8KB secure region 9'b11: 12KB secure region … 0x200 or above sets the entire Embedded SRAM space to secure

TZPC_DECPROT1Stat
Address :TZPC_BASE + offset(0x80c)
Status bit for secure device input port control

Bits	Attr	Reset Value	Description
31:8	R	0x0	Reserved
7:2	R	0xff	Status bit for DMAC_BUS boot_perih_ns input port control
1:0	R	0x0	Reserved

TZPC_DECPROT1Set
Address :TZPC_BASE + offset(0x810)
Set bit for secure device input port control

Bits	Attr	Reset Value	Description
31:8	W	N/A	Reserved
7:2	W	N/A	Set bit for DMAC_BUS boot_perih_ns input port control
1:0	R	0x0	Reserved

TZPC_DECPROT1Clr
Address :TZPC_BASE + offset(0x814)
Set bit for secure device input port control

Bits	Attr	Reset Value	Description
31:8	W	N/A	Reserved
7:2	W	N/A	Clear bit for DMAC_BUS boot_perih_ns input port control
1:0	R	0x0	Reserved

TZPC_DECPROT2Stat
Address :TZPC_BASE + offset(0x818)
Status bit for secure device input port control

Bits	Attr	Reset Value	Description
31:8	R	0x0	Reserved
7:1	R	0x06	Status bit for DMAC_BUS boot_irq_ns input port control
0	R	0x0	Stabus bit for DMAC_BUS boot_manage_ns input port control

TZPC_DECPROT2Set
Address :TZPC_BASE + offset(0x81c)
Set bit for secure device input port control

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Bits	Attr	Reset Value	Description
31:8	W	N/A	Reserved
7:1	W	N/A	Set bit for DMAC_BUS boot_irq_ns input port control
0	W	N/A	Set bit for DMAC_BUS boot_manage_ns input port control

TZPC_DECPROT2Clr
Address :TZPC_BASE + offset(0x820)
Set bit for secure device input port control

Bits	Attr	Reset Value	Description
31:8	W	undef	Reserved
7:1	W	undef	Clear bit for DMAC_BUS boot_irq_ns input port control
0	W	undef	Clear bit for DMAC_BUS boot_manage_ns input port control

16.5 Application Notes

Secure software conception
The basis of the security extensions model is that the computing environment splits into two isolated states, the secure state and the non-secure state, with no leakage of secure data to the non-secure state. Software secure monitor code, running in the monitor mode, links the two states and acts as a gatekeeper to manage program flow. The system can have both secure and non-secure peripherals that are suitable to secure and non-secure device driver control. Following figure shows the relationship between the secure and non-secure states. The operating system (OS) splits into the secure OS, that includes the secure kernel, and the non-secure OS, that includes the non-secure kernel.

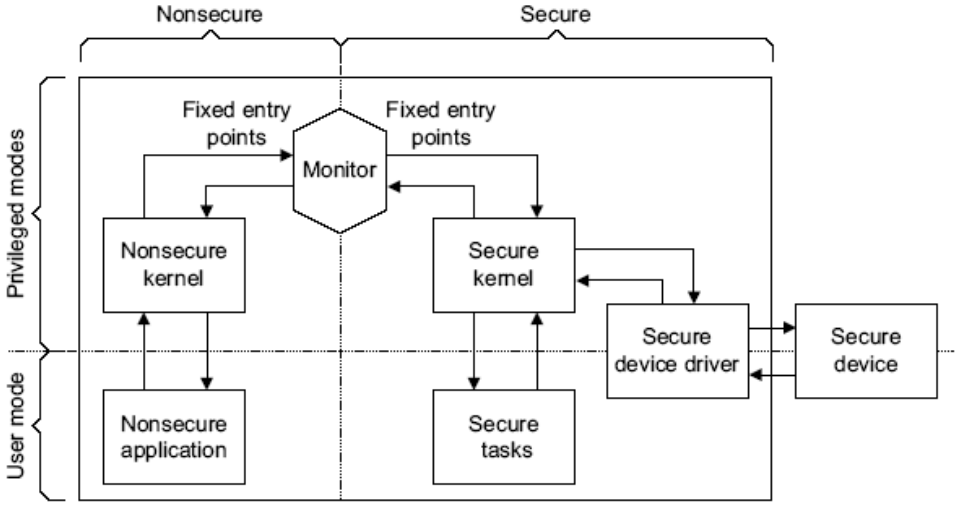

Fig. 16-5 Software Diagram of Secure and Non-secure

In normal non-secure operation, the OS runs tasks in the usual way. When a user process requires secure execution it makes a request to the secure kernel, that operates in privileged mode. This then calls the secure monitor to transfer execution to the secure state.
This approach to secure systems means that the platform OS that works in the non-secure state, has only a few fixed entry points into the secure state through the secure monitor. The trusted code base for the secure state, that includes the secure kernel and secure device drivers, is small and therefore much easier to maintain and verify.

Secure/Non-secure memory space for Embedded SRAM
The following figure gives an example of embedded SRAM secure/non-secure memory space setting. The software configure 4KB secure space by setting TZPC_R0SIZE=0x1. The bottom

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4KB space will act as secure space and the other 92K space will be non-secure space.

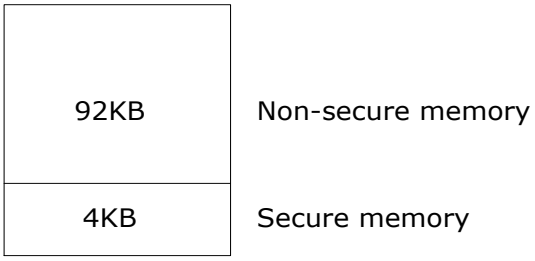

Fig. 16-6 Embedded SRAM secure memory space setting

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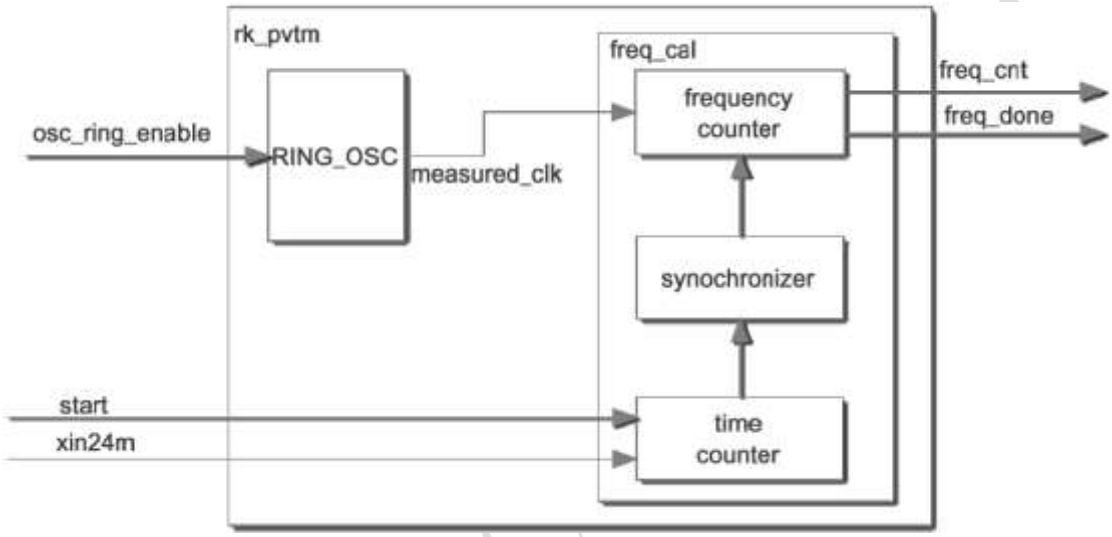
Chapter 17 Process-Voltage-Temperature Monitor (PVTM)

17.1 Overview

The Process-Voltage-Temperature Monitor (PVTM) is used to monitor the chip performance variance caused by chip process, voltage and temperature.
PVTM supports the following features:

- a clock oscillation ring is integrated and used to generate a clock like signal, the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit
- a frequency counter is used to measure the frequency of the clock oscillation ring.

17.2 Block Diagram



The PVTM include two main blocks

RING_OSC, it is composed with inverters with odd number, which is used to generate a clock

Freq_cal, it is used to measure the frequency of clock which generated from the RING_SOC block

Frequency Calculation

A frequency fixed clock(24MH) is used to calculate the clock cycles of RING_OSC generated clock. Suppose the time period is 1s, then the clock period of RING_OSC clock is T= 1/2*clock_counter(s)

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Chapter 18 Temperature-Sensor ADC(TS-ADC)

18.1 Overview

TS-ADC Controller module supports user-defined mode and automatic mode. User-defined mode refers, TSADC all the control signals entirely by software writing to register for direct control. Automatic mode refers to the module automatically poll TSADC output, and the results were checked. If you find that the temperature High in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC.
TS-ADC Controller supports the following features:

Support User-Defined Mode and Automatic Mode
In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
In Automatic Mode, the temperature of alarm interrupt can be configurable
In Automatic Mode, the temperature of system reset can be configurable
Support to 4 channel TS-ADC, the temperature criteria of each channel can be configurable
In Automatic Mode, the time interval of temperature detection can be configurable
In Automatic Mode, when detecting a high temperature, the time interval of temperature detection can be configurable
High temperature debounce can be configurable

18.2 Block Diagram

TS-ADC controller comprises with:

APB Interface
TS-ADC control logic

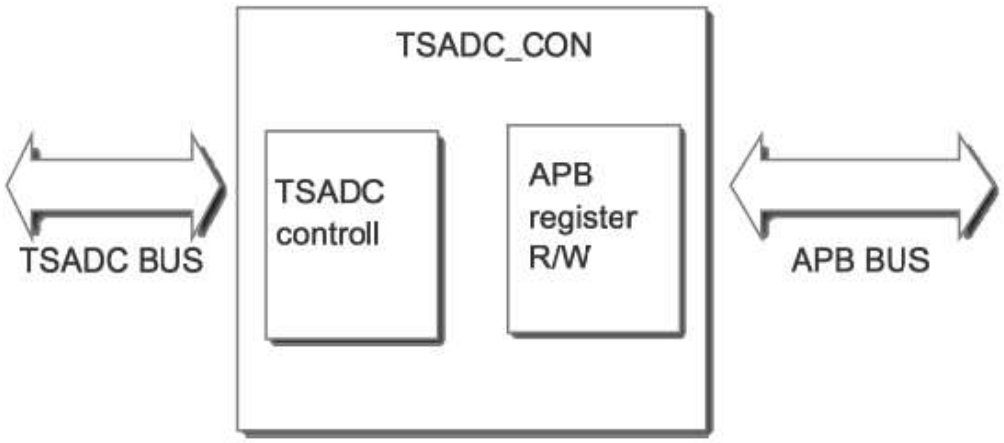

Fig. 18-1 TS-ADC Controller Block Diagram

18.3 Function Description

18.3.1 APB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

18.3.2 TS-ADC Controller

This block is exploited to realize binary search algorithm, storing the intermediate result and generate control signal for analog block. This block compares the analog input with the voltage generated from D/A Converter, and output the comparison result to SAR and Control Logic Block for binary search. Three level amplifiers are employed in this comparator to provide enough gain.

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18.4 Register Description

18.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000208	The control register of A/D Converter.
TSADC_AUTO_CON	0x0004	W	0x00000000	TSADC auto mode control register
TSADC_INT_EN	0x0008	W	0x00000000	Interrupt enable
TSADC_INT_PD	0x000c	W	0x00000000	Interrupt Status
TSADC_DATA0	0x0020	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA1	0x0024	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA2	0x0028	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA3	0x002c	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_COMP0_INT	0x0030	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_INT	0x0034	W	0x00000000	TSADC high temperature level for source 1
TSADC_COMP2_INT	0x0038	W	0x00000000	TSADC high temperature level for source 2
TSADC_COMP3_INT	0x003c	W	0x00000000	TSADC high temperature level for source 3
TSADC_COMP0_SHUT	0x0040	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_SHUT	0x0044	W	0x00000000	TSADC high temperature level for source 1
TSADC_COMP2_SHUT	0x0048	W	0x00000000	TSADC high temperature level for source 2
TSADC_COMP3_SHUT	0x004c	W	0x00000000	TSADC high temperature level for source 3
TSADC_HIGHT_INT_DEBOUNCE	0x0060	W	0x00000003	high temperature debounce
TSADC_HIGHT_TSHUT_DEBOUNCE	0x0064	W	0x00000003	high temperature debounce
TSADC_AUTO_PERIOD	0x0068	W	0x00010000	TSADC auto access period
TSADC_AUTO_PERIOD_HT	0x006c	W	0x00010000	TSADC auto access period when temperature is high

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

18.4.2 Detail Register Description

TSADC_USER_CON
Address: Operational Base + offset (0x0000)

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The control register of A/D Converter.

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	adc_status ADC status (EOC) 0: ADC stop; 1: Conversion in progress.
11:6	RW	0x08	inter_pd_soc interleave between power down and start of conversion
5	RW	0x0	start When software write 1 to this bit , start_of_conversion will be assert. This bit will be cleared after TSADC access finishing.
4	RW	0x0	start_mode start mode. 0: tsadc controller will asert start_of_conversion after "inter_pd_soc" cycles. 1: the start_of_conversion will be controlled by TSADC_USER_CON[5].
3	RW	0x1	adc_power_ctrl ADC power down control bit 0: ADC power down; 1: ADC power up and reset.
2:0	RW	0x0	adc_input_src_sel ADC input source selection(CH_SEL[2:0]). 111 : Input source 0 (SARADC_AIN[0]) 110 : Input source 1 (SARADC_AIN[1]) 101 : Input source 2 (SARADC_AIN[2]) 100 : Input source 3 (SARADC_AIN[3]) Others : Reserved

TSADC_AUTO_CON

Address: Operational Base + offset (0x0004)

TSADC auto mode control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	last_tshut TSHUT status. This bit will set to 1 when tshut is valid, and only be cleared when application write 1 to it. This bit will not be cleared by system reset.
23:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17	RO	0x0	sample_dly_sel 0: AUTO_PERIOD is used. 1: AUTO_PERIOD_HT is used.
16	RO	0x0	auto_status 0: auto mode stop; 1: auto mode in progress.
15:9	RO	0x0	reserved
8	RW	0x0	tshut polarity 0: low active 1: high active
7	RW	0x0	src3_en 0: do not care the temperature of source 3 1: if the temperature of source 3 is too high , TSHUT will be valid
6	RW	0x0	src2_en 0: do not care the temperature of source 2 1: if the temperature of source 2 is too high , TSHUT will be valid
5	RW	0x0	src1_en 0: do not care the temperature of source 1 1: if the temperature of source 1 is too high , TSHUT will be valid
4	RW	0x0	src0_en 0: do not care the temperature of source 0 1: if the temperature of source 0 is too high , TSHUT will be valid
3:1	RO	0x0	reserved
0	RW	0x0	auto_en 0: TSADC controller works at user-define mode 1: TSADC controller works at auto mode

TSADC_INT_EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	eoc_int_en eoc_Interrupt enable. eoc_interrupt enable in user defined mode 0: Disable; 1: Enable
11	RW	0x0	tshut_2cru_en_src3 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.

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Bit	Attr	Reset Value	Description
10	RW	0x0	tshut_2cru_en_src2 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
9	RW	0x0	tshut_2cru_en_src1 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
8	RW	0x0	tshut_2cru_en_src0 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
7	RW	0x0	tshut_2gpio_en_src3 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
6	RW	0x0	tshut_2gpio_en_src2 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
5	RW	0x0	tshut_2gpio_en_src1 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
4	RW	0x0	tshut_2gpio_en_src0 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
3	RW	0x0	ht_inten_src3 high temperature interrupt enable for src3 0: disable 1: enable
2	RW	0x0	ht_inten_src2 high temperature interrupt enable for src2 0: disable 1: enable
1	RW	0x0	ht_inten_src1 high temperature interrupt enable for src1 0: disable 1: enable
0	RW	0x0	ht_inten_src0 high temperature interrupt enable for src0 0: disable 1: enable

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TSADC_INT_PD
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	eoc_int_pd Interrupt status. This bit will be set to 1 when end-of-conversion. Set 0 to clear the interrupt.
7	RW	0x0	tshut_o_src3 TSHUT output status
6	RW	0x0	tshut_o_src2 TSHUT output status
5	RW	0x0	tshut_o_src1 TSHUT output status
4	RW	0x0	tshut_o_src0 TSHUT output status
3	RW	0x0	ht_irq_src3 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
2	RW	0x0	ht_irq_src2 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
1	RW	0x0	ht_irq_src1 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
0	RW	0x0	ht_irq_src0 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.

TSADC_DATA0
Address: Operational Base + offset (0x0020)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion (DOUT[9:0]).

TSADC_DATA1
Address: Operational Base + offset (0x0024)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 1 last conversion (DOUT[9:0]).

TSADC_DATA2
Address: Operational Base + offset (0x0028)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 2 last conversion (DOUT[9:0]).

TSADC_DATA3
Address: Operational Base + offset (0x002c)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 3 last conversion (DOUT[9:0]).

TSADC_COMP0_INT
Address: Operational Base + offset (0x0030)
TSADC high temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP1_INT
Address: Operational Base + offset (0x0034)
TSADC high temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP2_INT
Address: Operational Base + offset (0x0038)
TSADC high temperature level for source 2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src2 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP3_INT
Address: Operational Base + offset (0x003c)
TSADC high temperature level for source 3

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src3 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT
Address: Operational Base + offset (0x0040)
TSADC high temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP1_SHUT
Address: Operational Base + offset (0x0044)
TSADC high temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP2_SHUT
Address: Operational Base + offset (0x0048)
TSADC high temperature level for source 2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src2 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP3_SHUT
Address: Operational Base + offset (0x004c)
TSADC high temperature level for source 3

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src3 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGHT_INT_DEBOUNCE
Address: Operational Base + offset (0x0060)
high temperature debounce

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_INT for "debounce" times.

TSADC_HIGHT_TSHUT_DEBOUNCE
Address: Operational Base + offset (0x0064)
high temperature debounce

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_SHUT for "debounce" times.

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TSADC_AUTO_PERIOD
Address: Operational Base + offset (0x0068)
TSADC auto access period

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period when auto mode is enabled, this register controls the interleave between every two accessing of TSADC.

TSADC_AUTO_PERIOD_HT
Address: Operational Base + offset (0x006c)
TSADC auto access period when temperature is high

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT

18.5 Application Notes

18.5.1 Channel Select

The system has three Temperature Sensors, channel0 is reserve, and channel 1is for CPU, and channel 2 is for GPU.

18.5.2 Single-sample conversion

To saving power, the TS-ADC used single-sample conversion. The timing as flowing picture:

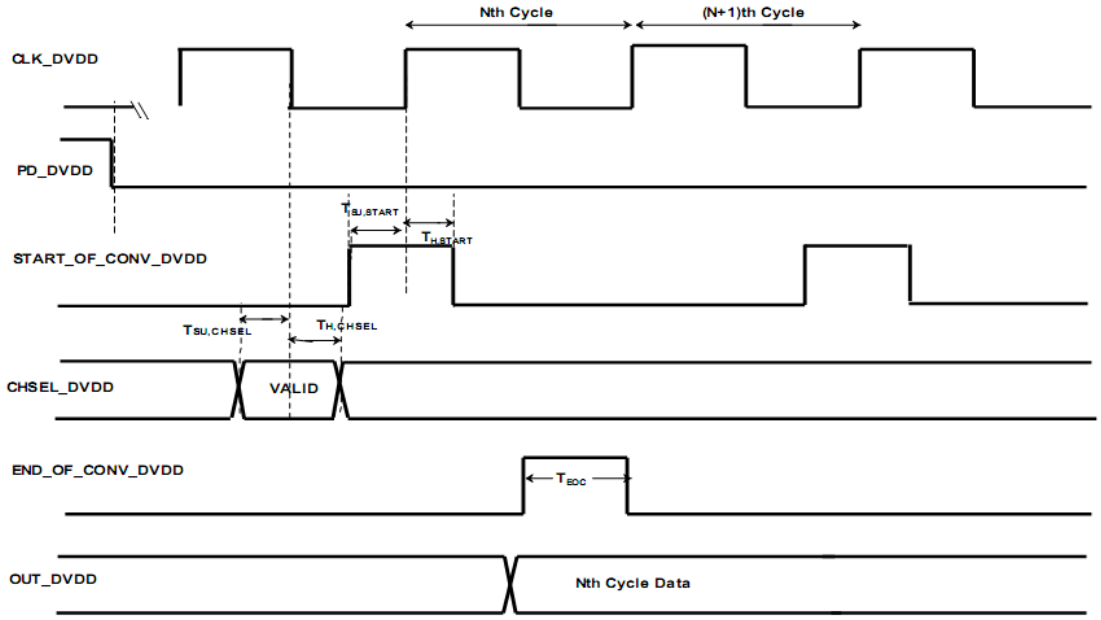

Fig. 18-2 Single-sample conversion

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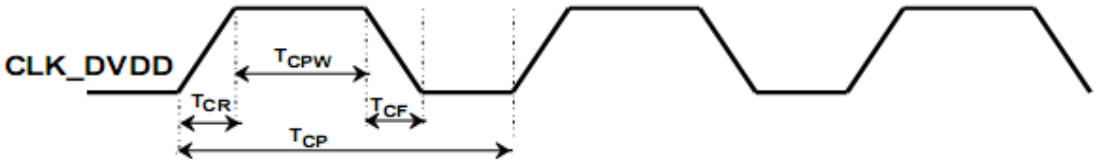

Fig. 18-3 Clock Timing Diagram

The below timing constraints are applicable for single-sample conversion mode.

Table 18-1 Timing parameters

Timing	Symbol	Value			Unit	Description
		Min	Typ	Max		
START_OF_CONV Setup time	TSU,START	5			ns	Set Up time for START_OF_CONV w.r.t CLKIN rising edge
START_OF_CONV Hold time	TH,START	5			ns	Hold time for START_OF_CONV w.r.t CLKIN rising edge
CHSEL setup time	TSU,CHSEL	5			ns	Set Up time for CHSEL w.r.t CLKIN falling edge
CHSEL Hold time	TH,CHSEL	5			ns	Hold time for CHSEL w.r.t CLKIN falling edge
Data Setup	TSU,DATA	11		15	us	Set Up time for output data w.r.t either CLKIN rising edge or END_OF_CONV falling edge
Data Hold	TH,DATA	5		9	us	Hold time for output data w.r.t either CLKIN rising edge or END_OF_CONV falling edge
Data access time	TDAC	5		9	us	Valid data w.r.t CLKIN rising edge
Delay time	TDelay			5	ns	Delay between Valid data and EOC_DVDD rising edge
EOC Pulse Width (max frequency)	TEOC	11		15	us	Pulse width of EOC
CLKIN Rise Time	TCR			2	ns	CLKIN Rise Time
CLKIN Fall Time	TCF			2	ns	CLKIN Fall Time
CLK Pulse Width(Duty Cycle)	TCPW	45		55	%	CLKIN High/Low Time Period
CLK Period	TCP	20			us	CLKIN Time Period

Note: The time from negedge of PD_DVDD to posedge of START_OF_CONV_DVDD is more than 8 cycles of CLK_DVDD, and less than 500us at same time.

18.5.3 Temperature-to-code mapping

Table 18-2 Temperature Code Mapping

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temp (C)	Code
-40	3800
-35	3792
-30	3783
-25	3774
-20	3765
-15	3756
-10	3747
-5	3737
0	3728
5	3718
10	3708
15	3698
20	3688
25	3678
30	3667
35	3656
40	3645
45	3634
50	3623
55	3611
60	3600
65	3588
70	3575
75	3563
80	3550
85	3537
90	3524
95	3510
100	3496
105	3482
110	3467
115	3452
120	3437
125	3421

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Note:

Code to Temperature mapping of the Temperature sensor is a piece wise linear curve. Any temperature, code faling between to 2 give temperatures can be linearly interpolated. Code to Temperature mapping should be updated based on sillcon results.

18.5.4 User-Define Mode

In user-define mode, the PD_DVDD and CHSEL_DVDD are generate by setting register TSADC_USER_CON, bit[3] and bit[2:0]. In order to ensure timing between PD_DVDD and CHSEL_DVDD, the CHSEL_DVDD must be set before the PD_DVDD.

In user-define mode, you can choose the method to control the START_OF_CONVERSION by setting bit[4] of TSADC_USER_CON. If set to 0, the start_of_conversion will be assert after "inter_pd_soc" cycles, which could be set by bit[11:6] of TSADC_USER_CON. And if start_mode was set 1, the start_of_conversion will be controlled by bit[5] of TSADC_USER_CON.

Software can get the four channel temperature from TSADC_DATAn (n=0,1,2,3).

18.5.5 Automatic Mode

You can use the automatic mode with the following step:

Set TSADC_AUTO_PERIOD，configure the interleave between every two accessing of TSADC in normal operation.

Set TSADC_AUTO_PERIOD_HT. configure the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.

Set TSADC_COMPn_INT(n=0,1,2,3), configure the high temperature level, if tsadc output is smaller than the value, means the temperature is high, tsadc_int will be asserted.

Set TSADC_COMPn_SHUT(n=0,1,2,3), configure the super high temperature level, if tsadc output is smaller than the value, means the temperature is too high, TSHUT will be asserted.

Set TSADC_INT_EN, you can enable the high temperature interrupt for all channel; and you can also set TSHUT output to gpio to reset the whole chip; and you can set TSHUT output to cru to reset the whole chip.

Set TSADC_HIGHT_INT_DEBOUNCE and TSADC_HIGHT_TSHUT_DEBOUNCE, if the temperature is higher than COMP_INT or COMP_SHUT for "debounce" times, TSADC controller will generate interrupt or TSHUT.

Set TSADC_AUTO_CON, enable the TSADC controller.

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Chapter 19 eFuse

19.1 Overview

In RK3288, there are two eFuse. One is organized as 32bits by 8 one-time programmable electrical fuses with random access interface, and the other is organized as 32bits by 32 one-time programmable electrical fuses.
The 32x32 eFuse can only be accessed by APB bus when IO_SECURITYsel is high.
It is a type of non-volatile memory fabricated in standard CMOS logic process. The main features are as follows:

- Programming condition : VQPS_EFUSE = 1.5V±10%
- Program time : 10us±0.2us .
- Read condition : VQPS_EFUSE = 0V
- Provide standby mode

19.2 Block Diagram

In the following diagram, all the signals except power supply VDD_EFUSE and VQPS_EFUSE are controlled by registers. For detailed description, please refer to detailed register descriptions.

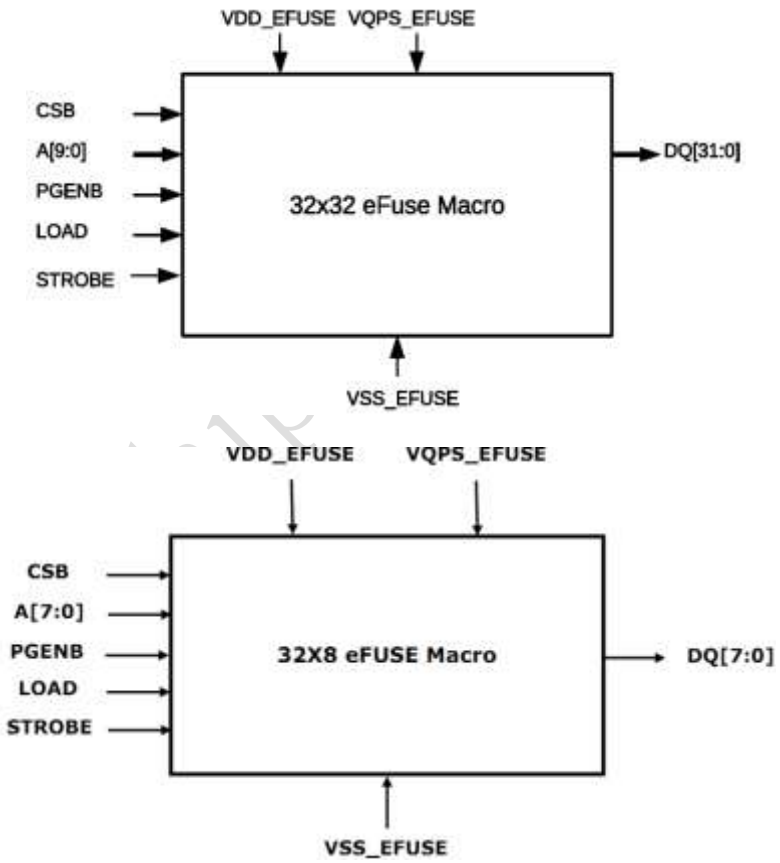

Fig. 19-1 RK3288 eFuse block diagram

19.3 Function description

eFuse has three operation modes. They are defined as standby, read and programming.

Program (PGM) Mode

In order to enter programming mode, the following conditions need to be satisfied: VQPS_EFUSE is at high voltage, LOAD signal is low, PGENB signal is low, and CSB signal is low. All bits can be individually programmed (one at a time) with the proper address selected, the STROBE signal high and the address bits satisfying setup and hold time with respect to STROBE.

Read Mode

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In order to enter read mode the following conditions need to be satisfied: VQPS_EFUSE is at ground, the LOAD signal is high, the PGENB signal is high, and the CSB is low. An entire 8-bit word of data can be read in one read operation with STROBE being high and a proper address selected (address signals A5~A7 are "don't cares").

Standby Mode

Standby is defined when the macro is not being programmed or read. The conditions for standby mode are: the LOAD signal is low, the STROBE signal is low, the CSB signal is high and PGENB is high.

19.4 Register Description

This section describes the control/status registers of the design.

19.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EFUSE_CTRL	0x0000	W	0x00000000	efuse control register
EFUSE_DOUT	0x0004	W	0x00000000	efuse data out register

*Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**- WORD (32 bits) access*

19.4.2 Detail Register Description

EFUSE_CTRL

Address: Operational Base + offset (0x0000)

eFuse control register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
15:6	RW	0x00	efuse_addr efuse address pins : A[7:0] / A[9:0]
5:4	RO	0x0	reserved
3	RW	0x0	efuse_pgenb efuse program enable (active low) :PGENB
2	RW	0x0	efuse_load efuse turn on sense amplifier and load data into latch (active high) : LOAD
1	RW	0x0	efuse_strobe efuse turn on the array for read or program access (active high) : STROBE
0	RW	0x0	efuse_csb efuse chip select enable signal, active low : CSB

EFUSE_DOUT

Address: Operational Base + offset (0x0004)

eFuse data out register

Bit	Attr	Reset Value	Description
31:0	RO	0x00	efuse_dout efuse data output

19.5 Timing Diagram

When efuse is in program(PGM) mode.

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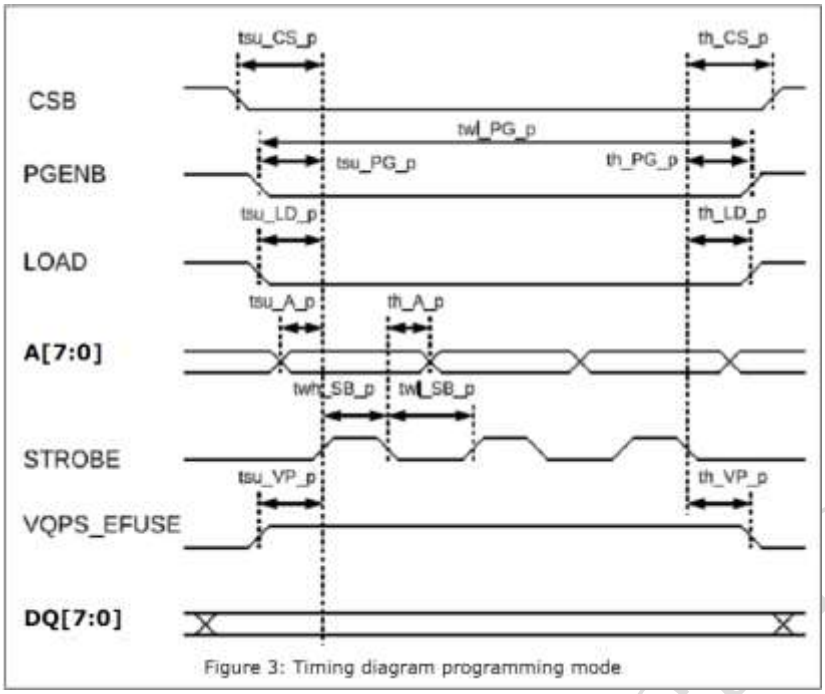

Fig. 19-2 RK3288 efuse timing diagram in program mode

When efuse is in read mode.

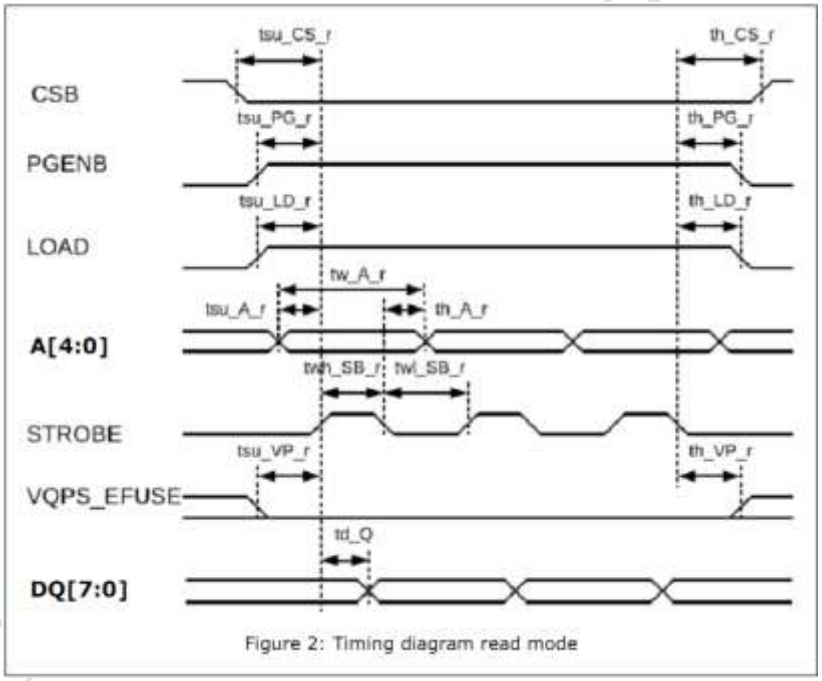

Fig. 19-3 RK3288 efuse timing diagram in read mode

The following table has shows the detailed value for timing parameters in the above diagram.

Table 19-1 RK3288 eFuse timing parameters list

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Mode	Item	Description	Min	Typ	Max	Unit
Read Mode	twh_SB_r	Pulse width high of STROBE read strobe	20		-	ns
	twl_SB_r	Pulse width low of STROBE read strobe	15		-	ns
	tsu_A_r	A[7:0] to STROBE setup time in read mode	25		-	ns
	th_A_r	A[7:0] to STROBE hold time in read mode	3		-	ns
	tw_A_r	A[7:0] pulse width while LOAD high in read mode	48		100	ns
	tsu_CS_r	CSB to STROBE setup time in read mode	16		-	ns
	th_CS_r	CSB to STROBE hold time in read mode	6		-	ns
	tsu_PG_r	PGENB to STROBE setup time in read mode	14		-	ns
	th_PG_r	PGENB to STROBE hold time in read mode	10		-	ns
	tsu_LD_r	LOAD to STROBE setup time in read mode	10		-	ns
	th_LD_r	LOAD to STROBE hold time in read mode	7		-	ns
	tsu_VP_r	VQPS_EFUSE to STROBE setup time in read mode	20		-	ns
	th_VP_r	VQPS_EFUSE to STROBE hold time in read mode	20		-	ns
	td_Q	DQ[7:0] delay time after STROBE high	0		8	ns
PGM Mode	twh_SB_p	Pulse width high of STROBE PGM strobe	9.8	10	10.2	us
	twl_SB_p	Pulse width low of STROBE PGM strobe	15		-	ns
	tsu_A_p	A[7:0] to STROBE setup time in PGM mode	12		-	ns
	th_A_p	A[7:0] to STROBE hold time in PGM mode	3		-	ns
	tsu_CS_p	CSB to STROBE setup time in PGM mode	16		-	ns
	th_CS_p	CSB to STROBE hold time in PGM mode	6		-	ns
	tsu_PG_p	PGENB to STROBE setup time in PGM mode	14		-	ns
	th_PG_p	PGENB to STROBE hold time in PGM mode	10		-	ns
	twl_PG_p	PGENB pulse width low (cumulative) in PGM mode	-		100	ms
	tsu_LD_p	LOAD to STROBE setup time in PGM mode	10		-	ns
	th_LD_p	LOAD to STROBE hold time in PGM mode	7		-	ns
	tsu_VP_p	VQPS_EFUSE to STROBE setup time in PGM mode	20		-	ns
	th_VP_p	VQPS_EFUSE to STROBE hold time in PGM mode	20		-	ns

19.6 Application Notes

During usage of efuse, customers must pay more attention to the following items:

1. In condition of program(PGM) mode, VQPS_EFUSE= 1.5V±10%.

2. Q0~Q7/Q31 will be reset to "0" once CSB at high.

3. No data access allowed at the rising edge of CSB.

4. All the program timing for each signal must be more than the value defined in the timing table.

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Chapter 20 WatchDog

20.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that may be caused by conflicting parts or programs in a SoC.The WDT would generated interrupt or reset signal when it's counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock is pclk
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  Generate a system reset
  First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period

20.2 Block Diagram

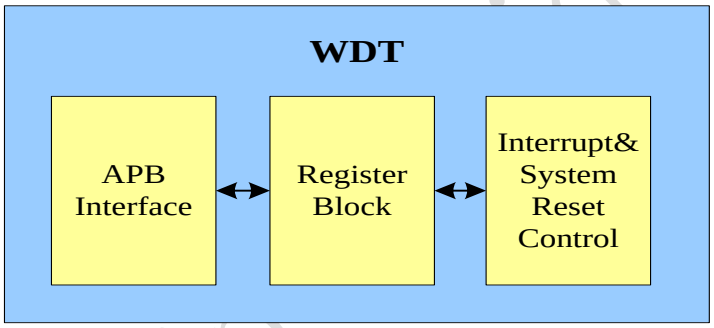

Fig. 20-1 WDT block diagram

Block Descriptions:

APB Interface

The APB Interface implements the APB slave operation. It's data bus width is 32 bits.

Register Block

A register block that read coherence for the current count register.

Interrupt & system reset control

An interrupt/system reset generation block comprising of a decrementing counter and control logic.

20.3 Function description

20.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog

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Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

System Resets

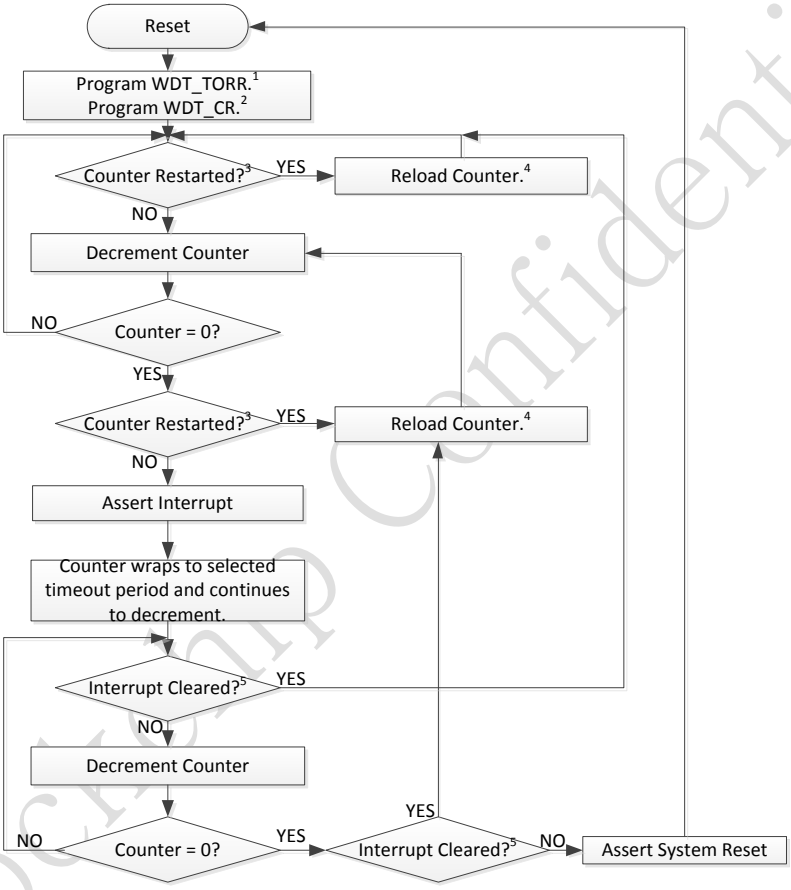
When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

20.3.2 Programming sequence

Operation Flow Chart (Response mode=1)



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 20-2 WDT Operation Flow

20.4 Register Description

This section describes the control/status registers of the design.

20.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x0000000a	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout range Register

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Name	Offset	Size	Reset Value	Description
WDT_CCVR	0x0008	W	0x00000000	Current counter value Register
WDT_CRR	0x000c	W	0x00000000	Counter restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

20.4.2 Detail Register Description

WDT_CR
Address: Operational Base + offset (0x0000)
Control Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:2	RW	0x2	rst_pluse_lenth Reset pulse length. This is used to select the number of pclk cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x1	resp_mode Response mode. Selects the output response generated to a timeout. 1'b0: Generate a system reset 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset
0	RW	0x0	wdt_en WDT enable 1'b0: WDT disabled 1'b1: WDT enabled

WDT_TORR
Address: Operational Base + offset (0x0004)
Timeout range Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	timeout_period Timeout period. This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff 4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR
Address: Operational Base + offset (0x0008)
Current counter value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cur_cnt Current counter value This register, when read, is the current value of the internal counter. This value is read coherently when ever it is read

WDT_CRR
Address: Operational Base + offset (0x000c)
Counter restart Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	W1C	0x00	cnt_restart Counter restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT
Address: Operational Base + offset (0x0010)
Interrupt status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	wdt_status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity. 1'b0: Interrupt is inactive.

WDT_EOI
Address: Operational Base + offset (0x0014)
Interrupt clear Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	wdt_int_clr Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter.

20.5 Application Notes

Please refer to the function description section.

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